An Extended Model for a Punch Through (PT) Insulated Gate Bipolar Transistor (IGBT) And Its Transient Characteristics

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Declaration of Authorship

This is to declare that this thesis named "An Extended Model For A Punch Through (PT) Insulated Gate Bipolar Transistor (IGBT) And Its Transient Characteristics" is submitted by the authors listed for the degree of Bachelor of Science in Electrical and Electronics Engineering to the Department of Electrical of Electronics Engineering under the School of Engineering and Computer Science, BRAC University. We hereby affirm that the research work and result was conducted solely by us and no other. Materials of the study and work found by other researchers have been properly referred and acknowledged. This thesis paper, neither in whole nor in part, has been previously submitted elsewhere for appraisal.

Submission Date: 20th August, 2017

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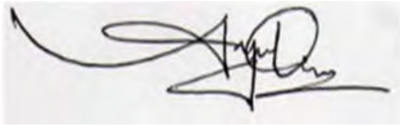

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Abstract

The IGBT (Insulated gate bipolar transistor) is driven by MOSFET and has been modeled as a wide-base bipolar junction transistor (BJT). In our thesis we are proposing to make a new physical-base model for a punch though (PT) IGBT. By manipulating the different region length, depth and doping we will try to obtain better threshold and I-V relation regarding IGBT characteristics and make a new extended model with proper research on its transient characteristics.

Acknowledgement

This note is made to express our gratefulness to some people who really encouraged and supported us a lot in making this report.

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Abbreviations

IGBT	Insulated Gate Bipolar Transistor
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
VDMOSFET	Vertical Double diffused MOSFET
PT IGBT	Punch Through Insulated Gate Bipolar Transistor
NPT IGBT	Non Punch Through Insulated Gate Bipolar Transistor
VFD	Variable frequency Drive
GEMFET	Gain Enhanced MOSFET
COMFET	Conductivity Modulated FET
BiFET	Bipolar FET
PWM	Pulse Width Modulation
UPS	Uninterruptable power Supply
DMOS	Depletion MOSFET
JFET	Junction gate Field Effect Transistor
RTC	Real Time Control
PCM	Plugged Cell Merged

Physical Constants

Ambipolar Diffusivities	D	=	18 cm^2/s
High level excess carrier lifetime	τ_{HL}	=	0.1 μs (τ_0)
		=	0.3 μs (τ_1)
		=	2.45 μs (τ_2)
		=	7.1 μs (τ_3)
Supply voltage	V_{bus}	=	400 V
Dielectric constant of Si	ε_{Si}	=	$11.7 \times 8.854 \times 10^{-14}$ F/cm
Charge of electron	q	=	1.6×10^{-19} C
Base doping concentration	N_B	=	2×10^{14} cm-3
Hole Diffusivity	D_p	=	14 cm^2/s
Metallurgical base width	W_B	=	9.3×10^{-3} cm
Device active area	A	=	0.1 cm^2
Emitter electron saturation current	I_{sne}	=	6×10^{-14} A
Intrinsic carrier concentration	n_i	=	1.45×10^{10} cm^{-3}
Electron mobility	μ_n	=	1500 $cm^2/V\,s$
Hole mobility	μ_p	=	450 $cm^2/V\,s$
Ambipolar mobility ratio	b	=	3.3
Total current	I_T	=	10 A

Symbols

A	Device active area	cm^{-3}
$I\ n, Ip$	electron hole current	A
δp	excess carrier concentration	$cm-3$
n, p	electron, hole carrier concentration	$cm-3$
Q	total excess carrier base charge	C
W_B	metallurgical base width	cm
P_0	excess carrier concentration at x=0	$cm-3$
$\emptyset_n$, $\emptyset_p$	electron,hole quasi-fermi potential	V
E	electric field	V/cm
x	distance in base from emitter	cm
Q	electron charge	C
μ_n, μ_p	electron, hole mobility	cm^{-2}/Vs
D_n , D_p	electron, hole diffusivity	cm^{-2}/s
τ_{HL}	high level excess carrier lifetime	s
$I_T = I_n + I_p$	Total current	A
$b = \frac{\mu_n}{\mu_p}$	ambipolar mobile ratio	-
D	ambipolar diffusivity	cm^{-2}/s
L	ambipolar diffusion length	cm

Chapter 1

Introduction

An Insulated-Gate Bipolar Transistor (IGBT) is a three-terminal power semiconductor device primarily used as an electronic switch which, as it was developed, came to combine high efficiency and fast switching. Since it is designed to turn on and off rapidly, amplifiers that use it often synthesize complex waveforms with pulse-width modulation and low-pass filters. In switching applications modern devices feature pulse repetition rates well into the ultrasonic range—frequencies which are at least ten times the highest audio frequency handled by the device when used as an analog audio amplifier.

The IGBT transistor takes the best parts of two types of transistors, the high input impedance and high switching speeds of a MOSFET with the low saturation voltage of a bipolar transistor, and combines them together to produce another type of transistor switching device that is capable of handling large collector-emitter currents with virtually zero gate current drive. The Insulated Gate Bipolar Transistor, (IGBT) combines the insulated gate (hence the first part of its name) technology of the MOSFET with the output performance characteristics of a conventional bipolar transistor, (hence the second part of its name). The result of this hybrid combination is that the "IGBT Transistor" has the output switching and conduction characteristics of a bipolar transistor but is voltage-controlled like a MOSFET.

IGBTs are mainly used in power electronics applications, such as inverters, converters and power supplies, were the demands of the solid state switching device are not fully met by power bipolar and power MOSFETs. High-current and high-voltage bipolar are available, but their switching speeds are slow, while power MOSFETs may have higher switching speeds, but high-voltage and high-current devices are expensive and hard to achieve. IGBT has many others

applications also such as variable frequency drives (VFDs), electric cars, trains, variable speed refrigerators, lamp ballasts, air-conditioners and even stereo systems with switching amplifiers.

The main advantages of IGBT over a Power MOSFET and a BJT are

- It has a very low on-state voltage drop due to conductivity modulation and has superior on-state current density. So smaller chip size is possible and the cost can be reduced.
- It offers greater power gain than the standard bipolar type transistor combined with the higher voltage operation and lower input losses of the MOSFET. In effect it is an FET integrated with a bipolar transistor in a form of Darlington type configuration.
- Wide SOA: It has superior current conduction capability compared with the bipolar transistor. It also has excellent forward and reverse blocking Capabilities.
- It has lower on-state and switching losses and also lowers thermal impedance.
- Low driving power and a simple drive circuit due to the input MOS gate structure. It can be easily controlled as compared to current controlled devices (thyristor, BJT) in high voltage and high current applications.

Main drawbacks are:

- The switching frequency of insulated gate bipolar transistor (IGBT) is not as high as that of a power MOSFET. The collector current following due to the minority charge carriers roots the turnoff speed to be slow.
- It cannot block high reverse voltages.
- There is a chance of latch up due to the internal structure of PNPN thyristor.

We can see that the insulated gate bipolar transistor is a three terminal, transconductance device that combines an insulated gate N-channel MOSFET input with a PNP bipolar transistor output connected in a type of Darlington configuration. As a result the terminals are labelled as: **Collector**, **Emitter** and **Gate**. Two of its terminals (C-E) are associated with the conductance path which passes current, while its third terminal (G) controls the device

IGBT Comparison Table [1]			
Device Characteristic	Power Bipolar	Power MOSFET	IGBT
Voltage Rating	High <1kV	High <1kV	Very High >1kV
Current Rating	High <500A	High > 500A	High >500A
Input Drive	Current ratio h_{FE} 20-200	Voltage V_{GS} 3-10V	Voltage V_{GE} 4-8V
Input Impedance	Low	High	High
Output Impedance	Low	Medium	Low
Switching Speed	Slow (µs)	Fast (ns)	Medium
Cost	Low	Medium	High

Table 1.1 Characteristics comparison of IGBT

.An insulated gate bipolar transistor is simply turned “ON” or “OFF” by activating and deactivating its Gate terminal. Applying a positive input voltage signal across the Gate and the Emitter will keep the device in its “ON” state, while making the input gate signal zero or slightly negative will cause it to turn “OFF” in much the same way as a bipolar transistor or a MOSFET.

1.1 Device Evolution: BJT, MOSFET and IGBT

The bipolar transistor was the only “real” power transistor until the MOSFET came along in the 1970’s. The bipolar transistor requires a high base current to turn on, has relatively slow turnoff characteristics (known as current tail), and is liable for thermal runaway due to a negative temperature co-efficient. In addition, the lowest attainable on-state voltage or conduction loss is governed by the collector-emitter saturation voltage $V_{CE(SAT)}$.

The MOSFET, however, is a device that is voltage- and not current-controlled. MOSFETs have a positive temperature co-efficient, stopping thermal runaway. The on-state-resistance has no theoretical limit; hence on-state losses can be far lower. The MOSFET also has a body-drain

diode, which is particularly useful in dealing with limited freewheeling currents. All these advantages and the comparative elimination of the current tail soon meant that the MOSFET became the device of choice for power switch designs.

Then in the 1980s the IGBT came along. The IGBT is a cross between the bipolar and MOSFET transistors. Early versions of the IGBT are also prone to latch up, but nowadays, this is pretty well eliminated. Another potential problem with some IGBT types is the negative temperature co-efficient, which could lead to thermal runaway and makes the paralleling of devices hard to effectively achieve. This problem is now being addressed in the latest generations of IGBTs that are based on "non-punch through" (NPT) technology. This technology has the same basic IGBT structure but is based on bulk-diffused silicon, rather than the epitaxial material that both IGBTs and MOSFETs have historically used.

Characteristics	MOSFET	IGBT	BJT
Type of drive	voltage	voltage	current
Drive power	Minimal	Minimal	Large
Drive complexity	simple	simple	High (large positive and negative currents required)
Current density for given voltage drop	High at low voltage. Low at high voltages.	Very high(small tradeoff with switching speed)	Medium (severe trade-off with switching speed)
Switching losses	Very low	Low to medium (depending on trade-off with conduction losses)	Medium to high (depending on tradeoff with conduction losses)

Table 1.1.1 Comparison among MOSFET, IGBT and BJT

1.2 Advent of IGBTs

Insulated Gate Bipolar Transistor (IGBT) emerged to be the milestone breakthrough in the sphere of power semiconductor devices. Figure 1.1 gives a general classification overview of all the traditional power semiconductor devices found in today's technology.

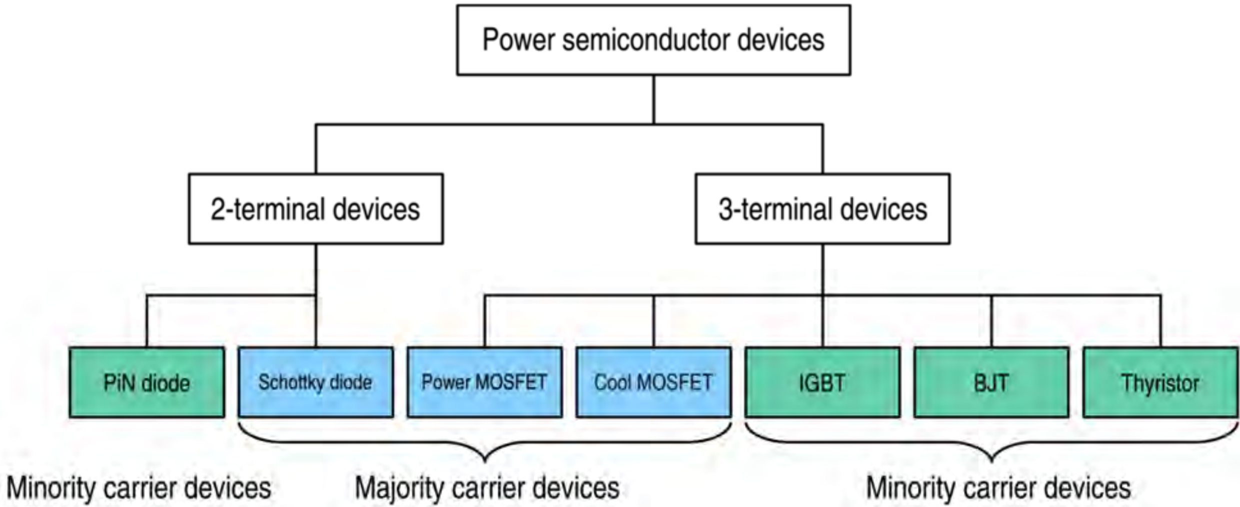


Figure 1.1 the power devices family, showing the principal power switches

IGBT was demonstrated for the first time by Baliga in 1979 Over the years it has been referred to by numerous other names which includes Insulated Gate Rectifier (IGR), Conductivity-Modulated FET (COMFET), Gain-Enhanced MOSFET (GEMFET), Bipolar FET (BiFET) and Injector FET. It became commercially available in 1983.

IGBTs are inherently a minority carrier device where the current conduction takes place through both the majority and minority carriers of the semiconductor material it is composed of. It is generally viewed as a device with MOS input characteristics and bipolar output characteristics that is a voltage-controlled bipolar device. Indeed, in principle, it has a very high input impedance and large bipolar current-carrying capability thus allowing the users to combine the advantages of Power MOSFET and BJT into a single monolithic device.

IGBTs have found numerous applications in various power electronic systems, especially in Pulse Width Modulated (PWM) servo and three-phase drives requiring high dynamic range control and low noise. It is also an essential component in Uninterruptible Power Supplies (UPS), Switched-Mode Power Supplies (SMPS), and other power circuits requiring high switch repetition rates. IGBT improves dynamic performance and efficiency and reduces the level of audible noise. It is equally suitable in resonant-mode converter circuits. Optimized IGBT is available for both low conduction loss and low switching loss.

Chapter 2

Basic Principles of IGBT

2.1 Basic Structure of IGBT

2.1.1 Cross Sectional Structure of IGBT

The basic schematic of a typical N-channel IGBT build on DMOS process that shown in Figure 2.1. This is one of many structures possible for this device. It is noticeable that the silicon cross section of an IGBT is almost identical of that of a vertical Power MOSFET except for the P+ injecting layer. It shares similar MOS gate structure and P wells with N+ source regions. At the top N+ layer is the source or emitter and at the bottom P+ layer is the drain or collector. It is also achievable to make P-channel IGBTs and which the doping profile in each layer will be reversed. IGBT has a parasitic thyristor comprising the four-layer NPN structure. Turn on of this thyristor is undesirable. There are different types of IGBT which are manufactured without the N+ buffet layer they are called non-punch through (NPT) IGBTs whereas those with this layer are called punch-through (PT) IGBTs. The presence of this buffer layer can significantly improve the performance of the device if the doping level and thickness of this layer are chosen appropriately.

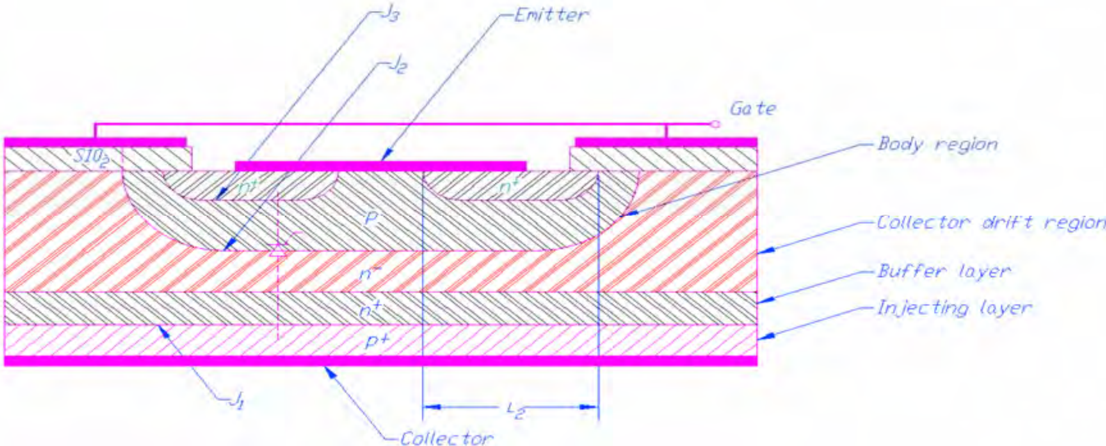


Figure 2.1.1 Schematic view of a Generic N-Channel IGBT

Despite physical similarities, the operation of an IGBT is closer to that of a power BJT than a power MOSFET. It is due to the drain layer (injecting layer) which is responsible for the minority carrier injection into the N-drift region and the resulting conductivity modulation.

2.1.2 NPT-IGBT and PT-IGBT

The NPT and PT-IGBT's are developed by IXYS Corporation. The physical construction of the NPT and PT IGBTs are shown in figure 2.1.2. The structure of PT consists of an extra buffer layer that executes two functions they are, 1) the failure can be avoided by punch through action as the depletion area expansion at applied high voltage is controlled by this layer. 2) Fail current can be reduced when it turns off & reduces the fall time of the IGBT because the holes are inserted by the collector of the P+ incompletely recombine in this layer.

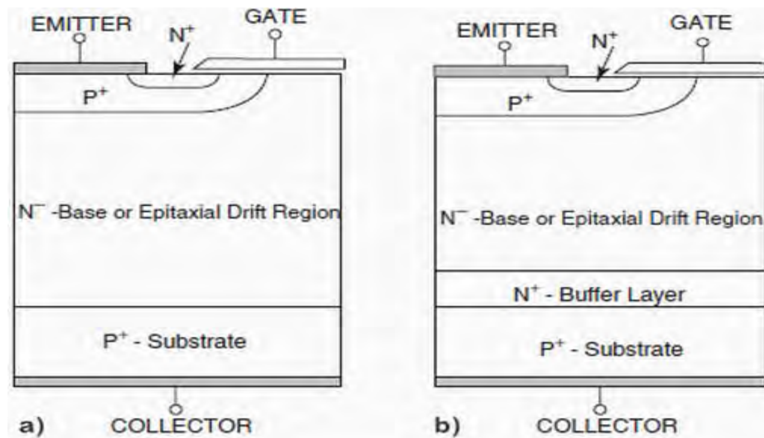


Figure 2.1.2 NPT-IGBT and PT-IGBT

The basics of NPT-IGBT, IXYS Corporation 4 IXAN0063 and Abdus Sattar have equal breakdown voltage and these are applicable for AC applications. The PT-IGBTs have less breakdown voltage and these are relevant for DC circuits where these devices are not essential to support voltage in the reverse direction.

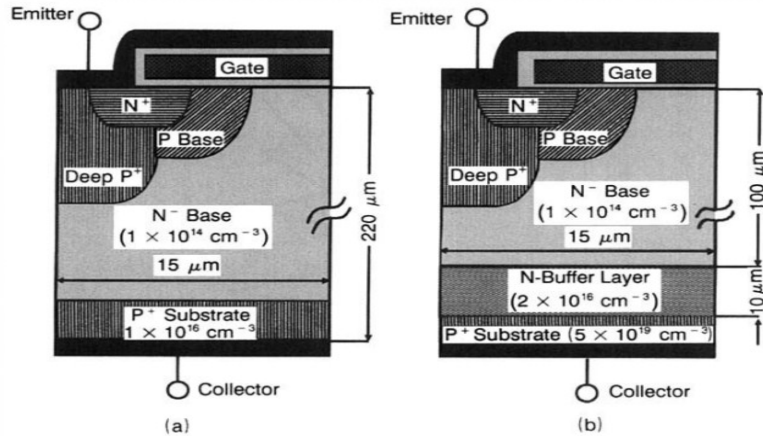


Figure 2.1.3 Cross Sectional Structure of (a) NPT IGBT & (b) PT IGBT

The NPT IGBTs, which have equal forward and reverse breakdown voltage, are suitable for AC applications. The PT IGBTs, which have less reverse breakdown voltage than the forward breakdown voltage, are applicable for DC circuits where devices are not required to support voltage in the reverse direction. Fig. 2.1.4 shows the Doping Concentration & Electric Field distribution of NPT & PT IGBT.

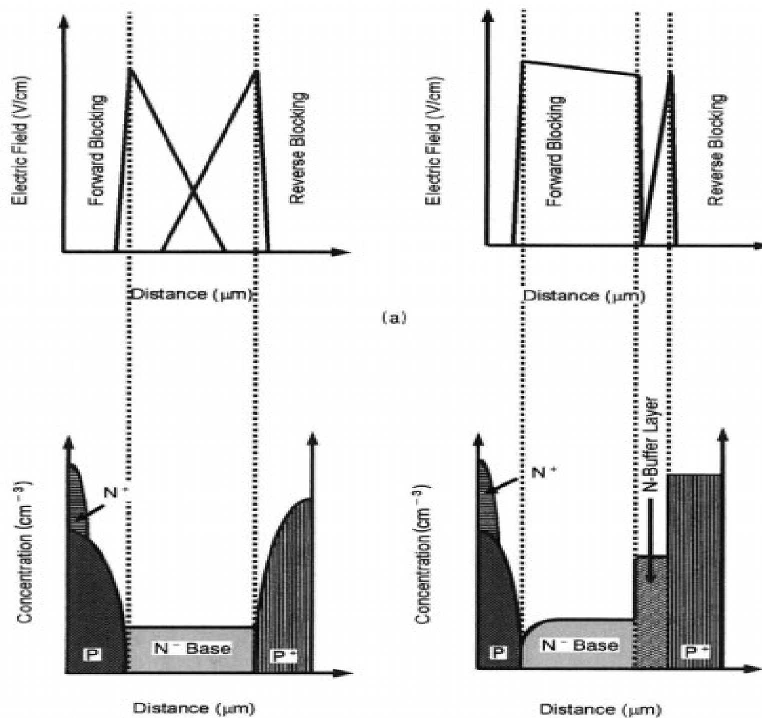


Figure 2.1.4 Doping Concentration & Electric Field Distribution (a) NPT IGBT & (b) PT IGBT

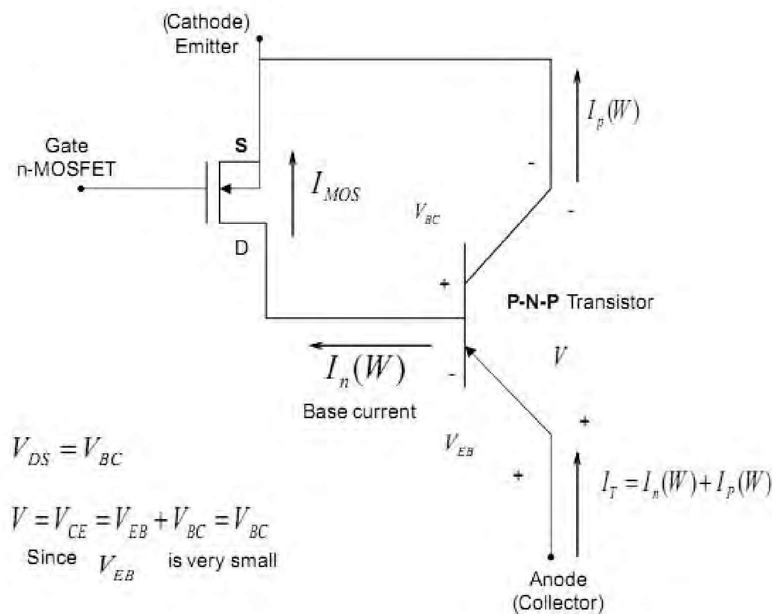


Figure 2.1.5 the equivalent circuit model of IGBT

2.1.3 Difference between NPT-IGBT and PT-IGBT

It is a voltage controlled device and it needs a small amount of voltage on the gate terminal to keep conduction through the device. This is a unidirectional device because, it can only change current in the forward direction that is collector-to-emitter.

	NPT	**PT**
Switching Loss	**Medium** Long, low amplitude tail current. Moderate increase in E_{off} with temperature	**Low** Short tail current Significant increase in E_{off} with temperature
Conduction Loss	**Medium** Increases with temperature	**Low** Flat to slight decrease with temperature
Paralleling	**Easy** Optional sorting Recommend share heat	**Difficult** Must sort on $V_{CE(on)}$
Short-Circuit Rated	**Yes**	**Limited** High gain

Table 2.1.2 Difference between NPT-IGBT and PT-IGBT

The principle of the BJTs is very similar to the N-channel MOSFET. The main difference is, the current existing by the conducting channel when current supplies through the device in its ON state is very small in the IGBT, due to this reason, the ratings of the currents are high when matched with an MOSFET.

2.2 Switching Behavior of IGBT

These devices are mostly used as switches, for instance frequency converter and chopper applications, the variation of a diode is most important, because when the switching of the IGBT is OFF, then the current is determined by the load that is inductive in many cases.

By connecting appropriate diodes, the current flow is allowed. When this transistor is switched on again, the current flowing in a diode at first works like a short. The voltage can be blocked by removing the stored voltage. This looks as a surplus current added to the load current which is called as the reverse recovery current of the diode 'Irr'. The max of Irr occurs (di/dt = 0) when the amount of the sudden voltages through the IGBT & the diode matches the supply voltage. When the IGBT is turned ON, then the current changes which make an over-voltage point by the change in the current in the dependent inductances agreeing to $\Delta VCE = L\sigma \times di/d$

2.3 Principles of Operation of IGBT

2.3.1 Circuit Diagram of IGBT

Based on the basic structure of the IGBT, a simple circuit can be drawn using PNP and NPN Transistors, JFET, MOSFET, that is shown in the below figure 2.3.1 The collector terminal of the NPN transistor is connected to the base terminal of the PNP via JFET transistor. These transistors signify the parasitic thyristor which creates a regenerative feedback loop. The RB resistor signifies the shorting of the base-emitter terminals of the NPN transistor to ensure that the thyristor doesn't latch up that will lead to the IGBT latch-up.

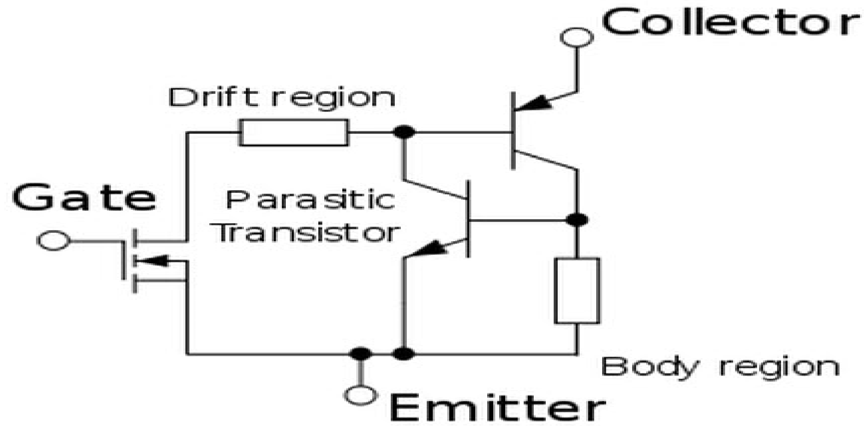


Figure 2.3.1 Circuit Diagram of an IGBT

The JFET transistor signifies the construction of current b/n any two adjacent IGBT cells. It allows the MOSFET and supports most of the voltage. A circuit symbol for the IGBT is shown below, that consists of three terminals namely emitter, gate and collector.

2.3.2 Equivalent Circuit of IGBT

The equivalent circuit of the IGBT can be depicted quite accurately by a pnp-transistor, where the base current is controlled by a MOS transistor. The conductivity of the resistor on the base branch is increased (modulated) when the IGBT is turned-on. This way, the greater part of the load current is flowing over the base branch. These effects only show for the user by a turn-on delay time and a tail current at turn-off. For this reason, the device can be simply considered as a MOS transistor with the corresponding capacities.

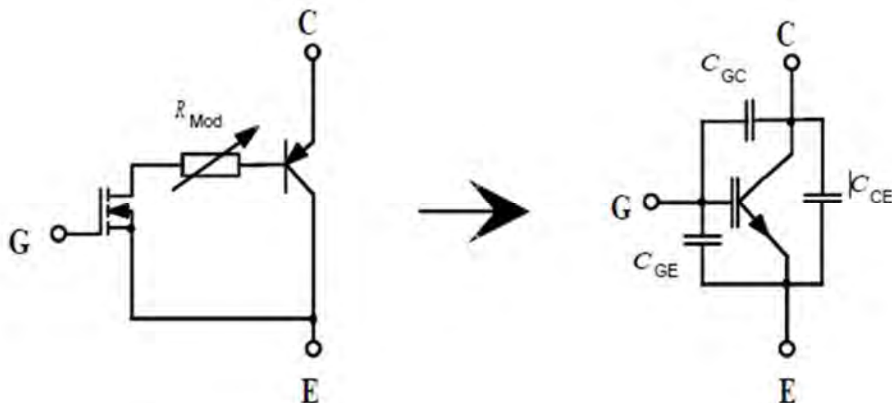


Figure 2.3.2 Equivalent Circuit of the IGBT

Based on the structure, an equivalent circuit of IGBT can be shown in Fig. 2.3.3 It consists of a PNP transistor (BJT) & an n-channel MOSFET. The p^+ substrate, n^- epilayer & p^+ body forms the PNP transistor. The p-type substrate is the emitter for BJT and is the anode terminal of the device. When the p substrate is forward biased (V_{EB}=0), the minority carrier injection causes transistor current I_T, flowing from the anode region.

This current has two parts at the Base-

- Electron current ($I_n(W)$).
- Hole current ($I_p(W)$).

The Anode to Cathode voltage (V_{AC}) can be represented by

$$V_{AC} = V_{EB} + V_{BC}$$

Where,

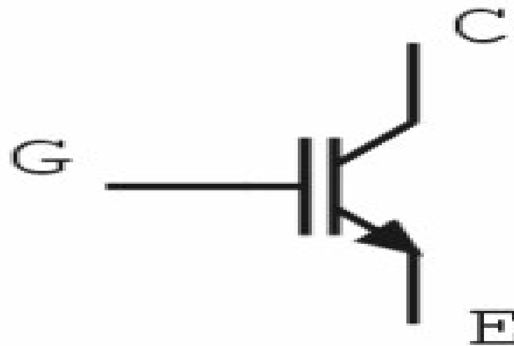


Figure 2.3.3 The Circuit symbol of IGBT

V_{EB}=Bipolar Emitter to Base voltage.

V_{BC}=Base to Cathode voltage.

Basically V_{DS} of MOSFET & V_{BC} are same. Since V_{EB} is very small, we can write

$$V_{AC} = V_{BC}$$

From the equivalent circuit, a circuit symbol can be formed which is shown in Fig. 2.3.3
It has three parts-

- Collector (C) which is the anode terminal of IGBT.
- Gate (G) which is the Gate terminal of MOSFET.
- Emitter (E) which is the cathode terminal of IGBT

2.3.3 IGBT Operation

When a positive gate voltage greater than the threshold voltage (V_T) is applied, electrons are attracted from the p^+ body towards the surface under the gate. These attracted electrons will invert the p^+ body region directly under the gate to form an n channel.

A path is formed for charges to flow between the n^+ source and the n^- drift region.

When a positive voltage is applied to the anode terminal of the IGBT, the emitter of the IGBT section is at higher voltage than collector. Minority carriers (holes) are injected from the emitter (p^+ region) into the base (n^- drift region). As the positive bias on the emitter of the BJT part of the IGBT increases, the concentration of the injected hole increases as well. The concentration of the injected holes will eventually exceed the background doping level of the n^- drift region; hence the conductivity modulation phenomenon. The injected carriers reduce the resistance of the n^- drift region and, as a result, the injected holes are recombined with the electrons flowing from the source of the MOSFET to produce the anode current (on state).

When a negative voltage is applied to the anode terminal, the emitter-base junction is reversed biased and the current is reduced to zero. A large voltage drop appears in the n^- drift region since the depletion layer extends mainly into that region.

The MOSFET gate voltage controls the IGBT switching action. The turn-OFF takes place when the gate voltage is less than the threshold voltage (V_T). The inversion layer at the surface of the p^+ body under the gate cannot be kept and therefore no electron current is available in the

MOSFET channel while the remaining minority carriers of holes, which were stored during the on state of the IGBT, require some time in order to be removed or extracted.

The switching speed of the IGBT device depends upon the time it takes for the removal of the stored charges in the n^- drift region which were built up during the on state current conduction (IGBT tern-on case).

2.4 Basic Tools for Operation

The Physics-based modeling approach is used in this discussion to better understand the effect of the carriers on the IGBT characteristics. The following points have to be taken into account in performing the analysis.

- The carrier distribution in the n-drift region of the IGBT is described by the ambipolar diffusion equation because of the high level injection of holes in this region ($p(x) >> N_B$)

$$\frac{\partial^2 p(x)}{\partial x^2} = \frac{p(x)}{L^2} + \frac{1}{D}\frac{\partial p(x)}{\partial x}$$

Where,

- N_B= Base background doping concentration
- P(x)= Hole concentration
- D= Ambipolar diffusion constant
- T_{HL}= Hole carrier lifetime
- $L = \sqrt{D\tau_{HL}}$=Bipolar diffusion length

- Transport of the bipolar charge is assumed to be one-dimensional (1-D) for the ease of analysis.

- The emitter region of the BJT part of the IGBT has a very high doping concentration level ($p^+ >> 10^{18} cm^{-3}$). This region acts like recombination centers for minority carriers coming from the lightly doped base region (electron in this case).

The space charge region, which is depleted of minority carriers, supports the entire voltage drop across the collector-base terminals based on Poisson's equation. The effect of mobile carriers in the depletion region is not accounted for in this dissertation.

2.4.1 The Steady State Operation

The equivalent circuit model and 1-D coordinate system of Fig. 2.6 is used in the modeling approach of the NPT IGBT analysis. From this figure, I_T is the IGBT total current, I_p is the hole current of the BJT and I_n is the base or MOS electron current.

I_T can be expressed in several ways:

$$I_T = I_p(x = 0) + I_n(x = 0) \tag{2.1}$$

$$I_T = I_p(x = W) + I_n(x = W) \tag{2.2}$$

$$I_T = I_p(x) + I_n(x) \tag{2.3}$$

The IGBT operates under low gain and high level injection conditions.

The current equations are as

$$J_n = nq\mu_n E + qD_n \frac{\partial n(x)}{\partial x} \tag{2.4}$$

$$J_p = pq\mu_p E - qD_p \frac{\partial p(x)}{\partial x} \tag{2.5}$$

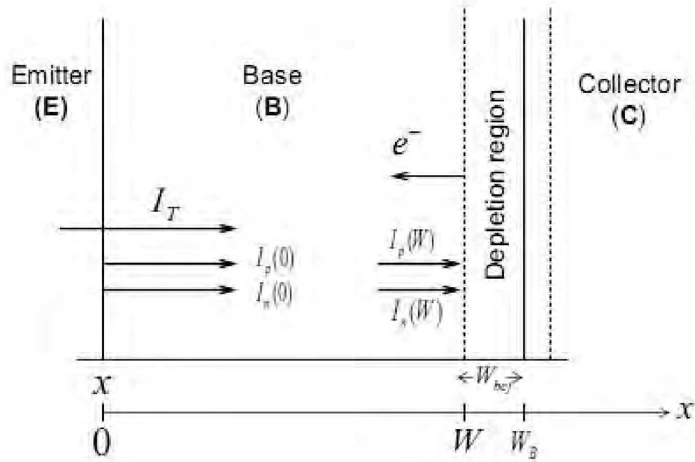


Figure 2.4.1 1-D coordinate system used in the modeling of the NPT IGBT

where J_n is the electron current & J_p is the hole current

The first terms in equations 2.4 & 2.5 are due to drift component while the second terms are due to diffusion component.

When the excess carrier concentration is larger than the background concentration the transport of electrons and holes are coupled by the electric field in the drift terms of the transport equations. The minority carrier current density J_n cannot be neglected and ends up affecting the majority carrier current density J_p. Hence equations 2.4 & 2.5 cannot be coupled. The total current density is given by

$$\begin{aligned} J_T &= J_n + J_p \\ &= (nq\mu_n + pq\mu_p)E + q\left(D_n \frac{\partial n(x)}{\partial x} - D_p \frac{\partial p(x)}{\partial x}\right) \end{aligned}$$

substituting for the electric field from the equations 2.4 yields

$$J_n = \left[\frac{nq\mu_n}{nq\mu_n + pq\mu_p}\right] J_T + q\frac{\partial n}{\partial x}\left[\frac{nq\mu_n D_p + pq\mu_p D_n}{nq\mu_n + pq\mu_p}\right]$$

An ambipolar diffusion coefficient D is defined as

$$D = \frac{nq\mu_n D_p + pq\mu_p D_n}{nq\mu_n + pq\mu_p}$$

The expression for J_n can be rearranged & rewritten as

$$J_n = \left[\frac{b}{1+b}\right] J_T + qD\frac{\partial n}{\partial x} \qquad (2.6)$$

where $b=\mu_n/\mu_p$

Repeating the same procedure starting with equation (2.6), J_p is obtained

$$J_p = \left[\frac{1}{1+b}\right] J_T - qD\frac{\partial p}{\partial x} \qquad (2.7)$$

where J_T is the total current density=J_n+J_p & assuming n=p

The excess hole carrier distribution p(x) can be obtained by solving the steady state hole continuity equation

$$\frac{\partial^2 p(x)}{\partial x^2} = \frac{p(x)}{L^2} \quad (2.8)$$

Considering the coordinate system given in Fig. 2.4.1, the boundary conditions for the excess hole carrier distribution are

$$p(x=0) = P_0 \qquad (2.9) \quad p(x=W) = 0 \qquad (2.10)$$

Equation (2.10) results from the collector-base junction being reversed biased for forward condition and equation (2.10) reflects that emitter-base junction is forward biased.

P_0 is the excess carrier concentration at x=0, W(t) is the quasi-neutral base width

given by

$$W = W_B - W_{bcj} \quad (2.11)$$

where W_B is the metallurgical base width and W_{bcj} is the collector-base depletion width. We know, Poisson's equation

$$\frac{d^2V}{dx^2} = \frac{qN_B}{\varepsilon_{Si}} \quad (2.12)$$

Solving Poisson's equation yields an expression for the collector-base junction depletion width as

$$W_{bcj} = \sqrt{\frac{2\varepsilon_{Si}V_{bc}}{qN_B}} \quad (2.13)$$

where N_B is the doping concentration of the lightly doped region of the IGBT and ε_{Si} is the dielectric constant of silicon. The junction voltage V_{bcj}=V=V_{bc}+V_{bi} is the collector base junction voltage drop of the BJT part of the IGBT and V_{bi} is the built in potential. Hence from Fig. 2.4.1

$$W = W_B - \sqrt{\frac{2\varepsilon_{Si}V}{qN_B}} \quad (2.14)$$

Where, $V=V_{bc}=V_{BE}=V_A$ is the collector base voltage that appears across the drift region.

2.4.2 The Transient State Operation

While the turn-on time of the IGBT is quite fast, the turn-off time can be slow because of the open base of the PNP transistor during the turn-off period. Fig. 2.4.2 shows the typical IGBT turn-off transient where $I_T(0^+)$ is the current after the initial rapid fall. The initial rapid drop in the anode current is due to the sudden removal of the MOS channel. This is followed by a slower decay due to the removal of the carriers stored in the lightly doped layer(n^-). The turn-off process is initiated when we lower the gate voltage to a value lower than threshold voltage(V_T)

(first phase). This removes the formed electron channel from under the gate and blocks the MOS component of the current I_{MOS}. $I_{MOS}=I_n(W)=0$ in this case and the collector-base voltage V_{bc} increases resulting in a widening of the depletion region at the n^- (base-collector side or source of MOSFET).

The relation between $I_T\,(0^-)$ and $I_T\,(0^+)$ is through β_{tr}. It is the ratio of the current immediately after the initial rapid fall to the magnitude of the fall and is shown along with the ratio of W(t) to L (W(t)/L) in the appendices.

The switching losses of the IGBT are dominated by the losses, which occur during the much slower second phase of the turn-off period transient. This is because of the time required removing or extracting the injected carriers in this phase. This is a major disadvantage of the IGBT device as it suffers from high-switching losses. This can be overcome by reducing the lifetime of the carriers in the base through recombination of extraction processes quickly as possible before the device reaches its blocking voltage state.

The collector-base junction is reversed biased and its depletion region widens during the turn-off of the IGBT. When the IGBT is on, the status of the base-collector junction is reversed biased as can be seen from Fig. 2.1.5 When the IGBT is off, the status of the base-collector junction is reversed biased and V_{bc} is increased leading to the increment of the depletion region since the current decreases. The widened region supports the entire voltage drop across the device as mentioned previously based on

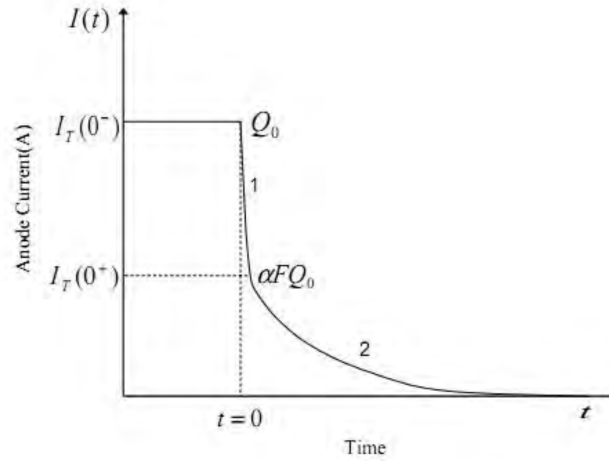


Figure 2.4.2 typical IGBT turn-off transient showing turn-off phases (1 &2)

Poisson's equation. Since the quasi-neutral base width of the IGBT changes with time and decreases with the increase of V_{bc}, we can find an expression for the rate of rise of the voltage across the device $\frac{dV(t)}{dt}$ (varying of the output voltage) during the switching OFF of the IGBT from the collector-base junction depletion width W_{bcj} expression as shown. From $W_{bcj} = \sqrt{\frac{2\varepsilon_{Si} V_{bc}(t)}{qN_B}}$ and the fact that W(t)=W_B-$W_{bcj}(t)$ if we take the time derivative of $W_{bcj}(t)$ we get,

$$\frac{dW_{bcj}(t)}{dt} = \sqrt{\frac{\varepsilon_{Si}}{2qN_B V(t)}} \frac{dV(t)}{dt}$$

and

$$\frac{dW(t)}{dt} = -\frac{dW_{bcj}(t)}{dt} = -\sqrt{\frac{\varepsilon_{Si}}{2qN_B V(t)}} \frac{dV(t)}{dt} \tag{2.15}$$

This equation shows the time rate of the change of the quasi-neutral base width (W(t)) that covers almost all the length across the drift region during the turn-off since the collector-base junction is reversed biased.

2.5 IGBT Generation Improvement

Summarizes the main characteristics of five generations of IGBT chips. Each generation represents an incremental improvement in performance obtained through continuous process

optimization and new chip structures. To understand this evolution it is useful to consider each generation of the IGBT chip in terms of its surface structure and vertical design. The following sections present a brief description of the key technologies developed to allow dramatic improvements in chip efficiency.

2.5.1 Surface Structure

Early improvements in IGBT performance were attained primarily through finer surface patterns and shallow diffusion processing technologies. These techniques enabled significant reductions in cell size thereby allowing more active channel width per unit of chip area. The increased channel width reduces the RDS(on) of the MOSFET portion of the chip which yields reduced V_{CE}(sat). The effect of this process refinement is highlighted by the simultaneous reduction of V_{CE}(sat) and required chip area for the generation 1 through 3 IGBTs shown in Table 2.5.11. Unfortunately, this approach reached the point of severely diminishing returns due to the so-called "parasitic JFET" resistance between adjacent cells in the MOSFET portion of the device.

Table 1 IGBT Generation Comparison 100A, 1200V IGBT					
	1st Gen. 1988	2nd Gen. 1990	3rd Gen. 1992	4th Gen. 1998	5th Gen. 2000
Family Name	---------	E-Series	H-Series	F-Series	NF-Series
Base Wafer Material	Epitaxial	Epitaxial	Epitaxial	Epitaxial	Float Zone
Surface Pattern	5µm Planar	5µm Planar	3µm Planar	1µm Trench	1µm Trench PCM
Vertical Design	PT	PT	PT	PT	LPT-CSTBT
$V_{CE(sat)}$ @ $I_{C(rated)}$	3.5V	2.8V	2.5V	1.9V	1.9V
SWSOA	Over 300A	Over 300A	Over 300A	Over 400A	Over 400A
Chip Size	2p 12x12	2p 12x12	2p 10x10	1p 9.1 x 11.5	1p
Gate Charge Q_G	760nC	1100nC	500nC	1100nC	675nC
Short-Circuit Current	800A	800A	600A	1500A (Without RTC)	500A
Short-Circuit Withstanding $t_{W(crit)}$	15µs	15µs	20µs	5µs 20µs With RTC	20µs

Table 2.5.1 IGBT generation comparison

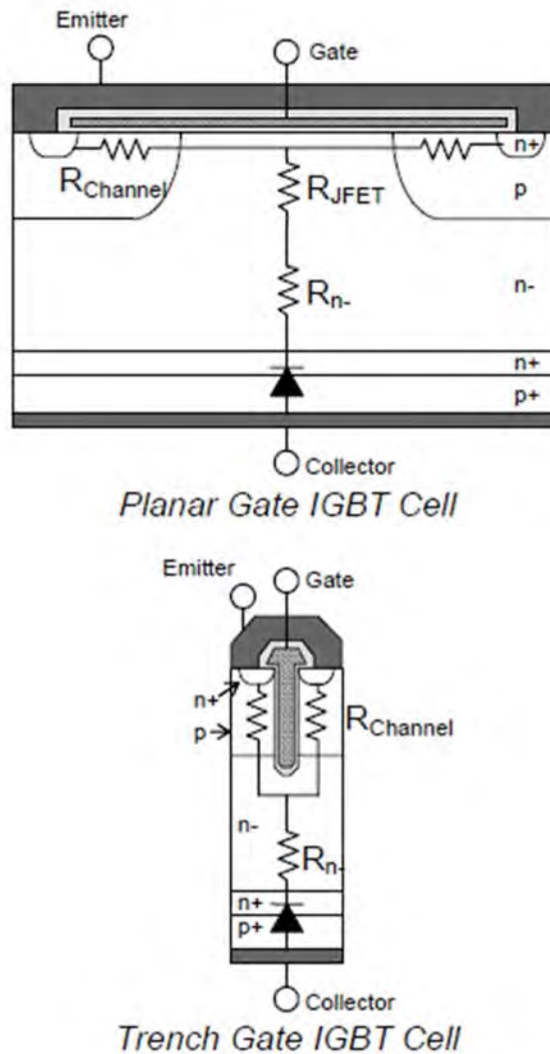


Figure 2.5.1 Unit cell comparison

One way to circumvent this problem is to adopt a high cell density trench-gate surface structure. A comparison of this structure to a conventional planar gate structure is illustrated in figure 2.5.1. In the trench gate structure the gate oxide and conductive polysilicon are formed in a deep narrow trench in the surface of the IGBT chip. This structure eliminates the parasitic JFET resistance and allows further reduction of cell size compared to conventional planar gated devices. The high density trench structure exhibits significant improvements in chip performance compared to planar gated predecessors. The significant advantage of the trench gate in terms of reduced V_{CE}(sat) can be seen in the transition from third to fourth generation in table 2.5.1. The

high cell density trench gate structure has two notable drawbacks. First, high cell density trench gate devices tend to have high short-circuit saturation currents. This characteristic degrades short-circuit withstanding capability of the device under low impedance fault conditions. To recover the short-circuit withstanding capability required for many industrial applications; it was necessary to add an additional current limiting circuit. An example of such a circuit is shown in figure 2.5.1 This circuit called an “RTC” or Real Time Control effectively restores short circuit withstanding capability by actively reducing the gate voltage when the current through the device exceeds approximately three times the device’s nominal rated current. Unfortunately, the addition of the RTC to the module increases its complexity and cost. Secondly, the high cell density trench gate device often exhibits significantly increased gate capacitance compared to their planar-gated predecessors. This characteristic can also be seen in the transition from 3rd to 4th generation in table 2.5.1. The larger gate capacitance results in an undesirable increase in gate drive power requirements.

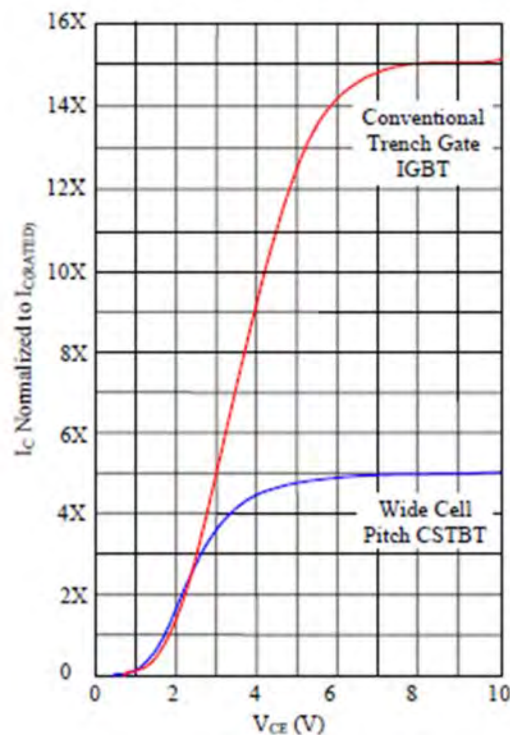


Figure 2.5.2 Effect of wide cell pitch on short circuit saturation current

One effective way to reduce the short-circuit saturation current, improve short-circuit ruggedness and reduce gate capacitance is to reduce the total channel width of the MOSFET part of the

IGBT structure. This can be accomplished by utilizing a wider trench pitch. Figure 2.5.2 shows the reduction of short circuit current resulting from increasing the trench pitch. This technique was found to be extremely useful for optimizing the trade-off between short circuit durability and V_{CE}(sat). To allow easy adjustment of cell pitch using only two mask changes a technique called "PCM" or Plugged Cell Merged was developed. In the PCM device some portion on the trenches are "plugged" by shorting their polysilicon gate to the emitter electrode. The PCM structure is shown along with conventional planar and high cell density trench gate devices in figure 2.5.3. Another advantage to the PCM process is that it produces a distributed drain source capacitance in the MOSFET portion of the device. The distributed capacitance helps to damp oscillations during severe dynamic conditions. Unfortunately, reducing the channel width increases the RDS(ON) of the MOSFET portion of the device resulting in an increased V_{CE}(sat). In the next section of this paper it will be shown that this undesirable increase in vertical structure.

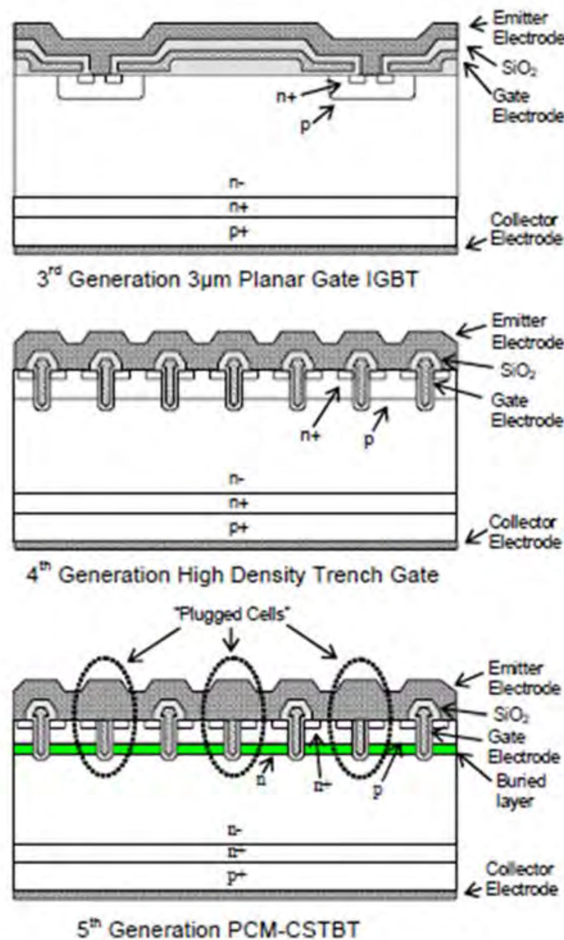


Figure 2.5.3 IGBT surface structure comparison

2.5.2 Vertical Structure

A schematic comparison of common IGBT vertical structures is shown in figure 2.5.4. The first successful industrial IGBT modules used almost exclusively the PT(Epi) (Punch-Through Epitaxial) structure. In this structure the main blocking junction is formed by the lightly doped n- depletion layer and relatively heavily doped n+ buffer layer. These layers are produced in epitaxial silicon. The main advantage of this structure is the ability to accurately control the resistivity and thickness of the n- layer to optimize the loss versus ruggedness trade-off. As a result devices using this structure often have the lowest losses on a per unit silicon area basis.

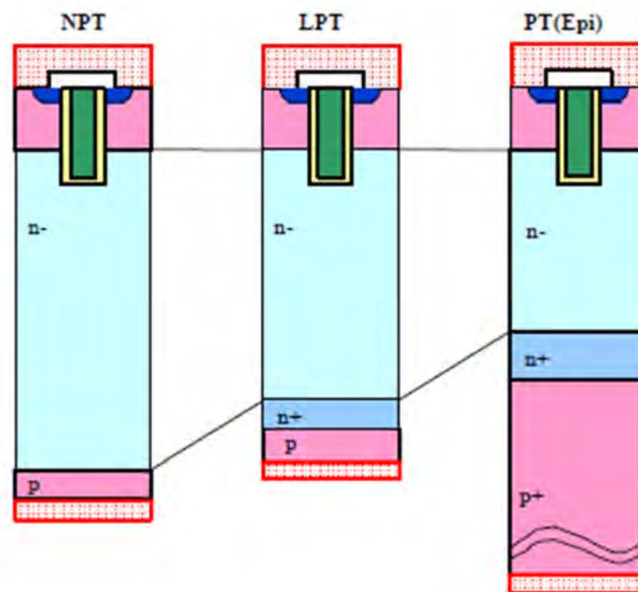


Figure 2.5.4 IGBT vertical Structure comparison

Unfortunately, there are two significant disadvantages of this structure. First, epitaxial silicon wafer material has a relatively high cost compared to the FZ (Float-Zone) wafer material that can be used with other structures. This is especially true for high voltage devices that require thicker epitaxial layers. Secondly, the long lifetime of carriers in the heavily doped n+ buffer layer must be modified to reduce turn-off losses. Typically this is done by electron irradiation or in some cases proton beam irradiation. This additional processing step adds cost and increases device to device characteristic variability. Another common vertical structure using less expensive FZ

wafer material is the conventional NPT (Non-Punch-Through) structure. The NPT device has an n- depletion layer with resistivity and thickness adjusted to block rated voltage. The lack of a buffer layer necessitates the use of a relatively thick high resistivity n- layer. The thick n- tends to provide good switching and short circuit ruggedness but higher V_{CE}(sat). In order to reduce V_{CE}(sat) it is necessary to make the n- layer thinner. This can be accomplished by thinning the silicon wafers. Special processing techniques have been developed to allow processing of optimally thin wafers. Unfortunately, as the n- thickness is optimized considering the blocking voltage versus V_{CE}(sat) trade-off of the device the lack of a buffer layer gives rise to excessive leakage current at elevated temperatures.

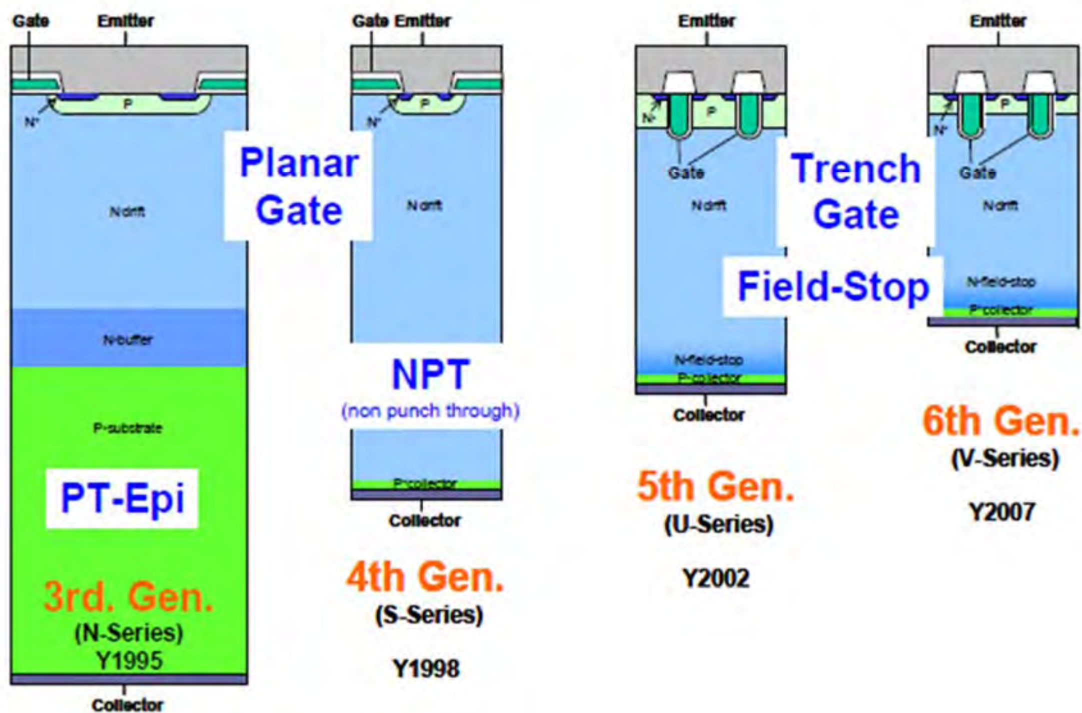


Figure 2.5.5 Transition of technologies applied to IGBT chips (1200volts)

Chapter 3

Literature Review analysis

3.1 Equation's Overview

3.1.1 Poisson's Equation

It relates variations in electrostatic potential to space charge densities

$$div(\varepsilon \nabla\psi) = -\rho$$

Where:

- ψ is the electrostatic potential
- ε is the local permittivity
- ρ is the local space charge density

The local space charge density is the sum of contributions from all mobile and fixed charges, including electrons, holes, and ionized impurities.

The electric field is obtained from the gradient of the potential:

$$E = -\nabla\psi$$

3.1.2 Carrier Continuity Equation

The continuity equations for electrons and holes are defined by:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial J_n(x)}{\partial x} - R_n + G_L$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\frac{\partial J_p(x)}{\partial x} - R_p + G_L$$

where,

- n and p are the electron and hole concentration
- J_N and J_P are the electron and hole current densities
- G_N and G_p are the generation rates for electrons and holes
- R_n and R_P are the recombination rates for electrons and holes
- q is the magnitude of electron charge.

It is sufficient in some cases solving only one carrier continuity equation.

3.2 Allen R. Hefner Model

3.2.1 Expression for Transient Voltage & Stored Charge Decay

In Hefner transient modeling approach, the general ambipolar transport electron current expression

$$I_n(W(t)) = \frac{I_T(t)}{1+\frac{1}{b}} + qAD\frac{\partial n(x,t)}{\partial x}$$

which was used to find an expression for the voltage rise (dV(t)/dt). $I_n(W(t))=I_{MOS}$ as shown in Fig. 2.4.1 and it is important since it controls the operation of IGBT. Since the reverse bias does not increase rapidly and the depletion capacitance is partially charged in a short period of time, I_{MOS} current is instantaneous. An expression for I_{MOS} can be obtained if we consider the collection-base junction depletion capacitance as in Fig. 3.2.1

For the voltage V(t) between the plates, the charge per unit area $q = \frac{\varepsilon_{Si} V(t)}{d}$, where d is the distance between the plates and the rate of q change is

$$\frac{dq}{dt} = I(current)$$

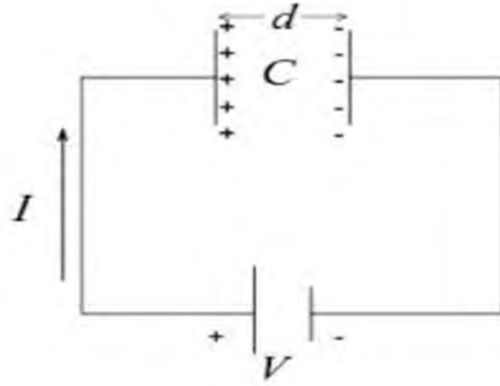


Figure 3.2.1 the collector base depletion capacitance formation

As we know $q(t) = C_{bcj}(t)V(t)$, so

$$\begin{aligned}\frac{dq}{dt} &= \frac{d}{dt}\left[C_{bcj}(t)V(t)\right]\\ &= V(t)\frac{dC_{bcj}(t)}{dt} + C_{bcj}(t)\frac{dV(t)}{dt}\end{aligned}$$

and in terms of the junction capacitance of the reverse biased junction, the displacement current $I_n(W(t))$ is

$$I_n(W) = V(t)\frac{dC_{bcj}(t)}{dt} + C_{bcj}(t)\frac{dV(t)}{dt} \quad (3.1)$$

The first term on the right hand side of the equation (3.1) was ignored by Hefner. The rate of change of $C_{bcj}(t)$ should be included in calculating the displacement current since the capacitance varies with time as the depletion width changes with voltage. From equation (2.6) and the fact that $J = I/A$, where A is the device active area

$$I_n(W(t)) = \frac{I_T(t)}{1+\frac{1}{b}} + qAD\frac{\partial p(x,t)}{\partial x}$$

And from Hefner's approach,

$$I_n(W(t)) = C_{bcj}(t)\frac{dV(t)}{dt} = \frac{I_T(t)}{1+\frac{1}{b}} + \frac{2qAD_p}{1+\frac{1}{b}}\frac{\partial p(x,t)}{\partial x}_{x=W(t)}$$
$$\Rightarrow \left(1+\frac{1}{b}\right)C_{bcj}(t)\frac{dV(t)}{dt} = I_T(t) + 2qAD_p\frac{\partial p(x,t)}{\partial x}_{x=W(t)} \quad (3.2)$$

Hefner used equation (3.2) to obtain V(t) for the transient operation of IGBT. He implemented the concept of moving the redistribution current. In his transient approach, he neither used the steady state expression for p(x) nor did he linearize the steady state expression for p(x). Moreover he assumed $C_{bcj}(t)$ to be constant with time, which is not so in reality.

His p(x) expression consists of two parts

$$p(x) = P_0\left[1-\frac{x}{W(t)}\right] - \frac{P_0}{W(t)D}\left[\frac{x^2}{2} - \frac{W(t)x}{6} - \frac{x^3}{3W(t)}\right]\frac{dW(t)}{dt} \quad (3.3)$$

From equation (2.6) & (3.3)

$$I_n(W(t)) = \frac{bI_T(t)}{1+b} + qAD\frac{\partial p(x)}{\partial x}_{x=W(t)}$$
$$\Rightarrow I_n(W(t)) = \frac{I_T(t)}{1+\frac{1}{b}} + \frac{2qAD_p}{1+\frac{1}{b}}\frac{\partial p(x)}{\partial x}_{x=W(t)} \quad (3.4)$$

and instead of equation (3.1), Hefner applied $I_n(W(t)) = C_{bcj}(t)\frac{dV(t)}{dt}$ in his approach. Integrating equation (3.3) in the base and multiplying by qA, the total charge Q

$$Q = qA\int_0^W p(x)dx$$
$$= qA\left[x - \frac{x^2}{2W(t)}\right] - \frac{P_0}{W(t)D}\left[\frac{x^3}{6} - \frac{W(t)x^2}{12} - \frac{x^4}{12W(t)}\right]\frac{dW(t)}{dt}\Bigg|_0^{W(t)}$$
$$= qA\left[P_0\left(W(t) - \frac{W(t)}{2}\right)\right] - \frac{P_0}{W(t)D}\left[\frac{W(t)^3}{6} - \frac{W(t)^3}{12} - \frac{W(t)^3}{12}\right]\frac{dW(t)}{dt}$$
$$= \frac{qAP_0W(t)}{2} - \frac{qAP_0}{WD}\times 0$$
$$Q = \frac{qAP_0W(t)}{2} \quad (3.5)$$

as can be seen $\frac{dW(t)}{dt}$ has no effect on Q calculation.

We can find $\frac{\partial p(x)}{\partial x}_{x=W(t)}$ from equation (3.3) as

$$\frac{\partial p(x)}{\partial x}_{x=W(t)} = \frac{P_0}{W(t)} - \frac{P_0}{W(t)D}\left[\frac{2x}{2} - \frac{W(t)}{6} - \frac{3x^2}{3W(t)}\right]\frac{dW(t)}{dt}_{x=W(t)}$$
$$\frac{\partial p(x)}{\partial x} = \frac{-P_0}{W(t)} - \frac{P_0}{W(t)D}\left[W(t) - \frac{W(t)}{6} - W(t)\right]\frac{dW(t)}{dt}$$
$$\frac{\partial p(x)}{\partial x} = \frac{-P_0}{W(t)} - \frac{P_0}{6D}\frac{dW(t)}{dt}$$

The hole current is $-qA\frac{\partial p(x)}{\partial x}$ and from the above equation

$$-qAD\frac{\partial p(x)}{\partial x} = \frac{qAP_0D}{W} - \frac{qAP_0D}{6D}\frac{dW(t)}{dt}$$
$$= \frac{qAP_0D}{W(t)} - \frac{qAP_0}{6}\frac{dW(t)}{dt}$$

As $Q = \frac{qAP_0W(t)}{2}$, So

$$-qAD\frac{\partial p(x)}{\partial x} = \frac{2QD}{W^2(t)} - \frac{Q}{3W(t)}\frac{dW(t)}{dt} \tag{3.6}$$

The first term on the right hand side of equation (3.6) is categorized by Hefner as the charge control component and the second term is categorized as the moving boundary redistribution component of the hole current.

From equations (3.4) & (3.6)

$$I_n(W(t)) = C\frac{dV(t)}{dt} = \frac{I_T(t)}{1+\frac{1}{b}} - \frac{4QD_p}{1+\frac{1}{b})\,W^2(t)} + \frac{Q}{3W(t)}\frac{dW(t)}{dt}$$

This equation can be expressed in a different way if $-qA\frac{\partial p(x)}{\partial x}$ in equation (3.6) is modified as

$$-qAD\frac{\partial p(x)}{\partial x} = \frac{-2qAD_p}{1+\frac{1}{b}}\frac{\partial p(x)}{\partial x} = \frac{2QD}{W^2(t)} - \frac{Q}{3W(t)}\frac{dW(t)}{dt}$$
$$\Rightarrow -2qAD_p\frac{\partial p(x)}{\partial x} = \frac{2QD}{W^2(t)}\left(1+\frac{1}{b}\right) - \frac{Q}{3W(t)}\left(1+\frac{1}{b}\right)\frac{dW(t)}{dt}$$
$$\Rightarrow -2qAD_p\frac{\partial p(x)}{\partial x} = \frac{4D_pD_nQ}{W^2(t)(D_p+D_n)}\left(1+\frac{1}{b}\right) - \frac{Q}{3W(t)}\left(1+\frac{1}{b}\right)\frac{dW(t)}{dt}$$
$$\Rightarrow -2qAD_p\frac{\partial p(x)}{\partial x} = \frac{4D_pQ}{W^2(t)} - \frac{Q}{3W(t)}\left(1+\frac{1}{b}\right)\frac{dW(t)}{dt} \tag{3.7}$$

From equation (3.4), we have

$$I_n(W(t)) = C\frac{dV(t)}{dt} = \frac{I_T(t)}{1+\frac{1}{b}} + \frac{2qAD_p}{1+\frac{1}{b}}\frac{\partial p(x,t)}{\partial x}_{x=W(t)}$$

That can be rearranged as

$$\left(1+\frac{1}{b}\right)C(t)\frac{dV(t)}{dt} = I_T(t) + 2qAD_p\frac{\partial p(x,t)}{\partial x}_{x=W(t)}$$

Now using equation (3.7), and the fact that $C(t) = C_{bcj}(t) = \frac{A\varepsilon_{Si}}{W_{bcj}(t)} = A\sqrt{\frac{2\varepsilon_{Si}N_B}{2V(t)}}$and $\frac{dW(t)}{dt} = \frac{-C}{qAN_B}\frac{dV(t)}{dt}$
the above equation yields

$$\left(1+\frac{1}{b}\right)C_{bcj}(t)\frac{dV(t)}{dt} = I_T(t) - \frac{4D_pQ(t)}{W^2(t)} + \frac{Q(t)}{3W(t)}\left(1+\frac{1}{ddb}\right)\frac{dW(t)}{dt}$$

$$\Rightarrow C_{bcj}(t)\frac{dV(t)}{dt}\left[1+\frac{Q(t)}{3qAW(t)N_B}\right] = \frac{I_T(t) - \frac{4D_pQ(t)}{W^2(t)}}{1+\frac{1}{b})}$$

$$\frac{dV(t)}{dt} = \frac{\left[I_T(t) - \frac{4D_pQ(t)}{W^2(t)}\right]}{C_{bcj}(t)\ \ 1+\frac{1}{b})\left[1+\frac{Q(t)}{3qAW(t)N_B}\right]} \qquad (3.8)$$

where $I_T(t)$=$I_T(0^-)$ for large inductive loads and$I_T(t) = \frac{4D_pQ(t)}{W^2(t)}$ for the constant anode voltage in which $\frac{dV(t)}{dt}$= 0 indicating that the voltage and W(t) are constants. Equation (3.8) is Hefner's transient$\frac{dV(t)}{dt}$ model for IGBT and Q(t) is expressed

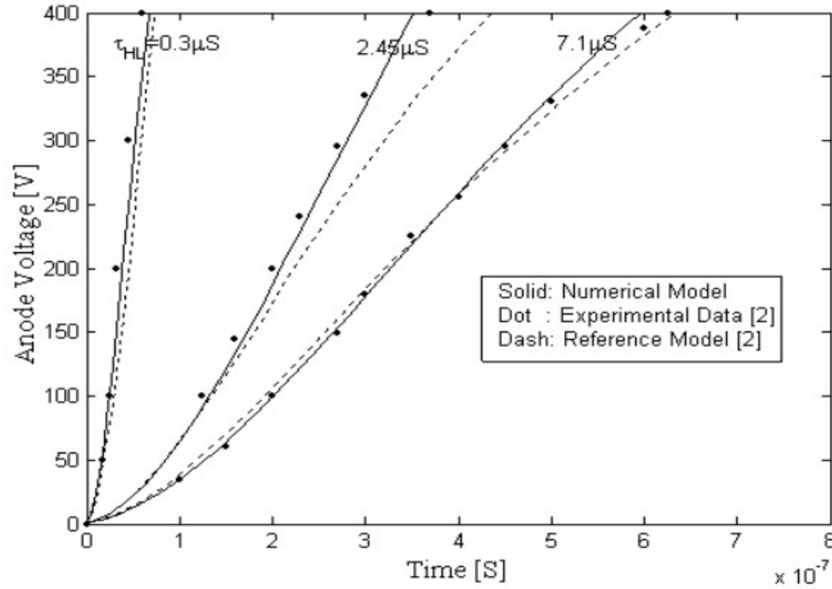


Figure 3.2.2 A comparison of the theoretical and measured 10A infinite inductive load switching voltage waveforms for devices with different base lifetimes

By solving the following non-linear Hefner differential equation

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau_{HL}} - \frac{4Q^2(t)I_{sne}}{W^2(t)A^2q^2{n_i}^2} \qquad (3.9)$$

where I_{sne} is emitter electron saturation current(A) and n_i is the intrinsic carrier concentration cm^{-3}.

In Hefner's approach, the negative of the collected hole current I_P ($W(t)$) consists of a charged control current (I_{CC}) and redistribution current (I_R), which make this model more complex. The expression (3.9) is not simple and Q_0 cannot be easily determined since there is no expression for P_0 which can be substituted for in Q_0 equation to evaluate Q_0 for magnitude. Also, this model did not consider the rate of change of C(t) in the calculation of the displacement current I_N ($W(t)$).

3.2.2 Redistribution time and Charge Control Current

Representative excess carrier distribution in the wide-base bipolar transient at various moments during a constant anode voltage turn-off transient are shown in Fig. 3.2.3

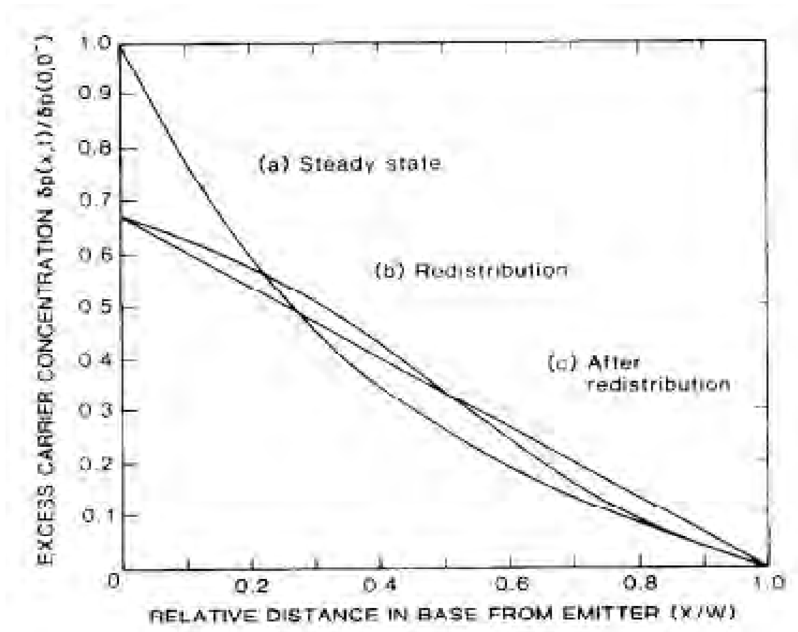


Figure 3.2.3 The Excess carrier distribution in the base before (a), during (b), and after (c) the redistribution phase of a constant anode voltage switching transient, for W/L=2.5 and for $I_n(x = 0) << I_p(x = 0)$. The effect of the decay of the total excess carrier has been left out to illustrate the re distribution process.

When the base current is removed (constant anode voltage case) or the anode clamp voltage is reached (inductive load case), the carrier distribution in the base changes rapidly to one for which the total current at the emitter is equal to the hole current at the collector (from distribution (a) to (b) in Fig. 3.2.3), so that quasi-neutrality is maintained in the bipolar base. This reduction in the total device current is responsible for the initial rapid fall in current observed in the switching transient current waveform. The initial rapid fall consists principally of the steady-state net electron current at the collector (base current for the constant anode voltage case) and the component of holes drift current associated with the net electron current there. The remaining slowly decaying excess majority carrier store is responsible for the slowly decaying portion of the switching transient current wave form.

The boundary conditions on the electron and hole currents are different between the steady-state condition and the slowly decaying current phase. As a result, the electrons & holes that recombine can no longer be supplied be the divergence of their current densities as they are in steady-state, but are only supplied by (and thus reduce)the local excess carrier concentration. The curvature in the carrier distributions and the corresponding divergence of the current densities that remains after the initial rapid fall in emitter current acts to redistribute the excess carriers in the base from distribution (b) & (c) in Fig. 3.2.3. After the redistribution is complete, the excess carrier distribution and the terminal current are given in terms of the total excess carrier charge in the base, so the remainder of the waveform can be described using a charge control model.

The redistribution time and the relation between the charge and current after the redistribution is complete are found from the time-dependent ambipolar diffusion equation with $I_n(W)$=0 and the total current equal to emitter edge of the base for negligible electron current at the injected into the emitter to the collector current gives:

$$\frac{\partial p(x,t)}{\partial t}\bigg|_{x=0} = \frac{\partial p(x,t)}{\partial t}\bigg|_{x=W} \quad (3.10)$$

The general solution to equation,

$$\frac{\partial^2 \delta p}{\partial x^2} = \frac{\delta p}{L^2} + \frac{1}{D}\frac{\partial \delta p}{\partial t}$$

with the conditions of

$$\delta p(x = 0, t = 0) \equiv P_{0,0} \quad (3.11) \qquad \delta p(W,t) = 0 \quad (3.12)$$

and equation (3.10) for W independent of time is

$$\delta p(x,t) = P_{0,0}\left(1 - \frac{x}{W}\right)e^{\left(-\frac{t}{\tau_{HL}}\right)} + \sum_{m=1}^{\infty} A_m \sin(2m\pi x)e^{\left(-\frac{t}{\tau_m}\right)} \quad (3.13)$$

(3.14)

Where $\frac{1}{\tau_m} = \frac{1}{\tau_{HL}} + \frac{(2m\pi)^2 D_p}{W^2}$ (3.15)

The first term of equation (3.13) is the linear charge control component of the distribution and the sine terms are the redistribution components which decay in time τ_m. For the base width W_B = 93 □ $10^{-6}m$ and other parameters, τ_m = $0.1/m^2us$. For times much larger than this, the redistribution terms become negligible and the current is determined by linear charge control component of the distribution.

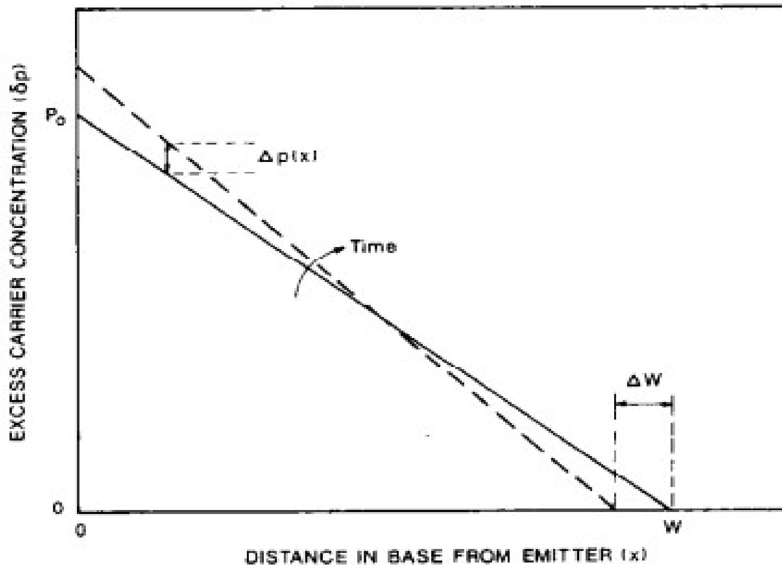


Figure 3.2.4 The carrier distribution in the base indicating the charge in excess carrier concentration with time due to the moving collector-base depletion edge boundary

The redistribution terms are independent of the total base charge and the integrated charge of the charge control term is equal to the total excess base charge:

$$Q(t) = \frac{qAP_{0,0}W}{2} e^{\left(-\frac{t}{\tau_{HL}}\right)} \quad (3.16)$$

Therefore, the current can only be described by a charge control model after the redistribution is complete. Using equations (3.13) & (3.15) for $I_n(W) = 0$, the charge control current is

$$I_T(t) = \frac{4D_p}{W^2} Q(t) \quad (3.17)$$

Because the integrated charge of each of the redistribution terms is zero, the value of current obtained by extrapolating the current decay waveforms back to the time of the initial rapid fall in current corresponds to the value of current obtained from equation (3.16) evaluated for the initial charge.

Chapter 4

Simulations

4.1 ATLAS A Physically-Based Simulator

In this thesis all the simulations involved are done with ATLAS from SILVACO which is a physically-based two and three dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation.

Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, onto this grid it is possible to simulate the transport of carriers through a structure. This means that the electrical performance of a device can now be modeled in DC, AC or transient modes of operation.

The major advantages of Physically-based simulation are it is predictive, it provides insight, and it captures theoretical knowledge in a simplified version.

Physically-based simulation is different from empirical modeling. The objective of empirical modeling is to obtain analytic formulae that approximate existing data with good accuracy and minimum complexity. Empirical models provide efficient approximation and interpolation. They do not provide insight, or predictive capabilities, or encapsulation of theoretical knowledge. Physically-based simulation is an alternative to experiments as a source of data.

Physically-based simulation has become very important for two reasons. Firstly, it is almost always much quicker and cheaper than performing experiments. Secondly, it provides information that is difficult or sometime impossible to measure. The drawbacks of simulation are that all the relevant physics must be incorporated into a simulator and numerical procedures must be implemented to solve the associated equations. These tasks have been taken care of for users of ATLAS.

Users of physically-based device simulation tools must specify the problem to be simulated. Users of ATLAS specify device simulation problems by defining:

1. The physical structure to be simulated

2. The physical models to be used

3. The bias conditions for which electrical characteristics are to be simulated.

ATLAS here is used in conjunction with the VWF INTERACTIVE TOOLS. These include DECKBUILD, TONYPLOT, DEVEDIT, ATHENA and many more. DECKBUILD provides an interactive run-time environment. TONYPLOT supplies scientific visualization capabilities. DEVEDIT is an interactive tool for structure and mesh specification and refinement while ATHENA servers for semiconductor process simulation.

The interaction overview of SILVACO: ATLAS with other tools is shown in Fig. 4.1.1

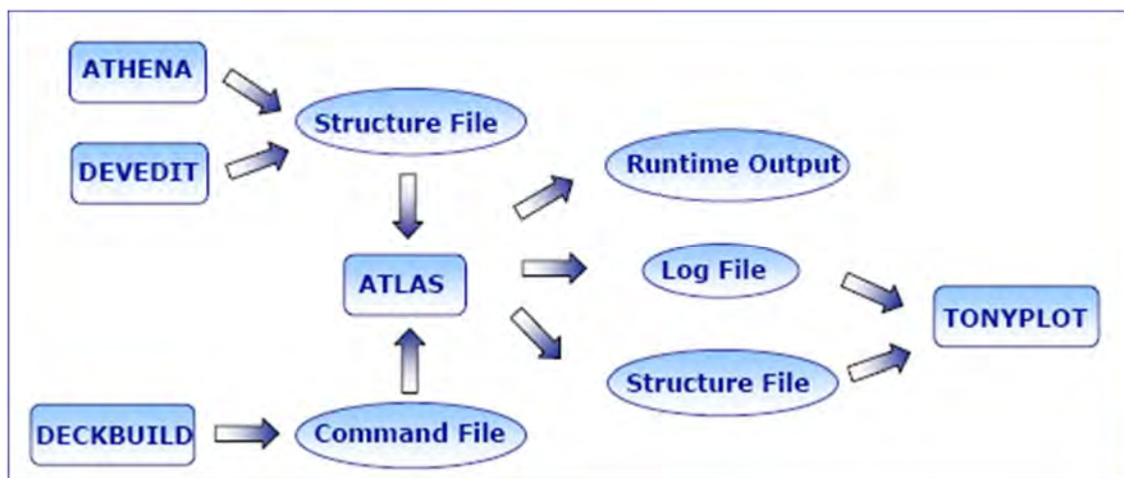


Figure 4.1.1 Interaction with ATLAS software

We use the DECKBUILD command file input for the ATLAS environment to build our Trench IGBT and utilize all the outputs as well as TONYPLOT to conclude and visualize the simulated results.

Atlas input file contains a sequence of command lines and each line consists of a keyword or statement that identifies the command and a set of parameters.

In ATLAS there are four groups of statements that must occur in the correct order mentioned in Fig. 4.1.2

Group	Statements
1. Structure Specification	MESH
	ELECTRODE
	CONTACT
2. Models specification	MODELS
3. Numerical Method Selection	METHOD
4. Solution Specification	LOG
	SOLVE
	LOAD
	SAVE

Figure 4.1.2 Elements of ATLAS input deck in correct order

Each statement consists of a keyword that identifies the statement and a set of parameters. The general format is:

<STATEMENT> <PARAMETER>=<VALUE> <PARAMETER>=<VALUE>

An example of a statement line is:

DOPING uniform n.type concentration=1.0e16 region=1 outfile=my.dop

The statement is DOPING. All other items are parameters of the DOPING statement. UNIFORM and N.TYPE are logical parameters. Their presence on the line sets their values to true. Otherwise, they take their default values. CONCENTRATION is a Real parameter and takes floating point numbers as input values. REGION is an Integer parameter taking only integer numbers as input. OUTFILE is a Character parameter type taking strings as input. The

statement keyword must come first but the order of parameters within a statement is unimportant.

4.2 Punch Through IGBT with Trench gate device structure

4.2.1 Mesh Structure of the Trench IGBT

In ATLAS the first parameter to be defined is the mesh for the entire device structure. Mesh grid parameter could give effects to the simulation process. As an example, doping process depends on the y-axis grid location and spacing. In Silvaco TCad, mesh grid is also known as the simulation grid. The correct specification of grid is critical in process simulation and the number of nodes in the grid has a direct influence on simulation accuracy and time. A finer grid should exist in those areas of the simulation structure where ion implantation will occur, where p-n junction will formed or where optical illumination will change photoactive concentration. Usually the finest grid will defined at the surface of the substrate. This region will be used to form the surface active region of the NMOS transistor. The mesh structure of our device is shown in Fig. 4.2.1

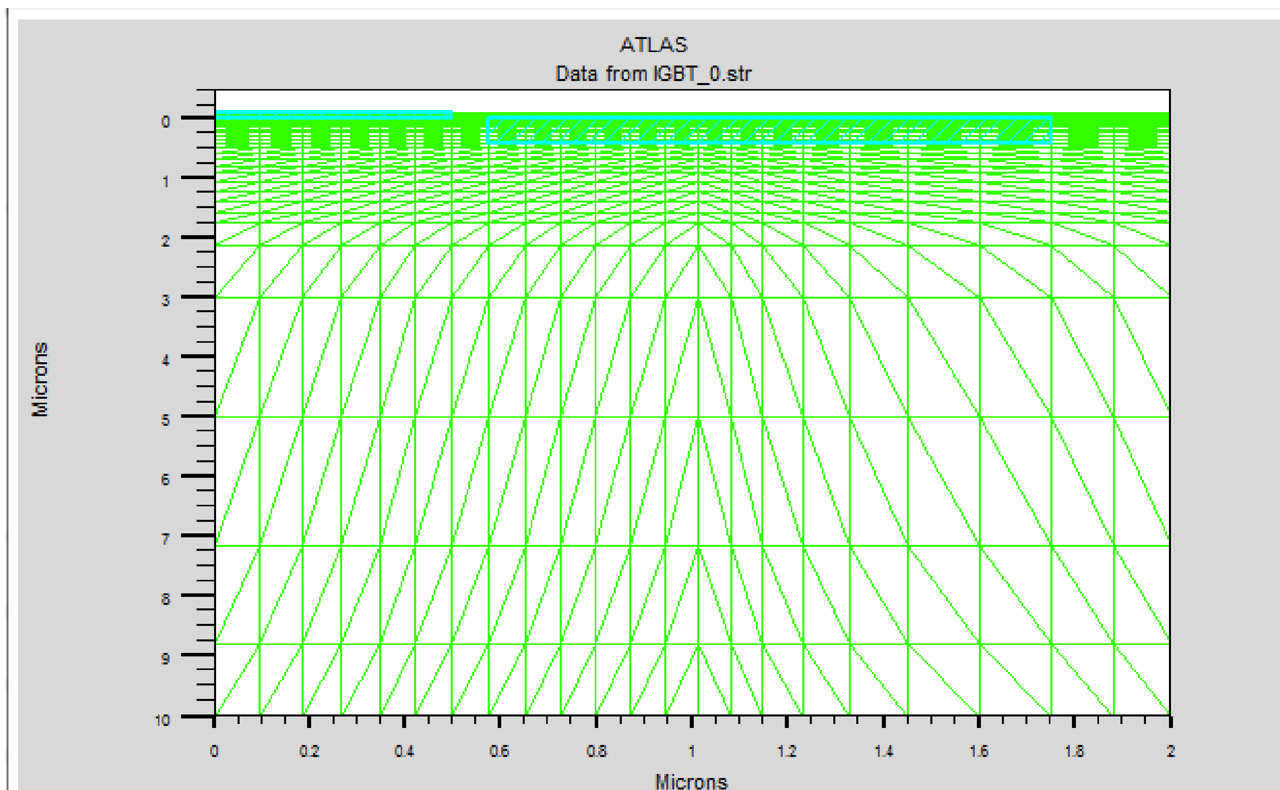


Figure 4.2.1 Mesh of Trench IGBT

4.2.2 Region and Doping formation

After defining the mesh structure the region of the device is being formed. In this part the silicon, SiO2 and p-n junction are being created. Firstly the gate, emitter and collector region are defined. Then the whole substrate is doped with n.type substrate. At this stage the structure has formed as follows in Fig.4.2.2

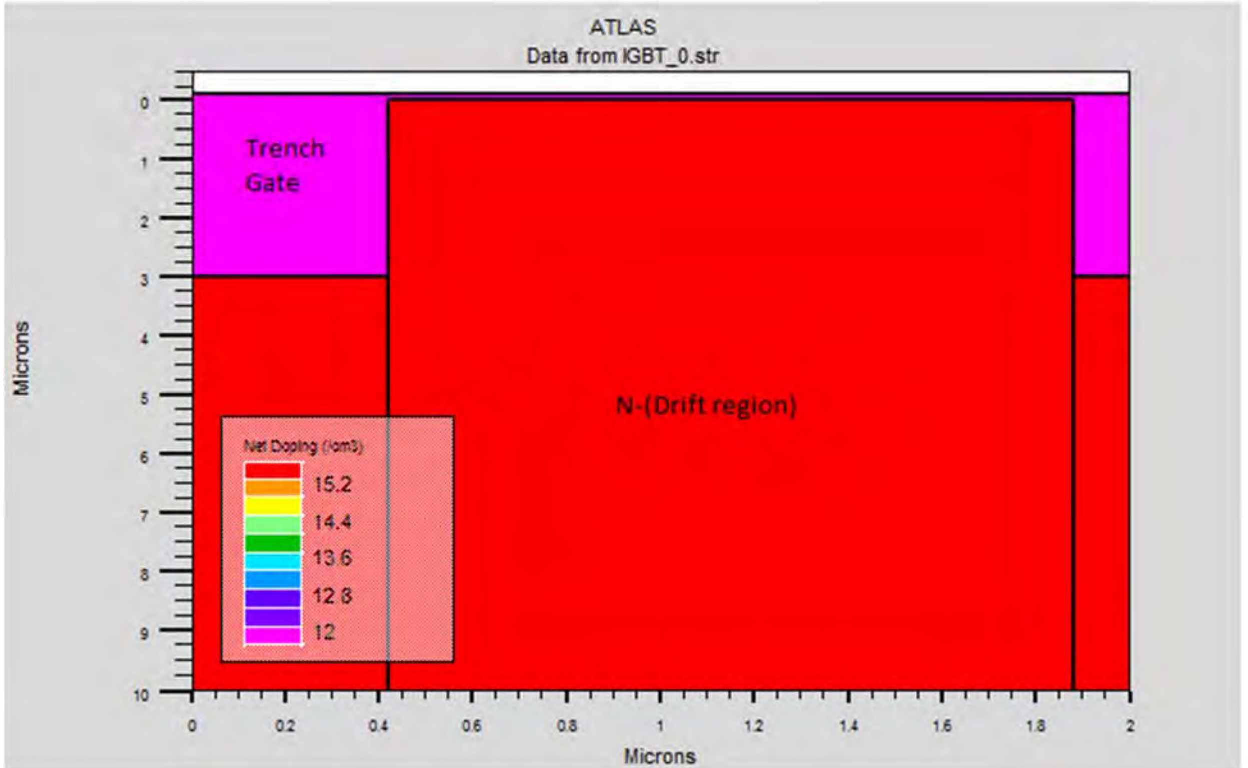


Figure 4.2.2 N-(Drift region) with Trench gate

Here our device in modeled with 2um in length and 10um of depth. The length of the trench gate is used 0.4um and depth is 3um. In the further process of our thesis we have simulated the device with different length and depth to observe the change in output characteristics.

In the emitter region we have used p+, n+ and p- region with proper doping level to acquire desired characteristics. In Fig.4.2.3 the structure formation shows the corresponding emitter region.

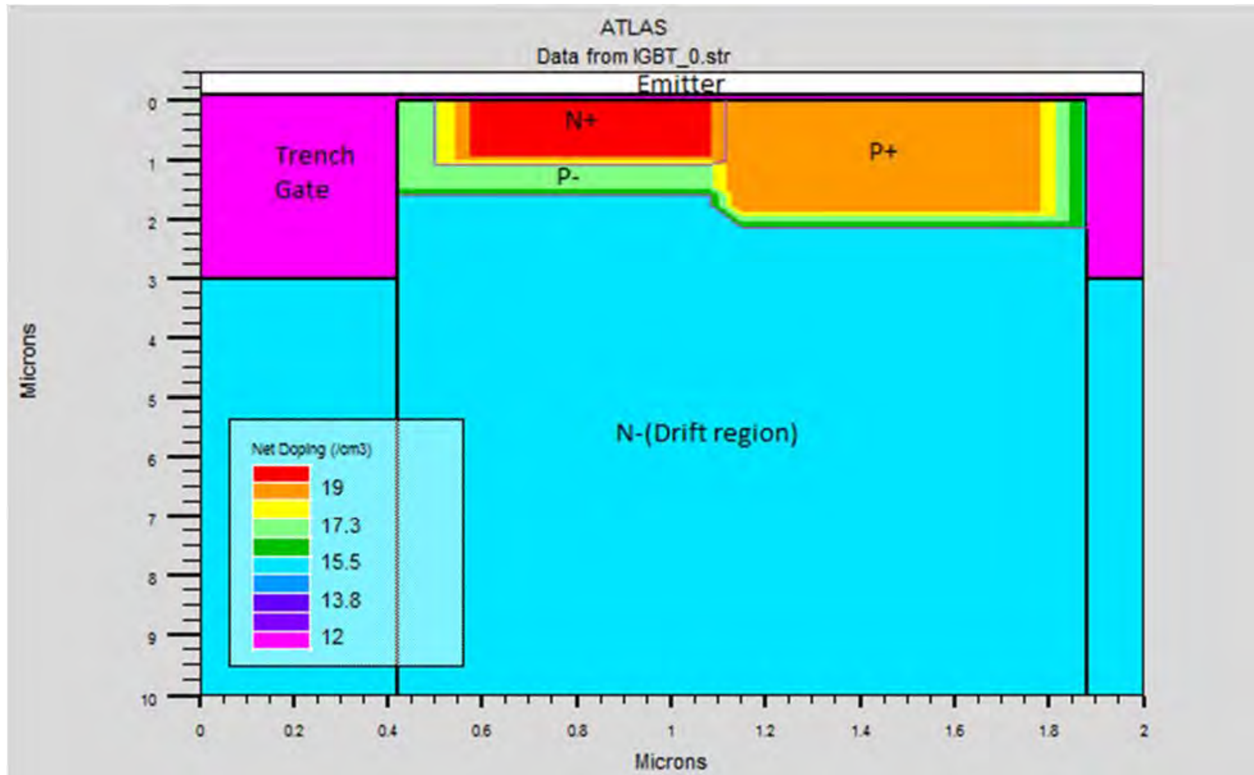


Figure 4.2.3 Emitter Region

In emitter region the length of p+, n+ and p- are respectively 0.72um, 0.6um and 0.7um with depth 2um, 1um and 1um-0.5um. Considering the hole and electron mobility of Power MOSFET we have determined and formed the emitter region for our trench IGBT to obtain higher collector current with minimum threshold voltage.

After forming the emitter region with n- substrate the p+, n+ and p- region formed. Here in order to control the hole injection we have induced an extra layer of p- in between the buffer region and collector region. This extra layer was formed to investigate the punch through operation of the trench IGBT and improve the threshold voltage and output characteristics.

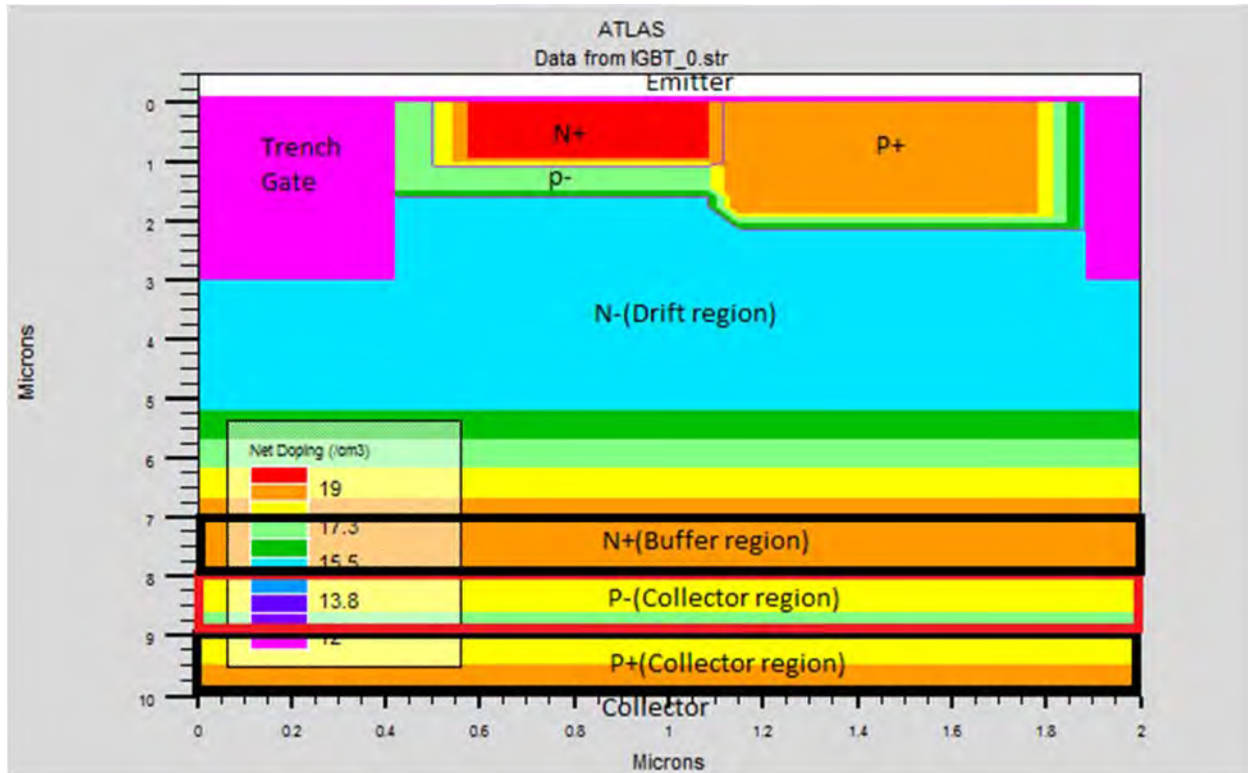


Figure 4.2.4 Trench IGBT designed full model

In Fig.4.2.4 illustrates the full designed trench IGBT device structure. We have formatted the buffer region with n.type doping which has a length of 2um and depth of 1um which was best suited for our desired transfer characteristics. Following P- and P+ regions also shares the same length and depth attributes as shown in Fig.4.2.4. These regions are created in such a way that the P+ collector region and N+ buffer region have a middle region in between them as P+ for controlled increase in hole concentration in a punch through operation conducted in a trench type IGBT.

4.2.3 Device simulation

4.2.3.1 1st simulation

After the completion of the whole device we have simulated under different doping concentration, length and depth of different region in order to study and analyze the difference response and transfer characteristics. Firstly we run the simulation with the following parameters set through study of previous research and publications with collector voltage (Vce) up to 30V.

	Length(um)	Depth(um)	Concentration
P+(Emitter)	0.72	2.0	1.0e19
P-(Emitter)	0.7	0.5-1.5	1.0e15
N+(Emitter)	0.6	1.0	1.0e19
N-(Drift region)	2.0	5.1-4.1	1.5e15
P+(Collector)	2.0	1.0	1.0e19
P-(Extra layer)	2.0	1.0	1.0e17
N+(Buffer region)	2.0	1.0	1.0e19
Trench Gate	0.4	3.0	-

Table 4.2.1 Set parameters for 1st simulation

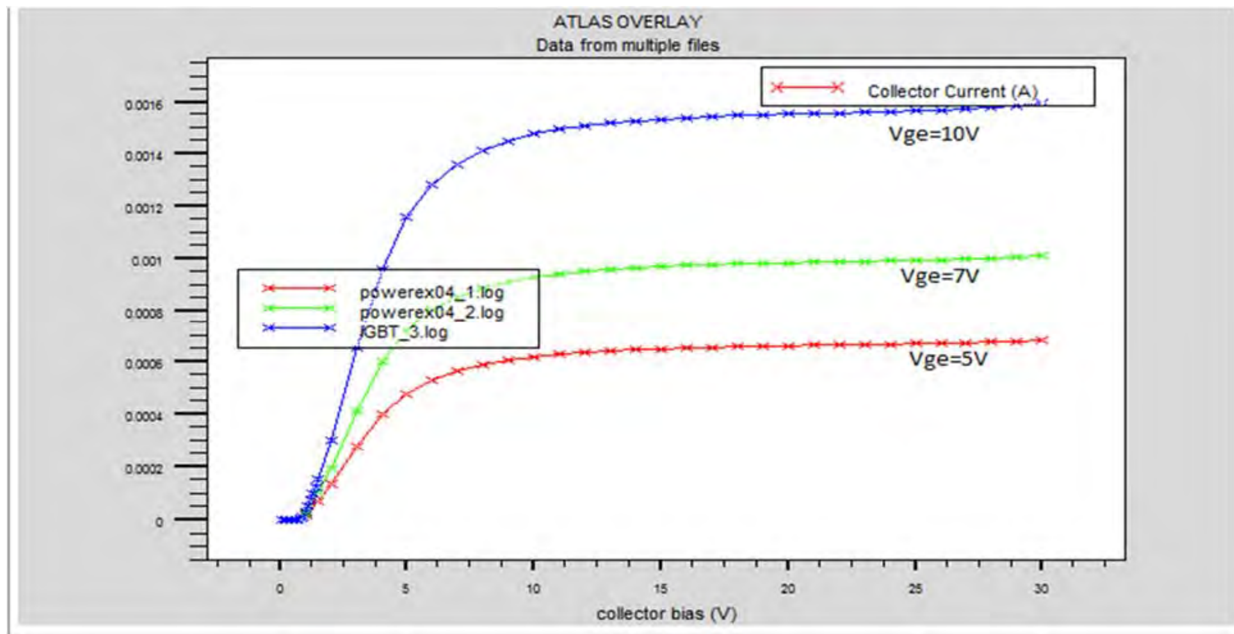


Figure 4.2.5 Output of 1st simulation

We obtain the following output from the 1st simulation of our designed device and set parameters.

Gate voltage(Vge)	Collector Current(Ic)(Approximate)
10V	0.0016A
7V	0.0011A
5V	0.00061A

Table 4.2.2 Ic vs Vce 1st simulation output

In the 1st simulation we observe that the collector current Ic is rising following the rise of gate voltage Vge. In this output of our designed Trench IGBT we were able to obtain greater Ic for corresponding Vge compared to conventional punch through IGBT letter in our research.

We indicated the saturation, active and cut off region in Fig.4.2.6 of the obtained output.

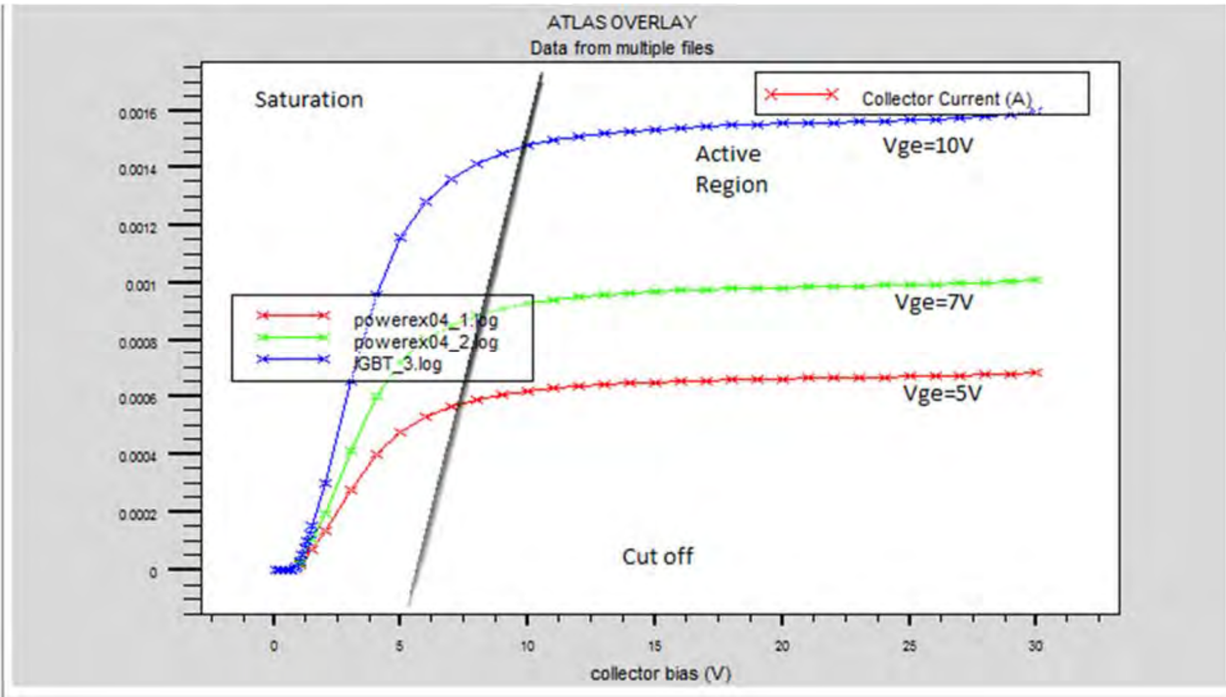


Figure 4.2.6 Saturation, active and cutoff region of Trench IGBT with hole injection layer (P-)

4.2.3.2 2nd simulation

For further study we changed the doping of different layers and length and depth of different regions one by one which helped us to analyze and determine the effect of different regions on the output of the designed trench IGBT.

	Length(um)	Depth(um)	Concentration
P+(Emitter)	0.72	2.0	1.0e19
P-(Emitter)	0.7	0.5-1.5	1.0e15
N+(Emitter)	0.6	1.0	1.0e19
N-(Drift region)	2.0	5.1-4.1	1.5e15
P+(Collector)	2.0	1.0	1.0e19
P-(Extra layer)	2.0	1.0	1.0e17
N+(Buffer region)	2.0	1.0	1.0e19
Trench Gate	0.4	1.5/2.0	-

Table 4.2.3 Set parameters for 2nd simulation

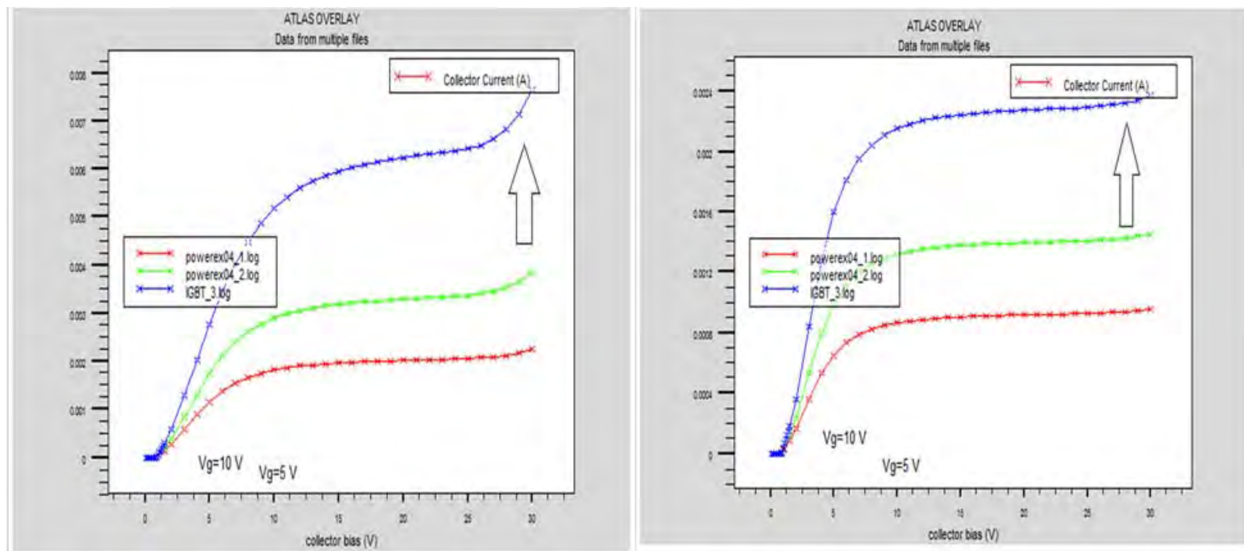


Figure 4.2.7 Output of 2nd simulation

In our second simulation we have varied the gate depth to 1.5um and 2.0um from 3.0um. We can see from the output curves that as the gate depth decreases the collector current increases but the stability of the total model has decreased and so the system may enter the breakdown region if we continue to decrease the gate depth within the same length of 0.4um.

Obtained values from 2nd simulation as follows-

Gate voltage(Vge)	Collector Current(Ic) (Approximate) Gate depth 1.5um	Collector Current(Ic) (Approximate) Gate depth 2.0um
10V	0.006A	0.0024A
7V	0.003A	0.0014A
5V	0.002A	0.0009A

Table 4.2.4 Ic vs Vce 2nd simulation output

From the obtained value we can say that, the collector current has increased at 2um depth but as we decrease it more than that, the collector current began to fall with less stable characteristics.

4.2.3.3 3rd simulation

Selected parameter shown in Table.4.2.5

	Length(um)	**Depth(um)**	**Concentration**
P+(Emitter)	**0.72**	**2.0**	**1.0e19**
P-(Emitter)	**0.7**	**0.5-1.5**	**1.0e15**
N+(Emitter)	**0.6**	**1.0**	**1.0e20/2.5e19**
N-(Drift region)	**2.0**	**5.1-4.1**	**1.5e15**
P+(Collector)	**2.0**	**1.0**	**1.0e19**
P-(Extra layer)	**2.0**	**1.0**	**1.0e17**
N+(Buffer region)	**2.0**	**1.0**	**1.0e19**
Trench Gate	**0.4**	**3.0**	**-**

Table 4.2.5 Set parameters for 3rd simulation

In the third simulation we varied the doping of n.type property of emitter region. We increased the doping to 1.0e20 and 2.5e19 from 1.0e19 and observed the changes respectively.

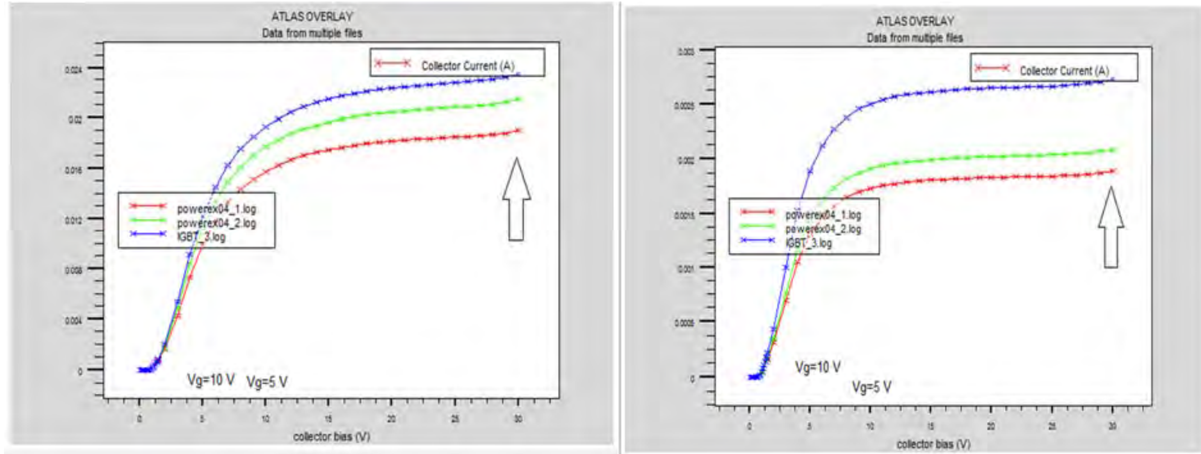


Figure 4.2.8 Output of 3rd simulation

From Fig.4.2.7 we can observe that the collector current is increasing due to the increased doping of n+ emitter region. It shows that the system may become independent from the gate voltage regarding the collector current if the doping in increased more.

Gate voltage(Vge)	Collector Current(Ic) (Approximate) n+emitter(1.0e20)	Collector Current(Ic) (Approximate) n+emitter(2.5e19)
10V	0.023A	0.0027A
7V	0.02A	0.002A
5V	0.018A	0.0017A

Table 4.2.6 Ic vs Vce 3rd simulation output

4.2.3.4 4th simulation

Selected parameters shown in Table.4.2.7

	Length(um)	Depth(um)	Concentration
P+(Emitter)	**0.72**	**2.0**	**1.0e19**
P-(Emitter)	**0.7**	**0.5-1.5**	**1.0e15**
N+(Emitter)	**0.6**	**1.3**	**1.0e19**
N-(Drift region)	**2.0**	**5.1-4.1**	**1.5e15**
P+(Collector)	**2.0**	**1.0**	**1.0e19**
P-(Extra layer)	**2.0**	**1.0**	**1.0e17**
N+(Buffer region)	**2.0**	**1.0**	**1.0e19**
Trench Gate	**0.4**	**3.0**	**-**

Table 4.2.7 Set parameters for 4th simulation

In the 4th simulation we changed the depth of n+ emitter region to 1.3um from 1.0um. as we induce the n+ more into the drift region the electron mobility may vary and effect the collector current.

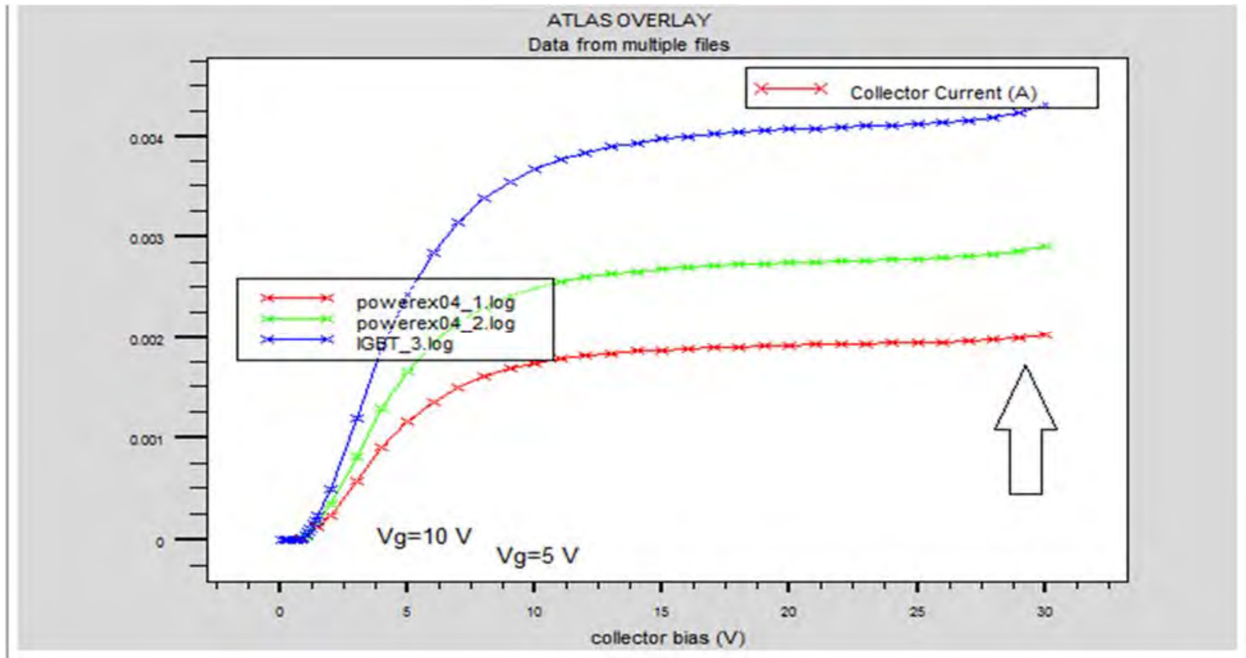


Figure 4.2.9 Output of 4th simulation

From Fig.4.2.9 we can see that the collector current is increasing due to the changed depth of n+ region. Despite of this fact the system does not illustrate any smooth output characteristics if we increase or decrease the depth more.

Gate voltage(Vge)	Collector Current(Ic)(Approximate)
10V	0.004A
7V	0.0028A
5V	0.0019A

Table 4.2.8 Ic vs Vce 4th simulation output

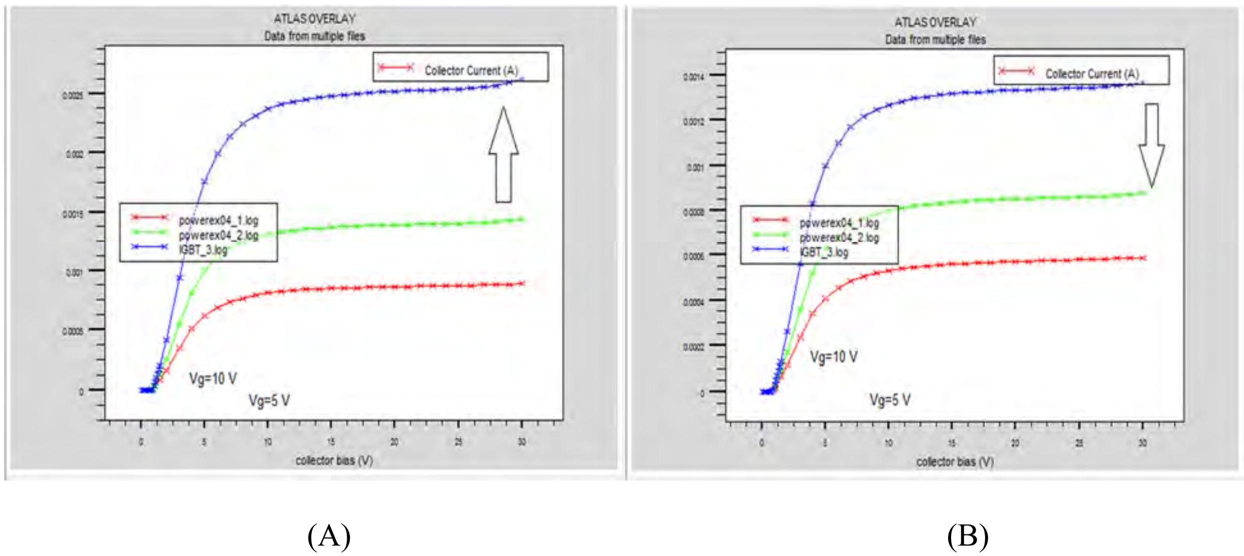
4.2.3.5 5th simulation

Set parameters are as follows

	Length(um)	Depth(um)	Concentration
P+(Emitter)	**0.72**	**2.0**	**1.0e18/1.0e21**
P-(Emitter)	**0.7**	**0.5-1.5**	**1.0e15**
N+(Emitter)	**0.6**	**1.0**	**1.0e19**
N-(Drift region)	**2.0**	**5.1-4.1**	**1.5e15**
P+(Collector)	**2.0**	**1.0**	**1.0e19**
P-(Extra layer)	**2.0**	**1.0**	**1.0e17**
N+(Buffer region)	**2.0**	**1.0**	**1.0e19**
Trench Gate	**0.4**	**3.0**	**-**

Table 4.2.9 Set parameters for 5th simulation

In this simulation we varied the doping of P+ emitter region.



(A) (B)

Figure 4.2.10 Output of 5th simulation

In Fig.4.2.10 (A) we have decreased the P+ doping to 1.0e18 which is affecting the collector current to increase from our standard model and on the other hand in Fig.4.2.10 (B) the current is decreasing as the doping has been increased to 1.0e21. Therefore, we can state that the P+ region doping is significantly affecting our transfer curve.

Gate voltage(Vge)	Collector Current(Ic) (Approximate) p+emitter(1.0e18)	Collector Current(Ic) (Approximate) p+emitter(1.0e21)
10V	0.0025A	0.0014A
7V	0.0014A	0.0009A
5V	0.0009A	0.0005A

Table 4.2.10 Ic vs Vce 5th simulation output

4.2.3.6 6th simulation

Set parameters are as follows for 6th simulation

	Length(um)	**Depth(um)**	**Concentration**
P+(Emitter)	**0.72**	**1.6/3.0**	**1.0e19**
P-(Emitter)	**0.7**	**0.5-1.5**	**1.0e15**
N+(Emitter)	**0.6**	**1.0**	**1.0e19**
N-(Drift region)	**2.0**	**5.1-4.1**	**1.5e15**
P+(Collector)	**2.0**	**1.0**	**1.0e19**
P-(Extra layer)	**2.0**	**1.0**	**1.0e17**
N+(Buffer region)	**2.0**	**1.0**	**1.0e19**
Trench Gate	**0.4**	**3.0**	**-**

Table 4.2.11 Set parameters for 6th simulation

The depth of P+ emitter region have significant role in electron-hole mobility in power transistor device according to conventional P-N junction characteristics. For that, we changed the depth accordingly to study the effect in trench IGBT.

Fig.4.2.11 will illustrate the changes that occurred due to P+ emitter region for 1.6um and 3.0um respectively.

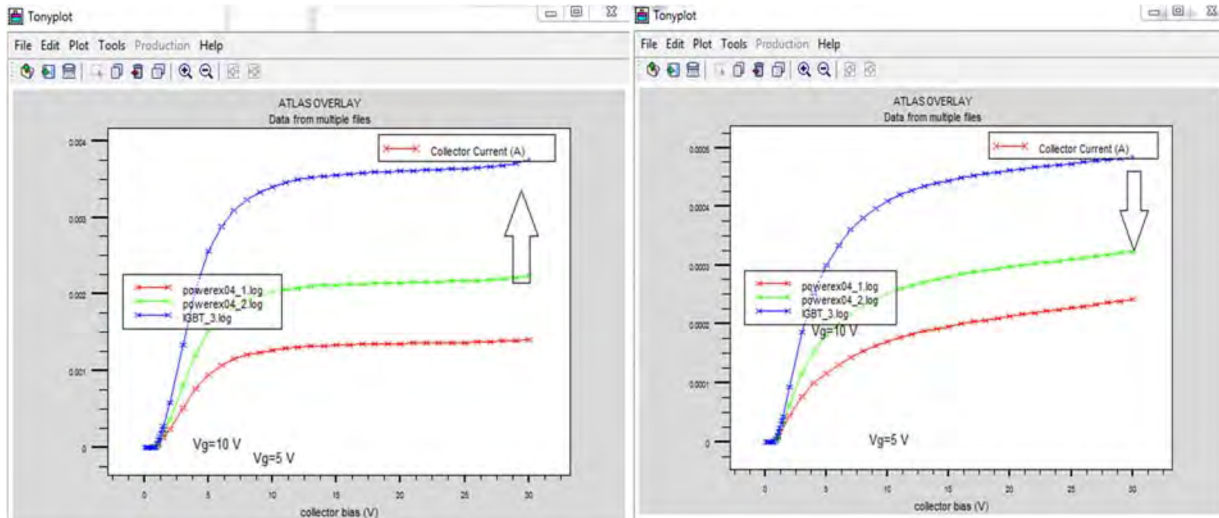


Figure 4.2.11 Output of 6th simulation

Gate voltage(Vge)	Collector Current(Ic) (Approximate) p+emitter(1.6um)	Collector Current(Ic) (Approximate) p+emitter(3.0um)
10V	0.0035A	0.0005A
7V	0.0021A	0.0003A
5V	0.0013A	0.00021A

Table 4.2.12 Ic vs Vce 6th simulation output

For the 1st part where we have formed the p+ emitter length as 1.6um, the values clearly states that the resistance due to the depletion region is much lower here as a result the electron-hole mobility has increased as well as collector current.om contrary, for increased depth of 3um the collector current has decreased significantly due to higher resistance.

4.2.3.7 7th simulation

Set parameters for next simulation are illustrated in Table.4.2.13

	Length(um)	Depth(um)	Concentration
P+(Emitter)	**0.72**	**2.0**	**1.0e19**
P-(Emitter)	**0.7**	**0.5-1.5**	**1.0e17**
N+(Emitter)	**0.6**	**1.0**	**1.0e19**
N-(Drift region)	**2.0**	**5.1-4.1**	**1.5e15**
P+(Collector)	**2.0**	**1.0**	**1.0e19**
P-(Extra layer)	**2.0**	**1.0**	**1.0e17**
N+(Buffer region)	**2.0**	**1.0**	**1.0e19**
Trench Gate	**0.4**	**3.0**	**-**

Table 4.2.13 Set parameters for 7th simulation

Here we have varied the P- emitter doping from 1.0e15 to 1.0e17 in order to observe the changes in electron-hole mobility. The PNP junction here can affect the transfer characteristics significantly. As we proceed with our simulation we have obtained the following result in Fig.4.2.12.

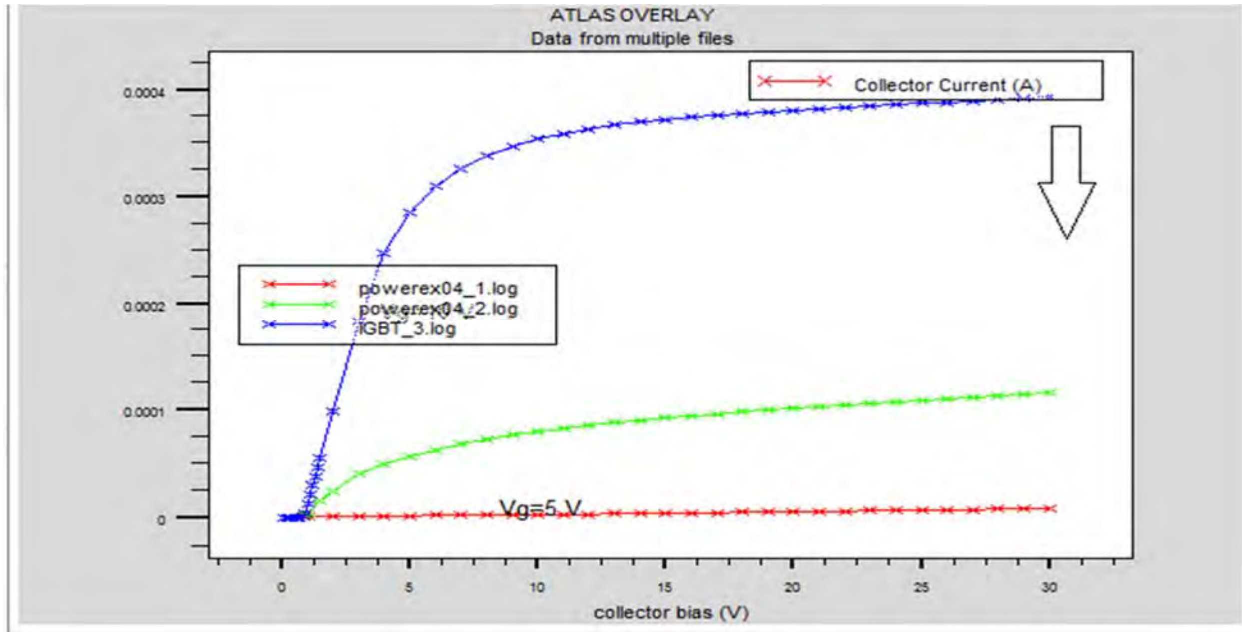


Figure 4.2.12 Output of 7th simulation

Obtained Ic vs Vce values due to different Vge are show in Table.4.2.14

Gate voltage(Vge)	Collector Current(Ic)(Approximate)
10V	0.0004A
7V	0.0001A
5V	5.0e-6A

Table 4.2.14 Ic vs Vce 7th simulation output

From Table.4.2.14 it is clarified that the electron-hole mobility has been decreased here as a result the collector current has greatly decreased than the output we have obtained earlier. Moreover increasing the doping of P- emitter region does not affect the output much and may consequently raise the depletion region resistance.

4.2.3.8 8th simulation

Set parameters for 8th simulation.

	Length(um)	Depth(um)	Concentration
P+(Emitter)	**0.72**	**2.0**	**1.0e19**
P-(Emitter)	**0.7**	**0.5-1.5**	**1.0e15**
N+(Emitter)	**0.6**	**1.0**	**1.0e19**
N-(Drift region)	**2.0**	**5.1-4.1**	**1.5e16/1.5e12**
P+(Collector)	**2.0**	**1.0**	**1.0e19**
P-(Extra layer)	**2.0**	**1.0**	**1.0e17**
N+(Buffer region)	**2.0**	**1.0**	**1.0e19**
Trench Gate	**0.4**	**3.0**	**-**

Table 4.2.15 Set parameters for 8th simulation

Considering the drift region of the substrate we fixated the depth under trench region to 4.1um and under the emitter region to 4.1um in order to keep the resistance of the device to minimum and maintain a controlled punch through operation with sufficient electron-hole mobility throughout emitter to collector junction. In this iteration we have just changed the doping of n-(Drift region) to observe the changes in the transfer characteristic

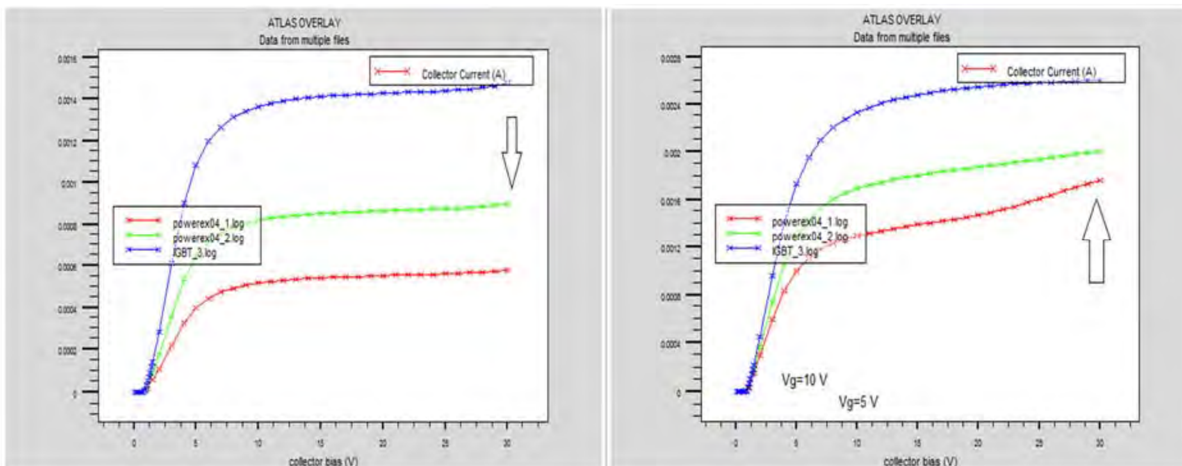


Figure 4.2.13 Output of 8th simulation

Obtained values from the transfer curve are as follows Table.4.2.16

Gate voltage(Vge)	Collector Current(Ic) (Approximate) n-Drift(1.5e12)	Collector Current(Ic) (Approximate) n-Drift(1.5e16)
10V	0.0014A	0.0026A
7V	0.0008A	0.0019A
5V	0.0005A	0.00015A

Table 4.2.16 Ic vs Vce 8th simulation output

The changes illustrates that, with decreasing concentration the collector has decreased and the effect of increased concentration has helped to improve the collector current as well as the transfer curve. We have also studied the output for higher concentrated drift region but in result we have found that the collector current becomes independent of the gate voltage.

4.2.3.9 9th simulation

Following parameters are under consideration for our next simulation.

	Length(um)	**Depth(um)**	**Concentration**
P+(Emitter)	**0.72**	**2.0**	**1.0e19**
P-(Emitter)	**0.7**	**0.5-1.5**	**1.0e15**
N+(Emitter)	**0.6**	**1.0**	**1.0e19**
N-(Drift region)	**2.0**	**5.1-4.1**	**1.5e15**
P+(Collector)	**2.0**	**1.0**	**1.0e19**
P-(Extra layer)	**2.0**	**1.0**	**1.0e17**
N+(Buffer region)	**2.0**	**1.0/3.0**	**2.5e19/1.0e19**
Trench Gate	**0.4**	**3.0**	**-**

Table 4.2.17 Set parameters for 9th simulation

In this simulation we have simulated the trench IGBT with changes to the concentration and depth of n+ buffer layer. We have observed the output characteristics with depth 1.0 and concentration of 2.5e19, depth 3.0 and concentration of 1.0e19 respective combinations**.**

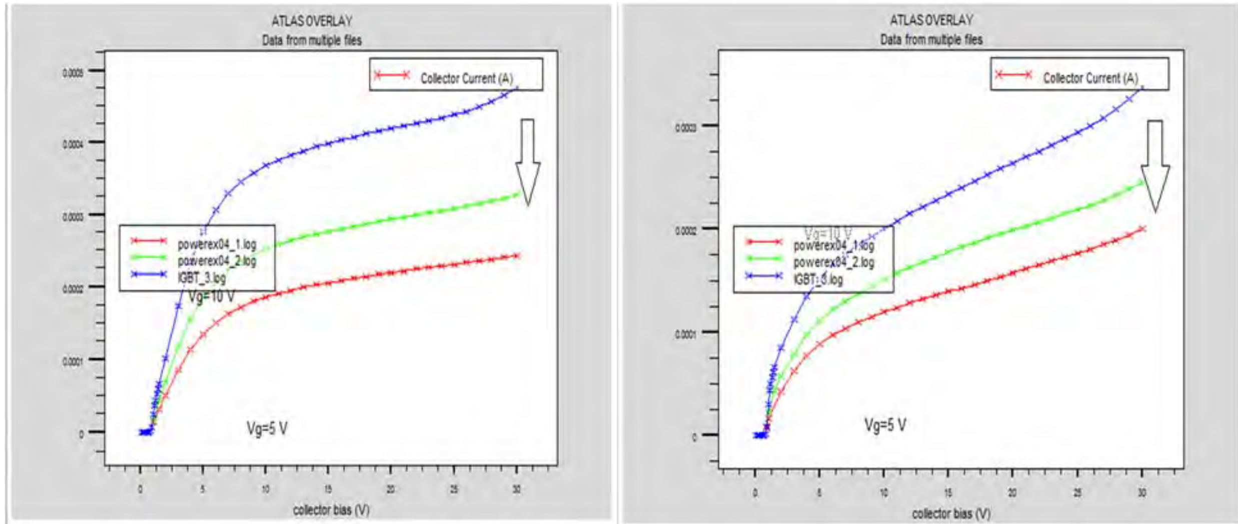


Figure 4.2.14 Output of 9th simulation

In both cases the collector current has decreased from our specified model. The values we obtained from the transfer curve are shown in Table.4.2.18

Gate voltage(Vge)	Collector Current(Ic)(Approximate) n+buffer(1.0um-2.5e19)	Collector Current(Ic) (Approximate) n+buffer(3.0um-1.0e19)
10V	0.00045A	0.0003A
7V	0.0003A	0.0002A
5V	0.0002A	0.00015A

Table 4.2.18 Ic vs Vce 9th simulation output

Due to the changes in buffer region the electron-hole mobility has decreased as a result the increasing resistance has caused the collector current to decrease which was not desired.

4.2.3.10 10th simulation

We have set the parameters for our next simulation as follows Table.4.2.19

	Length(um)	Depth(um)	Concentration
P+(Emitter)	0.72	2.0	1.0e19
P-(Emitter)	0.7	0.5-1.5	1.0e15
N+(Emitter)	0.6	1.0	1.0e19
N-(Drift region)	2.0	5.1-4.1	1.5e15
P+(Collector)	2.0	1.0	1.0e19
P-(Extra layer)	2.0	1.0	1.0e14/2.5e17
N+(Buffer region)	2.0	1.0	1.0e19
Trench Gate	0.4	3.0	-

Table 4.2.19 Set parameters for 10th simulation

As we mentioned earlier we have introduced a new layer of p- in between n+ drift region and p+ collector region. This layer is induced to increase the hole injection in drift region which may increase the electron-hole mobility as well as to create p-n junction with lower resistive depletion layer. We have changed the doping of this p- layer in our current simulation to observe the effect and come to solution in favor to our experimentation.

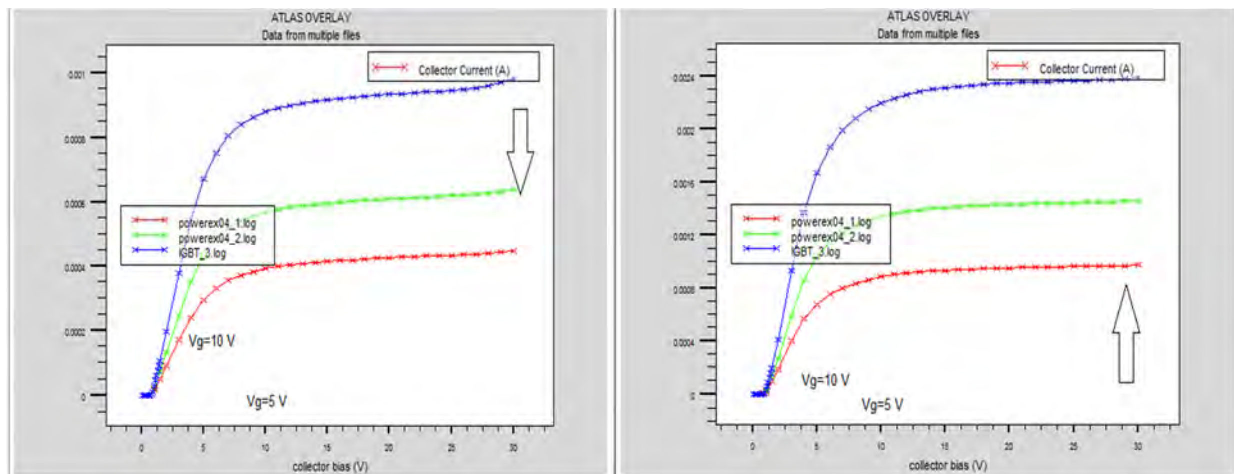


Figure 4.2.15 Output of 10th simulation

Gate voltage(Vge)	Collector Current(Ic)(Approximate) p-extra layer(1.0e14)	Collector Current(Ic) (Approximate) p-extra layer(2.5e17)
10V	0.0009A	0.0024A
7V	0.0006A	0.0014A
5V	0.0004A	0.0009A

Table 4.2.20 Ic vs Vce 10th simulation output

From the transfer curve and obtained values we can state that the concentration is effectively bringing changes to the output characteristics. As the concentration was decreased to 1.0e14 the collector current has decreased significantly. On the other hand the increased conduction has brought change in the transfer curve by increasing the collector current. We have come to an agreement that, this p- layer has effect on the electron-hole mobility as well as the depletion layer.

4.2.3.11 11th simulation

Our next simulation is depending on the change in P+ collector region. We have set the parameter as follows

	Length(um)	**Depth(um)**	**Concentration**
P+(Emitter)	**0.72**	**2.0**	**1.0e19**
P-(Emitter)	**0.7**	**0.5-1.5**	**1.0e15**
N+(Emitter)	**0.6**	**1.0**	**1.0e19**
N-(Drift region)	**2.0**	**5.1-4.1**	**1.5e15**
P+(Collector)	**2.0**	**1.0**	**1.5e19/1.8e19**
P-(Extra layer)	**2.0**	**1.0**	**1.0e17**
N+(Buffer region)	**2.0**	**1.0**	**1.0e19**
Trench Gate	**0.4**	**3.0**	**-**

Table 4.2.21 Set parameters for 11th simulation

The p+ layer is the collector region of trench IGBT. In this simulation we have focused to observe our transfer curve according to the change in our collector region. We have varied the doping of p+ collector region and obtained result for our trench gate IGBT. The collector region is always very significant for IGBT in the transistor family.

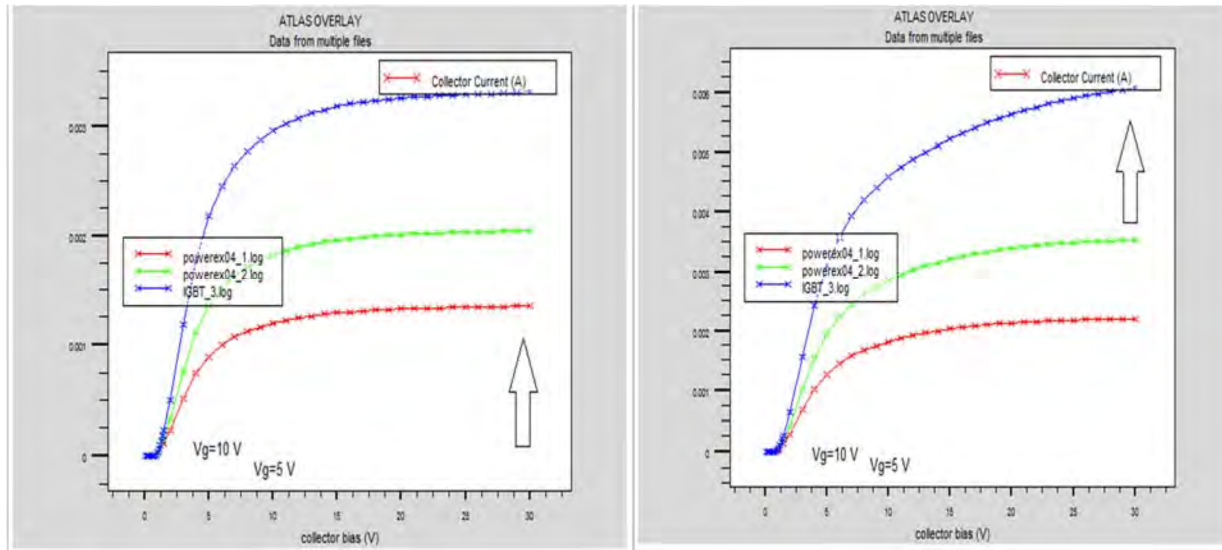


Figure 4.2.16 Output of 11th simulation

Gate voltage(Vge)	Collector Current(Ic)(Approximate) p+collector(1.5e19)	Collector Current(Ic) (Approximate) p-extra layer(1.8e19)
10V	0.0035A	0.006A
7V	0.002A	0.0035A
5V	0.0012A	0.002A

Table 4.2.22 Ic vs Vce 11th simulation output

From Fig.4.3.16 and Table.4.2.22 we can say that the increasing concentration has effective hold over electron-hole mobility as it is injecting more holes is drift region. As a result the collector current is increasing accordingly but to maintain a minimum threshold voltage we may not increase the concentration of collector region. We studied the output and obtained the solution

that we can get higher collector current with higher concentration of p+ collector region and maintain the threshold voltage as minimum as possible with this trench IGBT model.

4.2.3.12 12th simulation

After thoroughly analyzing and studying all our simulations over different doping and depths considering each region separately we fabricated a model which may provide us the maximum collector current. It is structured depending on the factors those were effectively increasing the collector current and brought significant change in the transfer carve.

Our parameters for the simulation to obtain the maximum current are illustrated in Table.4.2.23

	Length(um)	**Depth(um)**	**Concentration**
P+(Emitter)	**0.72**	**2.0**	**1.0e19**
P-(Emitter)	**0.7**	**0.5-1.5**	**1.0e15**
N+(Emitter)	**0.6**	**1.0**	**1.0e19**
N-(Drift region)	**2.0**	**5.1-4.1**	**1.5e16**
P+(Collector)	**2.0**	**1.0**	**1.1e19**
P-(Extra layer)	**2.0**	**1.0**	**1.0e17**
N+(Buffer region)	**2.0**	**1.0**	**1.0e19**
Trench Gate	**0.4**	**2.0**	**-**

Table 4.2.23 Set parameters for 12th simulation

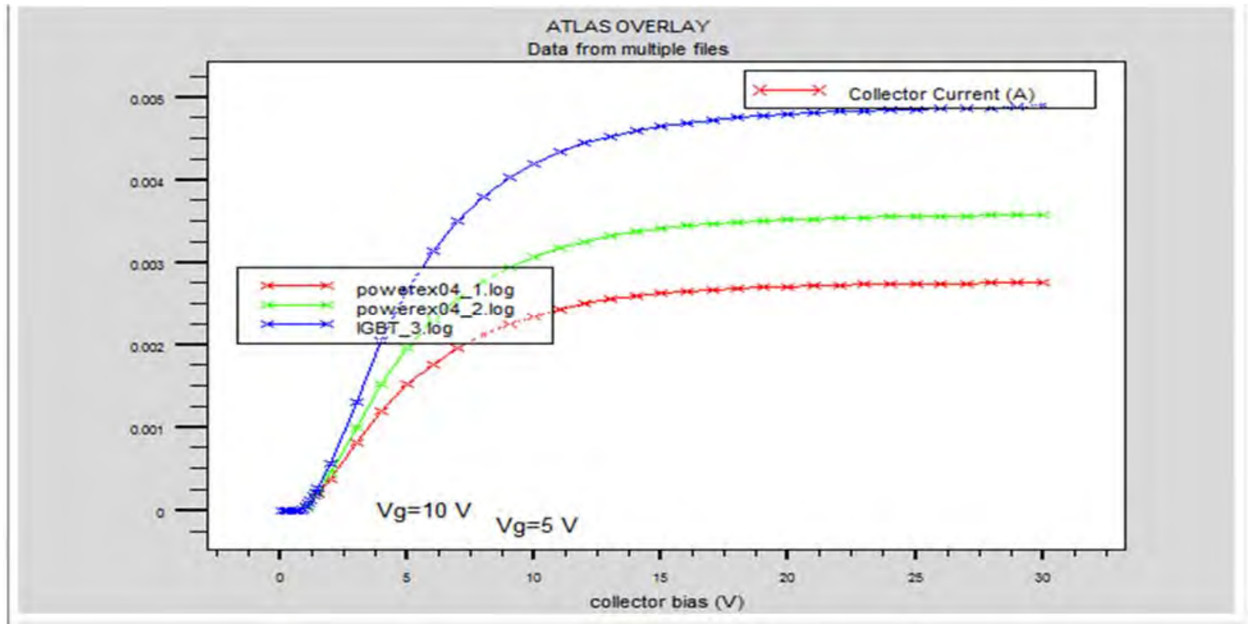


Figure 4.2.17 Output of 12th simulation

Gate voltage(Vge)	Collector Current(Ic)(Approximate)
10V	0.005A
7V	0.0035A
5V	0.0028A

Table 4.2.24 Ic vs Vce 11th simulation output

As we can see, we have obtained a higher collector current which a very significant increase as far as we have researched and analyzed our trench IGBT model considering all the simulation that has been taken place during our research.

Chapter 5

Result and discussion

In this chapter we have compared the transfer characteristics and threshold voltage between our designed trench IGBT and comprehensive Punch through IGBT model. Our purpose was to obtain better transfer characteristics with minimum threshold voltage than the existing model.

5.1 Simulation comparing transfer characteristics

Regarding the transfer curve and threshold voltage we have considered the following model parameters from our research to propose in comparison with existing Punch through model.

	Length(um)	**Depth(um)**	**Concentration**
P+(Emitter)	**0.72**	**2.0**	**1.0e19**
P-(Emitter)	**0.7**	**0.5-1.5**	**1.0e15**
N+(Emitter)	**0.6**	**1.0**	**1.0e19**
N-(Drift region)	**2.0**	**5.1-4.1**	**1.5e15**
P+(Collector)	**2.0**	**1.0**	**1.0e19**
P-(Extra layer)	**2.0**	**1.0**	**1.0e17**
N+(Buffer region)	**2.0**	**1.0**	**1.0e19**
Trench Gate	**0.4**	**3.0**	**-**

Table 5.1.1 Set parameters for proposed trench PT-IGBT

We have compared our model with a comprehensive model with following parameters

	Length(um)	Depth(um)	Concentration
P.type(Emitter)	**12.0**	**5.8**	**2.7e17**
N+(Emitter)	**7.0**	**0.8**	**9.3e19**
N-(Drift region)	**25.0**	**65.0**	**1.5e14**
P+(Collector)	**25.0**	**18.6**	**1.0e19**
N+(Buffer region)	**25.0**	**16.4**	**1.0e17**

Table 5.1.2 Set parameters for traditional PT-IGBT

With the above mentioned the PT-IGBT structure is illustrated in Fig.5.1.1

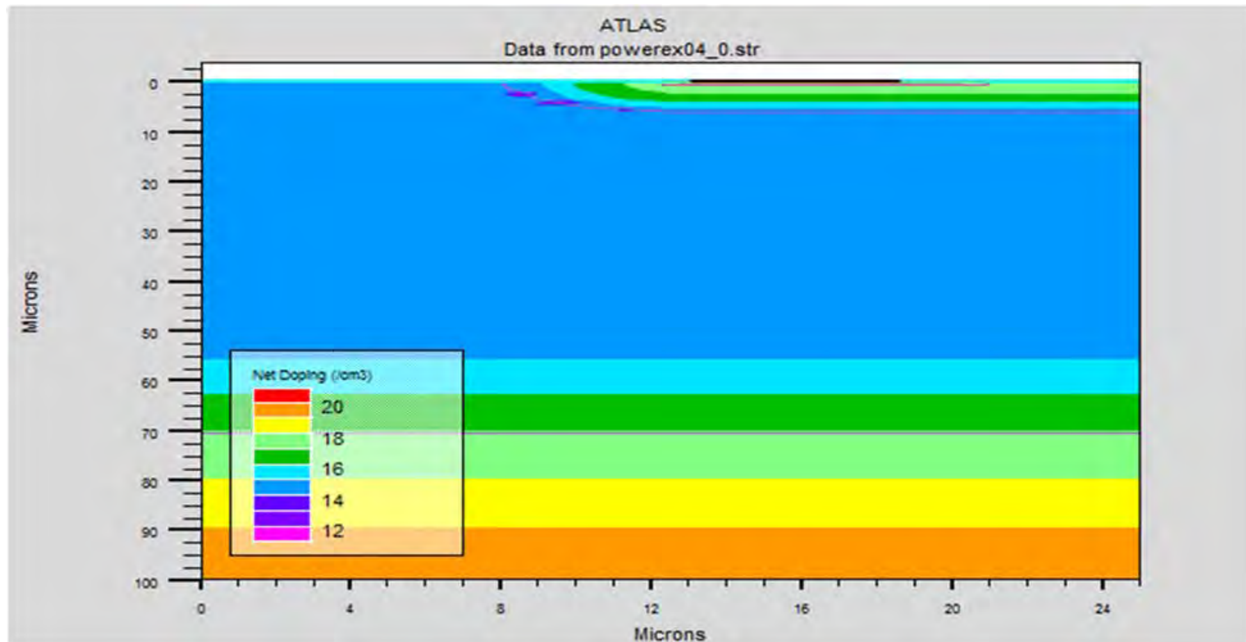


Figure 5.1.1 Comprehensive model of PT-IGBT

Through simulation we have obtained comparative transfer characteristics for both model structures which is shown in Fig.5.1.2

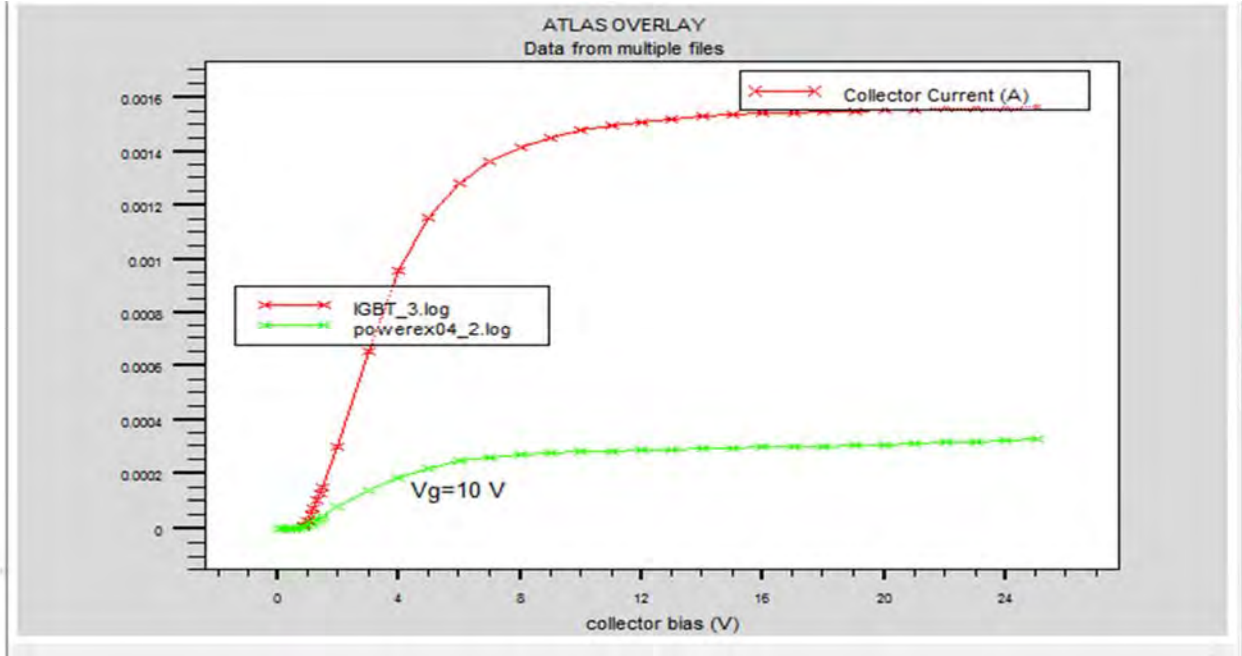


Figure 5.1.2 Comparison of transfer characteristics with Traditional Punch through IGBT

Gate voltage(Vge)	Collector Current(Ic)(Approximate) Traditional PT-IGBT	Collector Current(Ic) (Approximate) Proposed Trench PT-IGBT
10V	0.0003A	0.0016A

Table 5.1.3 Transfer characteristics comparison output

As we can see the collector voltage of our proposed model is higher than the traditional model from Table.5.1.3. Our aim was to obtain better transfer characteristics. In order to achieve that we have modeled the device in a smaller manner comparing with the traditional model as it is stated in Table 5.1.1 and 5.1.2. In order to achieve such characteristics we have introduce a p-layer as discussed earlier in a trench gate PT-IGBT.

5.2 Simulation comparing threshold voltage

In this section we have compare the threshold characteristics between both models. We could have chosen parameters regarding our model which may illustrate greater collector current but regarding the threshold voltage we have chosen this model. We were able to maintain a minimum threshold voltage in our proposed model. Regarding threshold voltage, at a low-power supply voltage, a low threshold voltage is preferable to maintain the performance trend. However, because the reduction of the threshold voltage causes a drastic increase in the cut-off current, the lower limit of the threshold voltage should be carefully considered by taking into account the stability of the circuit operation and the power dissipation.

Taking under the above mentioned criteria we have compared the threshold voltage of both models shown in Fig 5.2.1

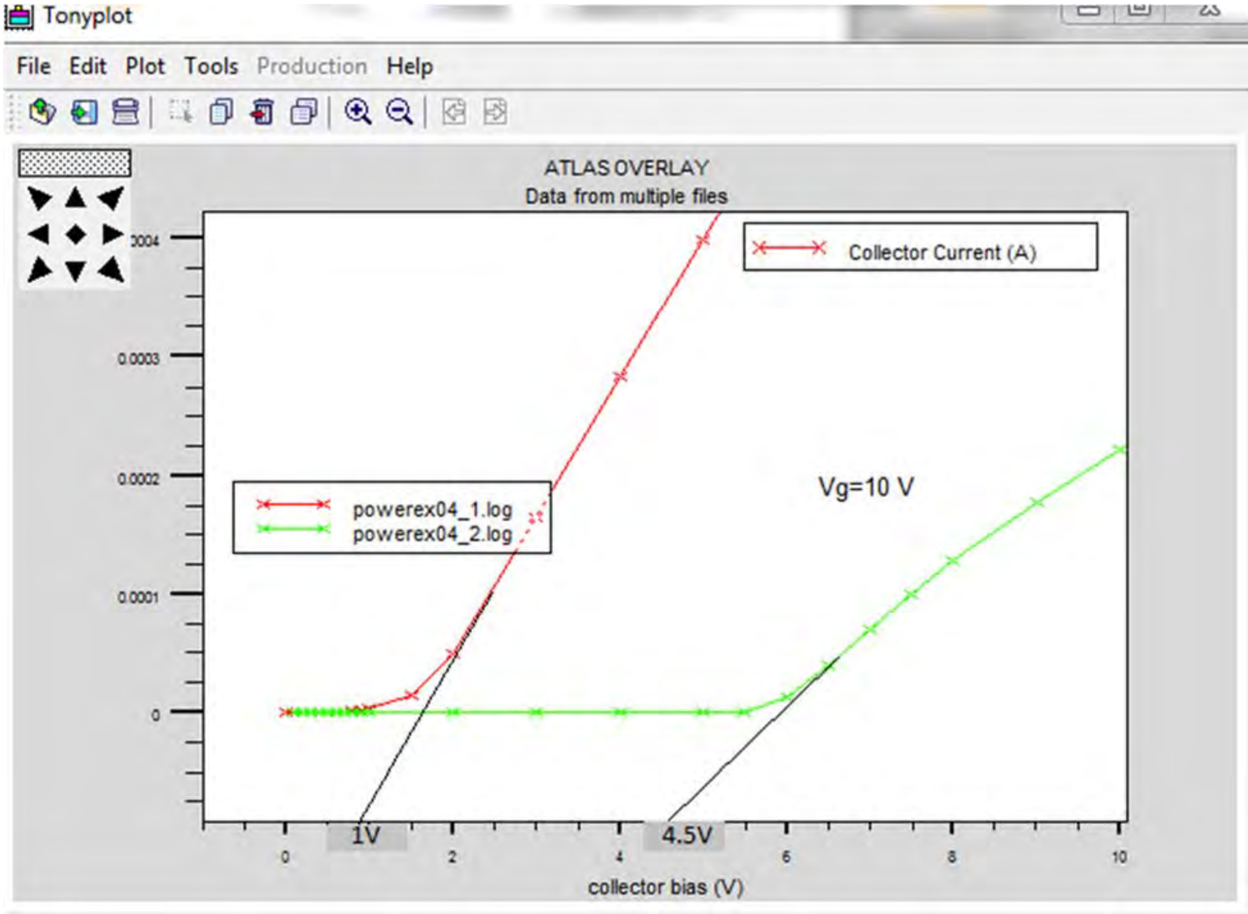


Figure 5.2.1 Comparison of threshold voltage with Traditional Punch through IGBT

Collector voltage(Vce)	Threshold voltage(Approximate) Traditional PT-IGBT	Threshold voltage (Approximate) Proposed Trench PT-IGBT
5V	4.25V	1.0V

Table 5.2.1 Threshold voltage comparison output

Chapter 6

Conclusion

In conclusion, this paper mainly introduces the new trench-IGBT with P- layer above the P+ collector region, which improves the devices transfer characteristics and decreases the threshold voltage by 3.5V. In addition our designed structure of punch through IGBT is completely a new model. Every element of different region within the device was fabricated by thorough research and experimentation. By using Silvaco-Atlas we were able to accurately characterize physics-based devices in 2D or 3D for electrical, optical, and thermal performance without costly split-lot experiments. This brief review shows that trench IGBTs are promising for the future. There are many more factors that can be tested and improve in the future research regarding breakdown voltage, low carrier life time, high carrier life time, effects due to high temperature in output characteristics and stability of the device. Moreover there can be multiple trench gates in one IGBT for further development. Although the prevailing designs do not fulfill all the requirements posed by the International Technology Roadmap for Semiconductors (ITRS), subsequent research works may lead to more practical ideas.

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Appendix A

Steady state charge control

Ambipolar Diffusion equation in Base

$$\frac{\partial^2 p(x)}{\partial x^2} - \frac{p(x)}{L^2} = 0 \qquad \text{(A.1)}$$

Boundary conditions:

$$p(x = 0) = P_0$$

$$p(x = W) = 0$$

Minority carrier concentration in n base region on IGBT is

$$p(x) = Ae^{\frac{x}{L}} + Be^{-\frac{x}{L}} \qquad \text{(A.2)}$$

Now at, $x = 0$

$$p(0) = A + B$$

$$P_0 = A + B \qquad \text{(A.3)}$$

Now at, $x = w$

$$0 = p(x) = Ae^{\frac{W}{L}} + Be^{-\frac{W}{L}}$$

(A.4)

Now multiplying $e^{-\frac{W}{L}}$ to the equation (A.3), we get

$$Ae^{-\frac{W}{L}} + Be^{-\frac{W}{L}} = P_0 e^{-\frac{W}{L}} \qquad \text{(A.5)}$$

Subtracting (A.5) from (A.4), we get A

$$A\left(e^{\frac{W}{L}} + e^{-\frac{W}{L}}\right) = -P_0 e^{-\frac{W}{L}}$$

W

$$A = \frac{-P_0 e^{-\frac{W}{L}}}{2j\ \sinh\left(\frac{W}{L}\right)} \tag{A.6}$$

Again we multiply equation (A.3) with $e^{\frac{W}{L}}$

$$Ae^{\frac{W}{L}} + Be^{\frac{W}{L}} = P_0 e^{\frac{W}{L}} \tag{A.7}$$

Subtracting (A.7) from (A.4), we find out B

$$B\left(e^{\frac{W}{L}} - e^{-\frac{W}{L}}\right) = P_0 e^{\frac{W}{L}}$$

$$B = \frac{P_0 e^{\frac{W}{L}}}{2j\ \sinh\left(\frac{W}{L}\right)} \tag{A.8}$$

So, the total solution would be

$$p(x) = \frac{-P_0 e^{-\frac{W}{L}}}{2j\ \sinh\left(\frac{W}{L}\right)} e^{\frac{x}{L}} + \frac{P_0 e^{\frac{W}{L}}}{2j\ \sinh\left(\frac{W}{L}\right)} e^{-\frac{x}{L}} \tag{A.9}$$

$$= P_0 \frac{e^{\frac{W-x}{L}} - e^{-\frac{(W-x)}{L}}}{2j\ \sinh\left(\frac{W}{L}\right)}$$

$$p(x) = P_0 \frac{\sinh\left(\frac{W-x}{L}\right)}{\sinh\left(\frac{W}{L}\right)} \tag{A.10}$$

Now, integrating p(x), we get the total steady state excess base charge

$$Q_0 = qA \int_0^W p(x)dx$$

$$Q_0 = qA \frac{P_0}{\sinh\left(\frac{W}{L}\right)} \int_0^W \sinh\left(\frac{W-x}{L}\right) dx$$

Let,

$$\frac{W-x}{L} = z$$

Differentiating

$$\frac{-1}{L} dx = dz$$

$$dx = -Ldz$$

Boundary Limits:

x=0 $\qquad z = \frac{W}{L}$

x=W $\qquad z = 0$

so, we get

$$Q_0 = qA \frac{P_0}{\sinh\left(\frac{W}{L}\right)} \int_{\frac{W}{L}}^{0} \sinh(-L) \sinh z dz$$

$$= \frac{qAP_0L}{\sinh\left(\frac{W}{L}\right)} [\cosh z]_0^{\frac{W}{L}}$$

$$= \frac{qAP_0L}{\sinh\left(\frac{W}{L}\right)} \left[\cosh\left(\frac{W}{L}\right) - 1\right]$$

We know,

$$\cosh(2x) = 1 + 2sinh^2(x) \tag{A.11}$$

$$\sinh(2x) = 2\sinh(x)\cosh(x) \tag{A.12}$$

The total excess base charge

$$Q_0 = qAP_0L \frac{2sinh^2\left(\frac{W}{2L}\right)}{2\sinh\left(\frac{W}{2L}\right)\cosh\left(\frac{W}{2L}\right)}$$

$$Q_0 = qAP_0L \tanh\left(\frac{W}{2L}\right) \tag{A.13}$$

Appendix B

Linear Charge Control

From the steady state analysis, we have

$$p(x) = P_0 \frac{\sinh\left(\frac{W-x}{L}\right)}{\sinh\left(\frac{W}{L}\right)} \quad \text{(B.1)}$$

Since the diffusion length (L) is larger than the drift layer thickness (W_B) because of the high lifetime of the carriers, one can approximate the carrier profile for the holes p(x) in the drift layer by a linear expression as shown previously

$$p(x,t) = P_0 \left[1 - \frac{x}{W(t)}\right] \quad \text{(B.2)}$$

With the aid of the general ambipolar transport hole current expression

$$I_p = \frac{1}{1+b} I_T(t) - qAD \frac{\partial p(x)}{\partial x} \quad \text{(B.3)}$$

We can find an expression forP_0 from equations (B.2) & (B.3) as

$$\frac{\partial p(x)}{\partial x} = -\frac{P_0}{W(t)} \quad \text{(B.4)}$$

As

$$(0) = 0$$

So

$$I_p(0) = I_T(t)$$

And

$$I_p(0) = I_T(t) = \frac{I_T(t)}{1+b} + \frac{2qAD_P}{1+\frac{1}{b}} \frac{P_0}{W(t)}$$

$$I_T(t)\left[1 - \frac{1}{1+b}\right] = \frac{2qAD_P}{1+\frac{1}{b}} \frac{P_0}{W(t)}$$

$$I_T(t) = I_T(t=0) = I_T(0^-)$$

$$P_0 = \frac{W(t) I_T(0^-)}{2qAD_P} \quad \text{(B.5)}$$

Since total anode current is constant$I_T(t) = I_T(0^-)$, from the above equation we can find $\frac{\partial P_0}{\partial t}$ as

$$\frac{\partial P_0}{\partial t} = \frac{W(t) I_T(0^-)}{2qAD_P} \frac{d}{dt} W(t)$$

Substituting for $I_T(0^-)$ from equation (B.5), the above equation becomes

$$\frac{\partial P_0}{\partial t} = -\frac{P_0}{W(t)} \frac{d}{dt} W(t) \qquad \text{(B.6)}$$

From Figure (3.3) the slope is negative since the behavior of (t) tends towards the minus x direction as the device voltage (t) varies with time (moving boundary). The total excess charge in the base of the IGBT is

$$Q(t) = qAP_0 \int_0^W \left[1 - \frac{x}{W(t)}\right] dx$$

$$= qAP_0 \left[x - \frac{x^2}{2W(t)}\right]_0^W$$

$$= qAP_0 \left[W(t) - \frac{W(t)^2}{2W(t)}\right]$$

$$= qAP_0 \left[W(t) - \frac{W(t)}{2}\right]$$

$$= qAP_0 \frac{W(t)}{2}$$

(B.7)

$$Q(t) = qA \frac{W(t)}{2} \frac{W(t) I_T(t)}{2qAD_P}$$

$$I_T(t) = \frac{4D_P}{W(t)^2} Q(t) \qquad \text{(B.8)}$$

Equation (B.8) is the linear charge control current and $W$is a constant in this case since

$$\frac{dV_{CE}}{dt} = 0$$

Appendix C

Ambipolar Diffusion Coefficient

At high injection levels, electrons and holes transport cannot be treated separately because the electrons move in a cloud of holes and conversely. A convenient approach to handle this situation involves combination of continuity equation for electrons with that for holes, and introduction of a new parameter, namely, Ambipolar Diffusion Coefficient, which is an algebraic function of electron and hole diffusivities and concentrations. The defining equation for the ambipolar diffusion coefficient is

$$D = \frac{nq\,\mu_n D_p + pq\,\mu_p D_n}{nq\,\mu_n + pq\,\mu_p}$$

Where,

D_n =Electron Diffusion Coefficient

D_p = Hole Diffusion Coefficient

μ_n = Electron mobility

μ_p = Hole mobility

n = electron concentration

p = hole concentration

q = charge

The advantage gained from this approach is that the resulting single equation allows focusing our attention on the minority carrier concentration, while the presence of majority carrier concentration is automatically accounted for by the ambipolar diffusion coefficient.

Now, we know from Eienstein's Equation

$$\frac{D_n}{\mu_n} = \frac{kT}{q}$$

$$\frac{D_p}{\mu_p} = \frac{kT}{q}$$

$$\frac{D_n}{D_p} = \frac{\mu_n}{\mu_p} = b$$

Assuming $n = p$

$$
\begin{aligned}
D &= \frac{nq(\mu_n D_p + \mu_p D_n)}{nq(\mu_n + \mu_p)} \\
&= \frac{\mu_n D_p + \mu_p D_n}{\mu_n + \mu_p} \\
&= \frac{\frac{\mu_n}{\mu_p} D_p + D_n}{\frac{\mu_n}{\mu_p} + 1} \\
&= \frac{bD_p + D_n}{b+1} \\
&= \frac{D_p + \frac{D_n}{b}}{1 + \frac{1}{b}} \\
&= \frac{D_p + D_n \frac{D_p}{D_n}}{1 + \frac{1}{b}} \\
&= \frac{2D_p}{1 + \frac{1}{b}}
\end{aligned}
$$

So, $$D\left(1 + \frac{1}{b}\right) = 2D_p \qquad \text{(D.1)}$$

Appendix D

Effective Depletion width from Poisson's Equation

An electric field is created in the depletion region by the separation of positive and negative space charge densities. Fig. C.1 shows the volume charge density distribution in the pn junction assuming uniform doping and assuming an abrupt junction approximation. We will assume that the space charge region abruptly ends in the n region at $x = +$, and abruptly ends in the p region at$x = -x_p$, (x_p is a positive quantity).

The electric field is determined from Poisson's equation which, for a one-dimensional analysis, is

$$\frac{d^2\emptyset(x)}{dx^2} = \frac{-\rho}{\epsilon_s} = -\frac{dE(x)}{dx} \qquad \text{(C.1)}$$

Where $\emptyset(x)$ is the electric potential, $E(x)$is the electric field, $\rho(x)$is the volume charge density and ϵ_s is the permittivity of the semiconductor. From Fig. D.1, the charge densities are

$$\rho(x) = -eN_a \qquad -x_p < x < 0 \qquad \text{(C.2)}$$

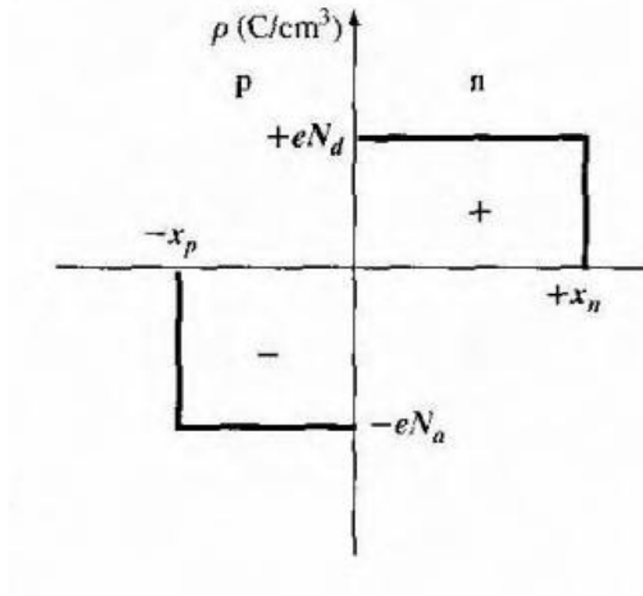

Figure C.1 The space charge density in a uniformly doped pn junction assuming the abrupt junction approximation.

and,

$$\rho(x) = -eN_d \qquad 0 < x < x_n \qquad \text{(C.3)}$$

The electric field in the p region is found by integrating Equation (C.1), we have that

$$E = \int \frac{\rho(x)}{\epsilon_s} dx = -\int \frac{eN_a}{\epsilon_s} dx = -\frac{eN_a}{\epsilon_s} x + C_1 \qquad \text{(C.4)}$$

Where C_1 is a constant of integration. The electric field is assumed to be zero in the neutral p region for $x < x_p$, since the currents are zero in thermal equilibrium. As there are no surface charge densities within the pn junction structure, the electric field is a continuous function. The constant of integration is determined by setting

$E = 0$ at $x = x_p$. The electric field in the p region is then given by

$$E = -\frac{eN_a}{\epsilon_s}(x + x_p) \qquad -x_p \leq x \leq 0 \qquad \text{(C.5)}$$

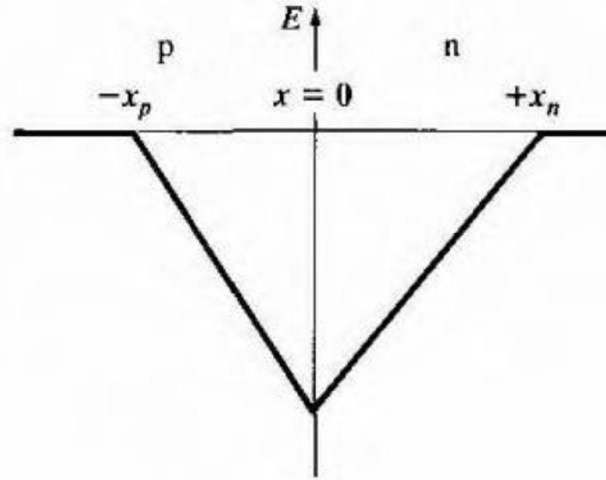

Figure C.2 Electric field in the space charge region of a uniformly doped pn junction

Then the n region, the electric field is determined from

$$E = \int \frac{eN_d}{\epsilon_s} dx = \frac{eN_d}{\epsilon_s} x + C_2 \qquad \text{(C.6)}$$

Where C_2 is again a constant of integration. The constant $C_2$is determined by setting $E = 0$ at $x = x_n$, since the Electric field is assumed to be zero in the n region and is a continuous function. Then

$$E = -\frac{eN_a}{\epsilon_s}(x_n - x) \qquad 0 \leq x \leq x_n \qquad \text{(C.7)}$$

The electric field is also continuous at the metallurgical junction, or at $x = 0$.Setting

Equations (C.5) and (C.7) equal to each other at $x = 0$ gives

$$N_a x_p = N_d x_n \qquad \text{(C.8)}$$

Equation (C.8) states that the number of negative charges per unit area in the p region is equal to the number of positive charges per unit area in the n region.

Fig. C.2 is a plot of the electric field in the depletion region. The electric field direction is from the n to the p region, or in the negative x direction for this geometry. For the uniformly doped pn junction, the Electric field is a linear function of distance through the junction, and the maximum (magnitude) electric field occurs at the metallurgical junction. An electric field exists in the depletion region even when no voltage is applied between the p and n regions.

The potential in the junction is found by integrating the electric field. In the p region then, we have

$$\emptyset(x) = -\int E dx = \int \frac{eN_a}{\epsilon_s}(x + x_p)dx \quad \text{(C.9)}$$

$$\emptyset(x) = \frac{eN_a}{\epsilon_s}\left(\frac{x^2}{2} + x_p\right) + C_1' \quad \text{(C.10)}$$

where C_1' is again a constant of integration. The potential difference through the pn junction is the important parameter, rather than the absolute potential, so we may arbitrarily set the potential equal to zero at $x = -x_p$. The constant of integration is then found as

$$C_1' = \frac{eN_a}{2\epsilon_s}{x_p}^2 \quad \text{(C.11)}$$

so that the potential in the p region can now be written as

$$\emptyset(x) = \frac{eN_a}{2\epsilon_s}\left(x + x_p\right)^2 \qquad -x_p \leq x \leq 0 \quad \text{(C.12)}$$

The potential in the region is determined by integrating the electric field in the n region, or

$$\emptyset(x) = -\int E dx = \int \frac{eN_d}{\epsilon_s}(x_n - x)dx \quad \text{(C.13)}$$

Then

$$\emptyset(x) = \frac{eN_d}{\epsilon_s}\left(x_n x - \frac{x^2}{2}\right) + C_2' \quad \text{(C.14)}$$

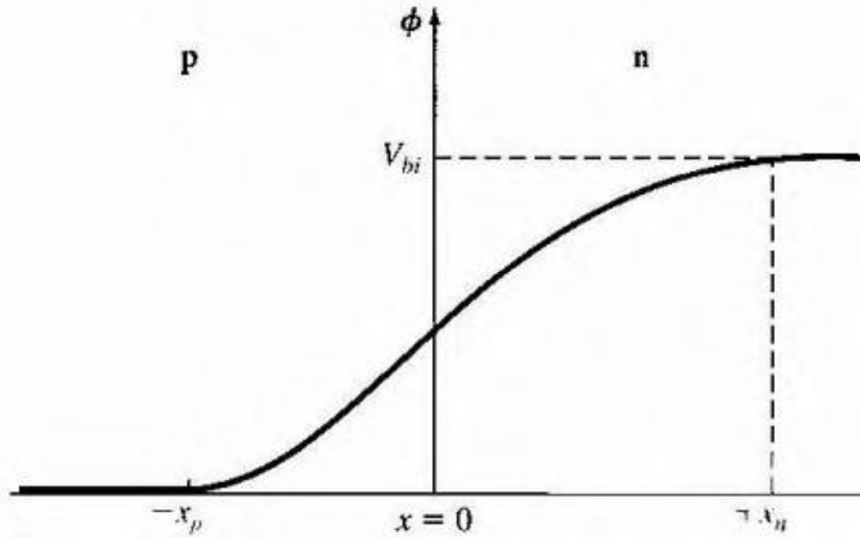

Figure C.3: Electric Potential through the space charge region of a uniformly doped pn junction

where C_2' is another constant of integration. The potential is a continuous function, so setting Equation (7.21) equal to Equation (C.14) at the metallurgical junction, or at x = 0, gives

$$C_2' = \frac{eN_a}{2\epsilon_s} x_p^2 \qquad \text{(C.15)}$$

The potential in the region can thus be written as

$$\emptyset(x) = \frac{eN_d}{\epsilon_s}\left(x_n x - \frac{x^2}{2}\right) + \frac{eN_a}{2\epsilon_s} x_p^2 \qquad 0 \le x \le x_n \qquad \text{(C.16)}$$

Fig. C.3 is a plot of the potential through the junction and shows the quadratic dependence on distance. The magnitude of the potential at $x = x_n$ is equal to the built-in potential barrier. Then from Equation (C.16), we have

$$V_{bi} = [\emptyset(x = x_n)] = \frac{e}{2\epsilon_s}\left(N_a x_p^2 + N_d x_n^2\right) \qquad \text{(C.17)}$$

We can determine the distance that the space charge region extends into the p and n regions from the metallurgical junction. This distance is known as the space charge width or Depletion

Width. From Equation (C.8), we may write;

For example

$$x_p = \frac{N_d x_n}{N_a} \qquad \text{(C.18)}$$

Then, substituting Equation (C.18) into Equation (C.17) and solving for x, we obtain

$$x_n = \left\{\frac{2\epsilon_s V_{bi}}{e}\left(\frac{N_a}{N_d}\right)\left(\frac{1}{N_a+N_d}\right)\right\}^{\frac{1}{2}} \qquad \text{(C.19)}$$

Equation (C.19) gives the space charge width or the width of the depletion region, x_n, extending into the n-type region for the case of zero applied voltage.

Similarly, if we solve for x_n from Equation (C.8) and substitute into Equation (C.17), we find

$$x_p = \left\{\frac{2\epsilon_s V_{bi}}{e}\left(\frac{N_d}{N_a}\right)\left(\frac{1}{N_a+N_d}\right)\right\}^{\frac{1}{2}} \qquad \text{(C.20)}$$

Where x_p is the width of the depletion region extending into the p region for the case of zero applied voltage.

The total depletion or space charge width W is the sum of the two components, or

$$W_{depletion} = x_n + x_p \qquad \text{(C.21)}$$

Using Equations (C.19) and (C.20), we obtain

$\frac{1}{2}$

$$W_{depletion} = \left\{\frac{2\epsilon_s V_{bi}}{e}\left(\frac{N_a+N_d}{N_a N_d}\right)\right\}^{2} \qquad (C.22)$$

In case of collector-base region of the IGBT, the collector is highly dopedp^+ region, whether the base is lightly doped n^-. So we can say $N_d \ll N_a$. From equation (C.8) we see

$$x_n \gg x_p \qquad \text{(C.23) and}$$

$$x_n \approx W_{bcj} \qquad (C.24)$$

where $W_{bcj} = W_{depletion}$. Here $V_{bi} = V_{CE}$ (collector-emitter voltage), q=e (electron charge) and $N_d = N_b$ (base impurity concentration). So the base-collector depletion width reduces to

$$W_{bcj} = \left\{\frac{2\epsilon_s V_{CE}(t)}{qN_B}\right\}^{\frac{1}{2}} \qquad (C.25)$$

If the metallurgical base width is W_B, then the effective depletion width can be written as

$$W(t) = W_B - W_{bcj}(t)$$

$$W(t) = W_B - \sqrt{\left\{\frac{2\epsilon_s V_{CE}(t)}{qN_B}\right\}} \qquad (C.26)$$

Appendix E

Sample of Code

```
go atlas
TITLE : PT_IGBT

# Silvaco International 1994

mesh

x.mesh loc=0.0   spac=0.1
x.mesh loc=0.42   spac=0.08
x.mesh loc=1.08  spac=0.07
x.mesh loc=1.6  spac=0.15
x.mesh loc=2.0  spac=0.12

y.mesh loc=-0.08 spac=0.04
y.mesh loc=0.0   spac=0.01
y.mesh loc=0.12   spac=0.04
y.mesh loc=1.6   spac=0.2
y.mesh loc=5.0  spac=2.0
y.mesh loc=10.0 spac=1.0


region     num=1 y.max=3.0  oxide
region     num=2 y.min=3.0  silicon
region     num=3 y.min=0.0 x.min=0.4 x.max=1.82 silicon
```

```
#   electrodes #1 - gate; #2 - emitter #3 - collector

elec      num=1 left  y.min=-0.08  y.max=2.99 length=0.40 name=gate
elec      num=2 right   y.min=0.0  y.max=0.0 x.min=0.45 length=1.5  name=emitter
elec      num=3 bottom  name=collector

#   impurity profile

doping     uniform conc=1.5e15 n.type
doping     uniform conc=1.0e19 p.type     y.t=9.0 y.b=10.0
doping     uniform conc=1.0e17 p.type     y.t=8.0 y.b=9.0
doping     uniform conc=1.0e19 n.type     y.t=7.0 y.b=8.0


doping     uniform conc=1.0e21 p.type    y.t=0.0 y.b=2.0 x.l=1.1 x.r=1.82
doping     uniform conc=1.0e19 n.type    y.t=0.0 y.b=1.3 x.l=0.5 x.r=1.1
doping     uniform conc=1.0e15 p.type    y.t=1.1 y.b=1.8 x.l=0.5 x.r=1.1
doping     uniform conc=1.0e15 p.type    y.t=0.0 y.b=1.8 x.l=0.4 x.r=0.5
save outf=IGBT_0.str
tonyplot  IGBT_0.str

########################################
#Codes for measurements
########################################
```