Analysis of Bulk Negative Capacitance Field Effect Transistor

A Thesis

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Declaration

This is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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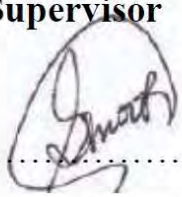

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Abstract

In this work, a comprehensive analysis of bulk Negative Capacitance Field Effect (NCFET) transistor has been done. The objective of the paper is to show if a ferroelectric insulator is introduced in MOSFET structure, it should be possible to obtain a value of sub-threshold slope (SS) lower than 60mV/decade that puts a fundamental lower limit on the operating voltage and hence the power dissipation in standard FET based switches. Si doped HfO_2 has been used as the ferroelectric material of NCFET. Polarization, energy distribution, dielectric constant, anisotropy constant variation of the Ferroelectric material has been analyzed. Condition to avoid hysteresis effect of the ferroelectric has been indicated. A numerical model of the device has been developed in Silvaco, ATLAS which included Fermi-Dirac Carrier Statistics, Shockley-Read Model, and Lombardi CVT models. Charge distribution of baseline MOSFET has been extracted from TCAD model and incorporated in 1-D Landau model to find the voltage drop across ferroelectric material. Ultimately device transfer characteristics with and without ferroelectric layer has been compared. Due to the use of FE layer, relative improvement in the device performance (especially in SS region) is observed compared to the conventional MOSFET device.

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Chapter 1

Introduction

With the rapid development of technology, the need of smaller and more efficient gadgets has been increasing for smarter and easier life.CMOS being the dominant technology for integrated circuits, the scaling of MOS has been a primary concern of electronics industry. This need for more integrated and efficient circuit has fueled the scaling trend of MOS. To scale MOS intro smaller device, channel length of MOS is being reduced and that resulted in decrease in power per switching event and improvement in density. Along with this, the power density and the total chip power consumption have also been increasing. Due to this, the parameters of VLSI design such as effective channel length, gate dielectric voltage, supply voltage, device leakage have been changed a lot to get the desired integrated circuit. Hence, the transistors manufactured today are 20 times faster and occupy less than 1% space from the ones built two decades ago[1].

The CMOS technology has been very useful for VLSI circuit because it can be scaled down to smaller dimension which in turn provides higher performance [2]. CMOS has become the

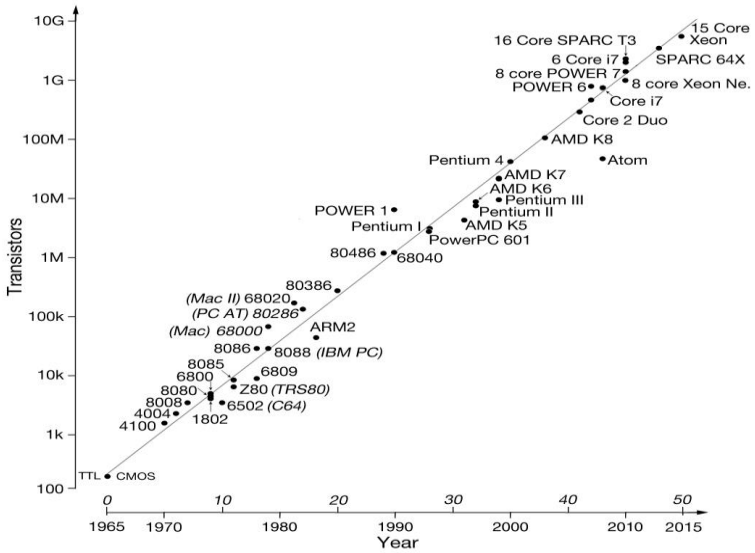


Figure 1.1: This shows from 1971 to 2015, how the number of transistors per chip increased with time in logarithmic vertical scale against the dates of introduction. The straight line indicates the exponential growth of transistor density.

dominant technology for integrated circuits due to this consistent scope of improvement. According to an observation by Gordon Moore in 1966, the number of transistors in a dense integrated circuit doubles in every two years which played a significant role to accelerate the scaling trend of transistors.

Decrease in drain to source length (channel length) of MOS allows smaller circuit. But reducing the channel length creates some undesirable changes in device characteristics [3]. To maintain the flow of Moore's Law, the oxide thickness needs to be decreased. The voltage supply needs to be scaled inversely alongside the changing transistor sizes [4] which can be defined by the basic equations of electromagnetism relating to the decrease in capacitance which results in increase in thermal noise (defined by Nyquist) . As a result, it increases the probability of bit-flipping which decreases the overall reliability.

1.1 Scaling trends

Scaling MOS to smaller physical dimensions have contributed to higher levels of integration. The most renowned scaling scheme of MOS was proposed by Robert Dennard and his team in 1975 that is known as constant field scaling [5]. To maintain the qualitative performance as we scale the device into smaller sizes, Dennard suggested the following scaling scheme,

Description	Parameter	Scaling
Device Dimension	L, W	1/S
Oxide thickness	TOX	1/S
Channel Doping	NSUB	S
Power Supply	VDD	1/S
Junction Depth	XJ	1/S

Table1.1: Constant Field Scaling

(From Table1) the oxide thickness and depletion width are decreased by the same factor as the supply voltage, all the electric fields within the device remains constant. This seemed to be an advantage at the beginning when scaling of MOS started. Later, it has been observed that, for smaller device, it decreases the device performance (thermal noise, bit flipping). Though this table played a significant role by showing how much it is necessary to scale

oxide thickness and doping level to scale MOS, it was not good enough for scaling of power supply voltage. Therefore, it led the industries to not use the table entirely.

Emphasizing more on performance and reliability, it is necessary to scale the parameters to provide highest performance. [6] Satisfying the basic requirements the limitations of scaling MOS are elaborated further,

To keep the power density constant, supply voltage and threshold voltage need to be reduced proportionally. On the other hand, to keep the power consumption low, it is required to maintain high threshold to limit the leakage current.

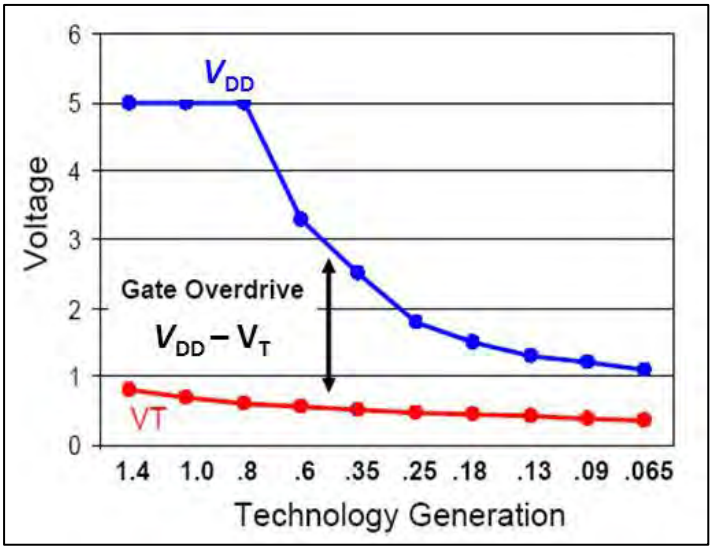


Figure 1.1.1: Threshold voltage, V_T and supply voltage, V_{DD} scaling vs. technology generation that shows that the supply voltage has not been scaled down in proportion to the threshold voltage.

Source: P. Packan (Intel), 2007 IEDM Short Course

Due to this, the power supply voltage must be significantly above the threshold voltage. This eventually limits the power supply to decrease enough to follow the constant field scaling method.

1.2 Inadequacies of MOSFET

1.2.1 Power dissipation

The power dissipation of CMOS are mainly categorized into two types; Static and dynamic power dissipation. Static power dissipation occurs when the transistor is in standby mode. For

example, when the transistor is OFF, there should not be any current flow through the channel. But practically, there is leakage current in the sub-threshold region that results into static power dissipation. The thinner oxide and higher supply voltage create gate induced drain leakage current.

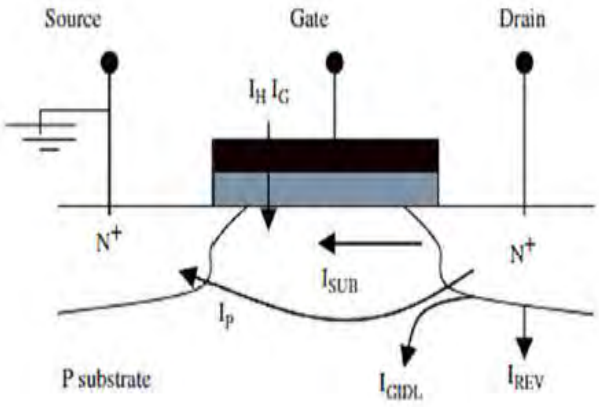


Figure 1.2.1: The leakage current for NMOS is shown. $I_G$stands for gate oxide tunneling current that flows from gate to substrate and vice versa, I_{SUB} represents leakage current in sub-threshold region, I_{REV}representsleakage current when MOS is in reverse bias, I_{GIDL}stands for gate induced drain leakage current [7].

On the other hand, the power consumed by CMOS due to short channel current is called dynamic power consumption. It occurs due to the charging and discharging of the output capacitive load [7]. Since there is a specific rise and fall time for PMOS and NMOS, there will be a small period of time when both the transistors will be on. Therefore, direct current will flow from V_{DD} to ground which is called short circuit current.

1.2.2 Short Channel Effects

When a MOSFET channel is scaled down, V_T becomes dependent on the channel length and drain to source voltage. These are respectively known as short channel effect and drain induced barrier lowering (DIBL). In particular, five different short channel effects have been distinguished; (1) drain induced barrier lowering (DIBL), (2) surface scattering, (3) velocity saturation, (4) impact ionization and (5) hot electrons [8].

When the depletion region surrounding the drain extends to the source, punchthrough occurs. It can be minimized by thinner oxide, larger substrate doping, shallower junctions and obviously by using longer channel. On the other hand, if the gate bias voltage is not sufficient to create an inversion layer on the surface, the carriers in the channel face a potential barrier. In short channel devices, the potential barrier is controlled by both V_{GS} and V_{DS}. If V_{DS} increases, potential barrier in the channel decreases leading to DIBL. Therefore, current flows even when $V_{GS}<V_T$.

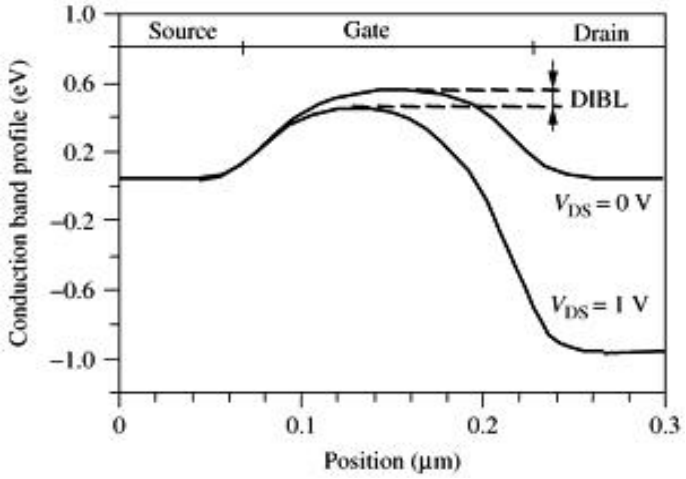


Figure 1.2.2: Drain Induced barrier lowering in MOS. Here it is shown that the potential barrier in the channel changes with VDS which can lead to a current flow before threshold.

With the extension of the depletion layer into the channel region, electric field component at the Y-axis increases and surface mobility becomes more field dependent. The electrons that are accelerated toward the interface by the lateral field faces collisions that results in reduction of the mobility.

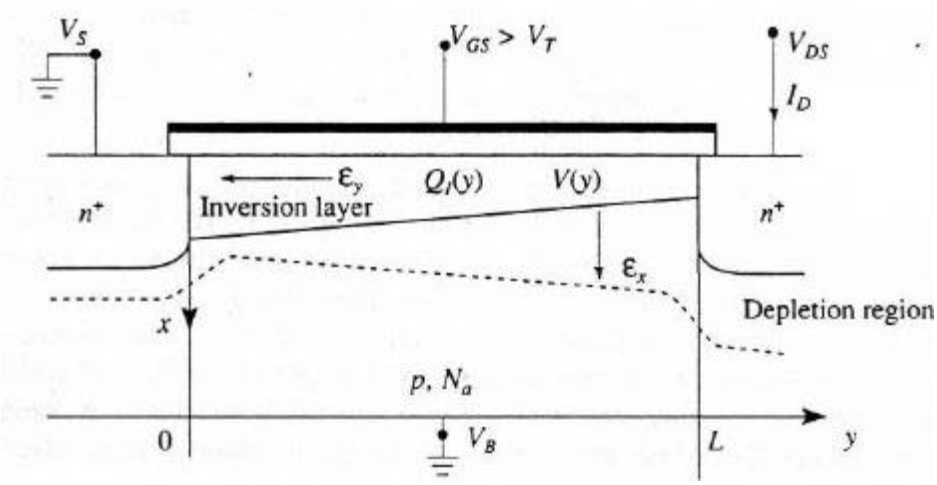


Figure1.2.2: Surface scattering due to the vertical component of electric field, E_Y[8].

Moreover, when E_Y increases above 10^4 V/cm, the drift velocity increases more slowly with the field and this is known as velocity saturation. Another short channel effect that occurs specially in NMOS is impact ionization. The high velocity electrons in presence of high electric field generate electron-hole pairs. This ionizes the silicon atom. High lateral electric field in the channel excites some electron to pass through the gate oxide. These high electrons result the drain current in off state and increase V_T and affects the gate's control on drain current which is known as hot electron.

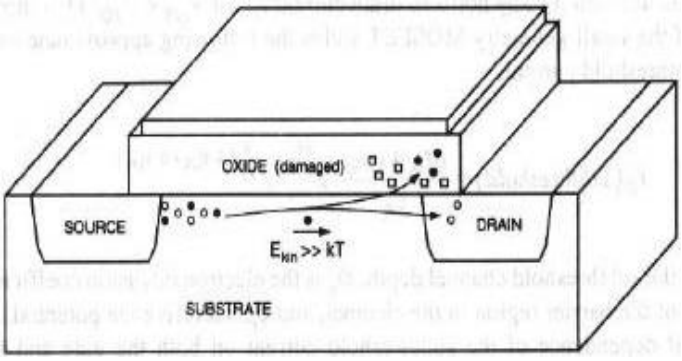


Figure 1.2.3: Hot Electrons entering the oxide.

1.2.3 Sub-threshold Swing

For simple MOSFET it is assumed that the device's drain current is 0 when $V_{GS}<V_T$. However, while $V_{GS}<V_T$ the drain current decreases exponentially to 0 resulting off state current or sub-threshold current (SS).

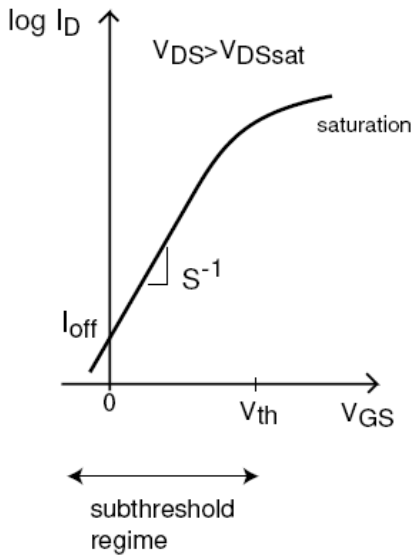


Figure 1.2: Here, showing the exponentially decreasing drain current, I_D in the sub-threshold regime known as sub-threshold current.

The slope of the sub-threshold current can be shown as $d(V_G)/d(\log I_D)$. This current depends on the depletion capacitance of the channel.Mathematically SS is defined as,

$$SS = \frac{\mathrm{d}(\mathrm{V_G})}{\mathrm{dlog}(\mathrm{I_D})} = \left(\frac{\mathrm{kT}}{\mathrm{q}}\ln 10\right)\left(1 + \frac{\mathrm{C_D}}{\mathrm{C_{OX}}}\right)$$

C_D is the depletion capacitance in the channel. At room temperature,$T = 300K$ substituting $k = 1.3806 \times 10^{-23}$g, $q = 1.6 \times 10^{-19}$

$$\mathrm{SS} = (60 \times 10^{-3})\left(1 + \frac{\mathrm{C_D}}{\mathrm{C_{OX}}}\right)$$

This means at the room temperature with the best case where $C_D \ll \mathrm{C_{OX}}$, theoretically SS will be 60mV/decade [6].

However, the less the ratio of the currents at$V_{GS} = V_T$and $V_{GS}= 0$ or the I_{ON} and I_{OFF} ratio, the less the leakage current will be. Therefore, for a high performance chip, the current ratio needs to be as low as possible and the sub-threshold slope to be steeper which can be a solution for the situation. Different transport mechanisms can be applied for the solution of this problem such as impact ionization, tunneling and positive feedback basically by amplifying the gate voltage [9]. Since, MOS is designed to be ON at V_T, this sub-threshold current creates flawed device.

However, if the power supply voltage is not scaled with the oxide thickness, electric field in the oxide increases. This electric field in the gate oxide creates gradual degradation of oxide layer causing dielectric breakdown eventually [10]. Therefore, for long time reliability, gate oxide layer cannot be thinned extremely.

1.3 Possible Solutions

Since, some of the fundamental parameters of MOSFET are reaching its fundamental limit, introduction of new devices, technologies and structures are necessary to hold Moore's Law in the long run.

1.3.1 Impact Ionization

To solve the problems of MOS scaling different device ideas have already been proposed. As the solution for impact ionization a p-i-n structure with lightly doped breakdown region can be used. This reduces the field required for impact ionization. On a simulation including models for both impact ionization and BTBT (band to band tunneling) at 400K temperature the impact ionization coefficients were found to be lower and anSS of 5mV/decade was achieved [11].

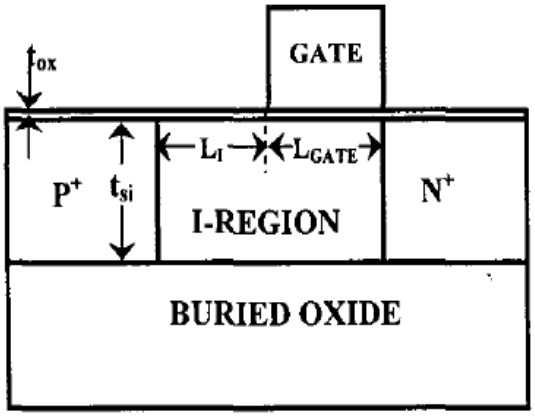


Figure 1.3.1: Basic structure of an n channel IMOS.

At low V_G there is no inversion layer under the gate and the effective channel length is the entire I region. With the increase in V_G, inversion layer forms under the gate increasing the electric field. This is lightly doped; therefore field is not enough for impact ionization.

1.3.2 Feedback FET

To turn on the transistor faster than 60mV/decade positive feedback mechanism can be used [22]. The concept of positive feedback is widely used in operational amplifiers where it results in large change in output signal with a small input current. Therefore, in a MOS with positive feedback, a small change in V_G can induce a large change in the drive current.

The basic structure of a feedback FET is similar to MOSFET. Instead of similar type doing in the source and drain, FBFET is doped with opposite dopants and the silicon underneath the nitride spacers are undoped (Figure 1.3.2).In off state the electron and hole barriers are large which allows very small current. A small change in the gate voltage can lower electron barrierwhich slightly increases the electron current flowing into the channel from N+ source. Then these electrons accumulate near the P+ region and reduce the hole barrier. These holes

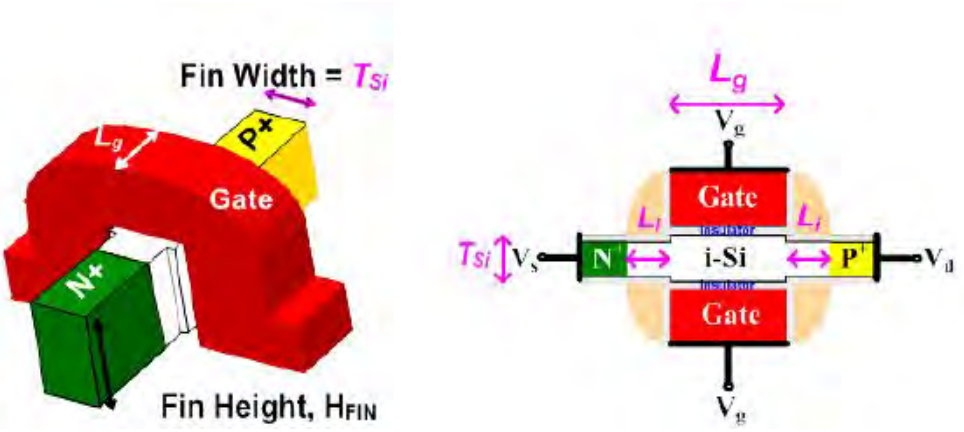


Figure 1.3.2: Isometric view and cross sectional view of FBFET fabricated on SOI wafer using finFET technology [22].

will accumulate near the N^+ region and further reduce the electron barrier. Thus the device will turn on with small change in V_G.

1.3.3 Tunnel FET

Tunnel FET is another solution proposed to overcome the short channel effects. Tunnel FET is fabricated based electron tunneling through the source to drain barrier. It uses lower voltage to turn ON and OFF and reduces power consumption.

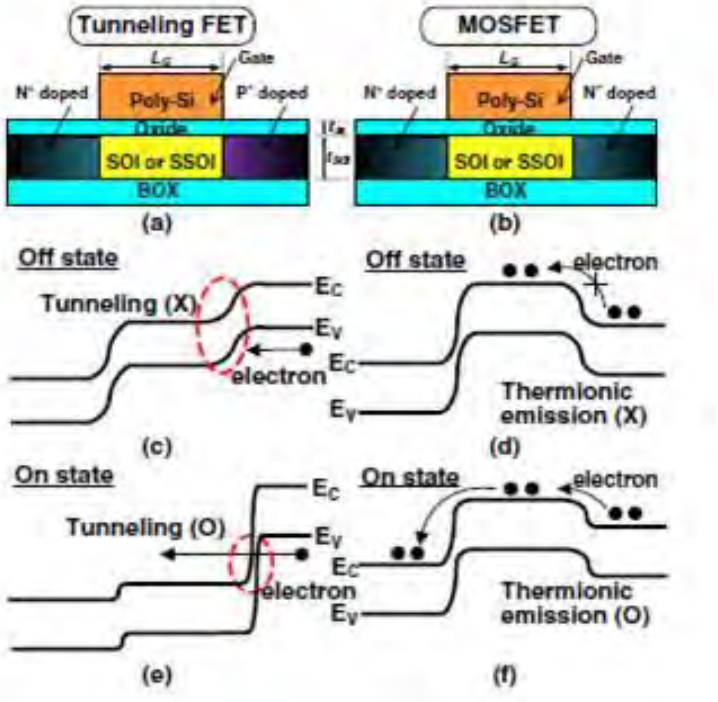


Figure 1.3.3: Relative structure and energy band diagram stating ON and OFF condition between TFET and MOSFET.

An n-channel TFET consists of highly doped P^+source, nearly intrinsic channel and N^+ drain. When a gate voltage is applied to gate electrode of tunnel FET the width of the barrier between the source and the channel increases due to the electric field (*Figure 1.3.3*). As a result the electrons pass through the barrier because of the tunneling effect which implies that current flows through the transistor [12]. This occurs at lower gate voltage and the switching activity is faster than conventional MOSFET.

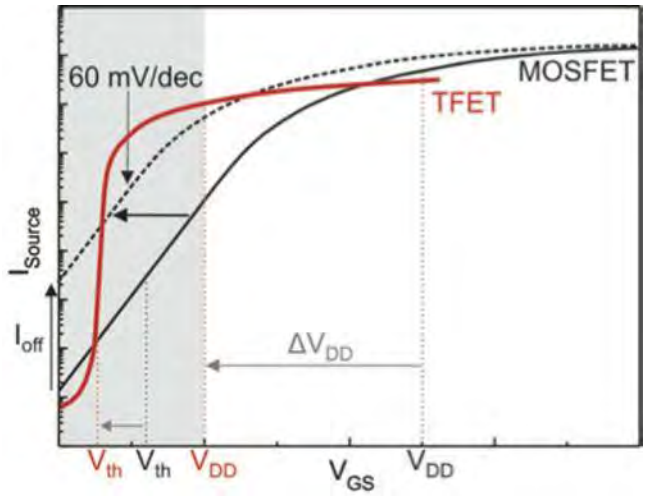


Figure 1.3.4: A comparative I_D vs. V_{GS} curve of TFET and MOSFET showing the sub-threshold slope.

TFET is a sharper turn-on device compared to MOSFET (*Figure 1.3.4*). The very fast switching leads to a steeper sub-threshold slope. As a result TFET shows better performance in ultra-low power applications.

Because of the tunneling effect, the current passing through the TFET is smaller than the current through the MOSFET. To obtain a higher current efficiency, a stronger electric field is required in the tunnel junction. For this, a high gate voltage is necessary while TFET needs to be operated at a lower gate voltage to reduce power consumption.

1.4 Outline and overview

The research work in this thesis has been described in five chapters. This chapter introduces with the problem in hand and the methodology to solve the problem. The upcoming chapters unveil the NCFET operation and its ability to improve the SS of the MOSFETs.

In Chapter 1, mainly the importance of transistors and the problems in its path of development have been discussed. The most famous scaling rules for transistors and how it follows Moor's Law has been described briefly. But these rules have their limitations and a good number of solutions for these limitations has already been proposed. A short description about these limitations and their proposed solutions are also discussed in this chapter.

In Chapter 2, a detailed description on Negative Capacitance Field Effect Transistor and its exceptional structure with ferroelectric material is presented. The hysteresis, polarization characteristics and how the use of ferroelectric material can lead to steeper sub-threshold swing have been discussed in this chapter. Moreover, this chapter also includes a brief history of NCFET and all the works that have been done before the writing of this thesis.

Chapter 3 prioritizes on the numerical analysis of the research using process simulator ATLAS, Silvaco version 2010. After defining the device structural properties like meshing, doping concentrations, models and electrodes etc., numerically surface potential, electric field, band diagram, carrier concentration can be extracted for that device using TONYPLOT. Besides, I_D-V_{GS} curve for different biasing conditions is also extracted from TONYPLOT.

Chapter 4 focuses on solving Landau equations and extract Landau coefficients from the equation. The ferroelectric material Si-doped HfO_2 , its advantages, disadvantages has been introduced in this chapter. Polarization, surface potential, Electric field etc. have been extracted for different ferroelectric thickness conditions. The structures of Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) and Metal-Ferroelectric-Insulator-Semiconductor have been designed and its characteristics have been discussed. Moreover, simple bulk NCFET operation and its potential, electric field, band diagram and charge concentration in different operating regions have been briefly described. I_D-V_{GS} graph has been extracted and compared with the conventional MOSFET to see the steeper SS.

Finally, Chapter 5 concludes the thesis of this dissertation by depicting scopes and limitations of this work.

Chapter 2

Negative Capacitance Field Effect Transistor

In the trend of introducing new device structures for transistors Negative Capacitance FET (NCFET) is one of the newest devices. The basic structure of an NCFET includes a ferroelectric material as gate insulator [13].

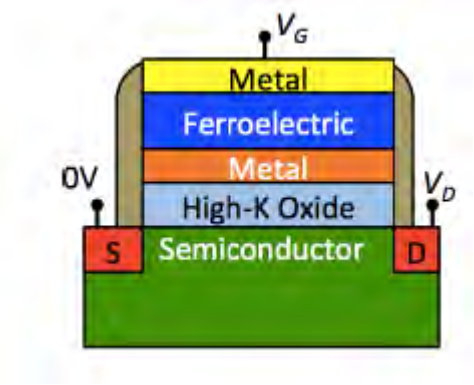


Figure 2.1: Basic structure of NCFET using ferroelectric material as gate insulator [23]

2.1 Ferroelectric material and negative capacitance

Ferroelectric materials are like dielectric material with only difference in property that is ferroelectric materials gets polarized even in the absence of electric field. The concept of ferroelectricity is not new. In 1921 J. Valasek who was researching on the properties of Rochelle salt ($NaKC_4H_4O_6.4H_2O$), discovered the phenomena of ferroelectricity. Later KDP (KH_2PO_4) and Barium Titanate ($BaTiO_3$) was also discovered to be ferroelectric. The basic properties of ferroelectric materials can be listed as

1. It is capable of getting polarized when electric field is 0 named as spontaneous polarization.
2. Ferroelectric materials have pre-existing or permanent dipoles or natural dipoles.
3. The individual dipoles are not randomly oriented but the regions or domains consisting of dipoles are randomly oriented which causes zero net polarization at zero electric field.
4. When external electric field is applied the dipoles are oriented in parallel in the domains and they are aligned with the direction of electric field.

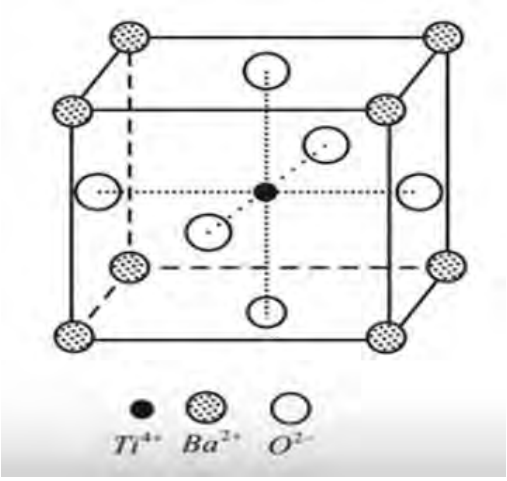


Figure 2.1.1: As $BaTiO_3$ represents the ferroelectric material characteristics properly, here showing the crystal structure of $BaTiO_3$

There are 4 different perovskite structures and cubic perovskite is one of them. The structure of $BaTiO_3$is similar to the cubic perovskite structure. Cubic perovskite is cubic symmetrical structure but $BaTiO_3$ is not actually a cubic symmetry because of the distortion and displacement of the center of positive charge and the center of negative charge even in the absence of electric field.

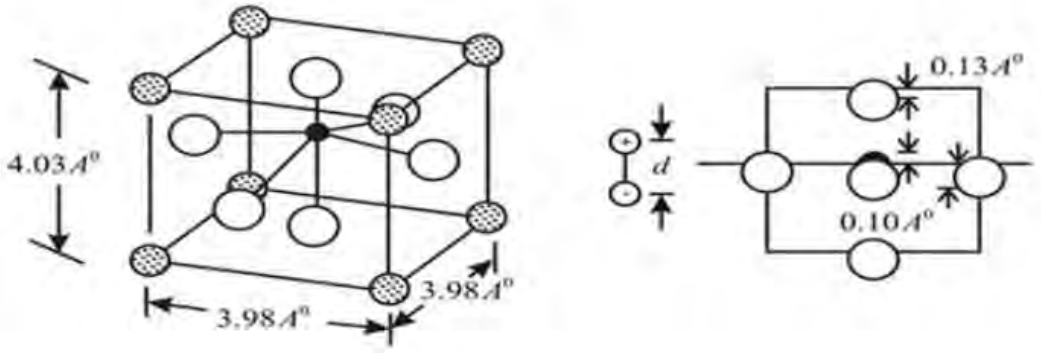


Figure 2.1.2: Showing the displacement of the center atom or Oxygen in the $BaTiO_3$ crystal.

From the cross section of the cube, it can be seen that the Oxygen ions are displaced downwards about 0.13 Angstroms below the center of the phase. Therefore, all of them are displaced from the symmetric position. Ba and Ti both are positively charged and because of the positive charges, the Oxygen ions are displaced downwards. That is how dipoles are created in the ferroelectric materials where positive charges are upwards and negative charges are placed little bit downwards. Thus dipole moments are generated and that is the origin of

spontaneous polarization. It is basically the tetragonal symmetry that gives rise to the spontaneous polarization.

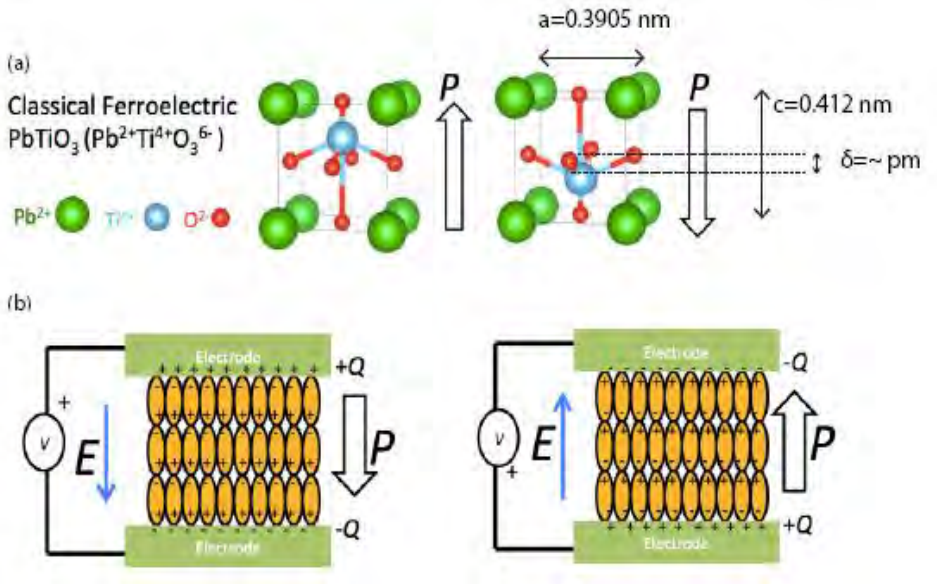


Figure 2.1.3: change in the orientation of dipole moments with the voltage applied more than coercive voltage. [23]

The dipole moments are oriented in certain regions and those regions are known as domains. The domains stay together like a crystal structure. The individual dipole moments are randomly oriented but they are always in a group forming parallel orientation in a domain. Polarity of electrically charged system is measured in terms of electric dipole moment, P which is the product of charge, Q and the displacement vector, r. here polarization refers to the density of permanent or induced electric dipole moments in a material.

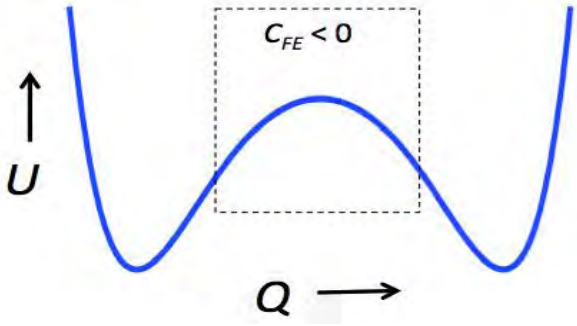


Figure 2.1.4: Energy landscape of a ferroelectric material [23]. The dotted area represents the negative capacitance region.

Ferroelectrics switch their polarization when a certain critical voltage is reached which is known as coercive voltage. This causes an enormous sudden accumulation of bound charge at the material's surface that can be momentarily exceed the free charge supplied to the electrodes by a power source. If a resistance is placed between the electrodes and the charge supplied by the external voltage is slowed down, a decrease in voltage across the ferroelectric can be detected while the charge is still increasing. Consequently, the capacitance (charge divided by voltage) has a negative value which is named as negative capacitance.

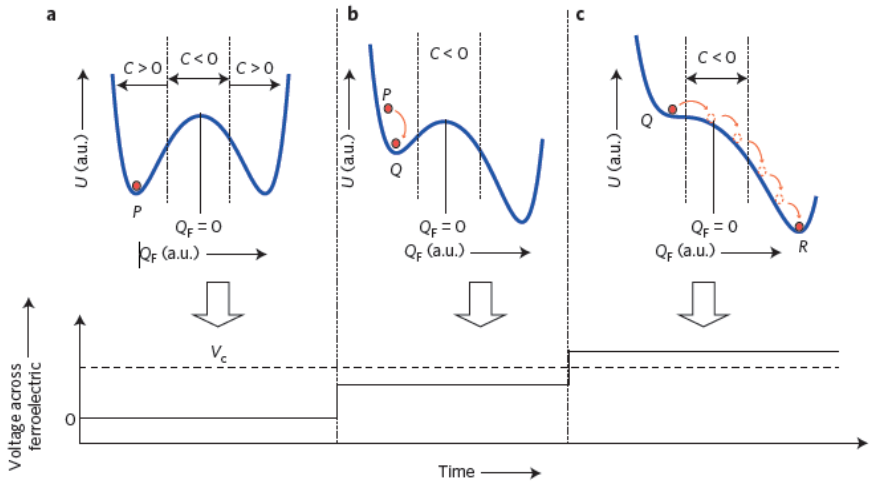


Figure 2.1.5: P, Q and R are representing different polarization stages in energy landscape. (a) When applied field is 0, capacitance C is negative at the barrier region. Where (b) and (c) shows the change in barrier region when voltage is applied across the ferroelectric capacitor. It shows that with enough voltage applied (greater than coercive voltage) the polarization passes through the negative capacitance region [13].

One of the inherent characteristics of ferroelectric material is its hysteresis. The polarization is not directly proportional to the electric field. At the very beginning, the net polarization is 0 due to the random orientation of domains at E=0. Therefore the curve starts from 0. When electric field is applied, all the dipoles tend to orient themselves along the direction of electric field. Some domains will be favorably oriented with the direction of electric field, whereas, others will completely misalign. In a word, after applying field, the favorably oriented domains try to grow in size and unfavorably oriented domain want to sink. At the end of the process, all the domains will have parallel orientation aligned with the direction of electric field and maximum polarization occurs at that stage, known as saturation polarization. Beyond this level, polarization does not change with the applied electric field.

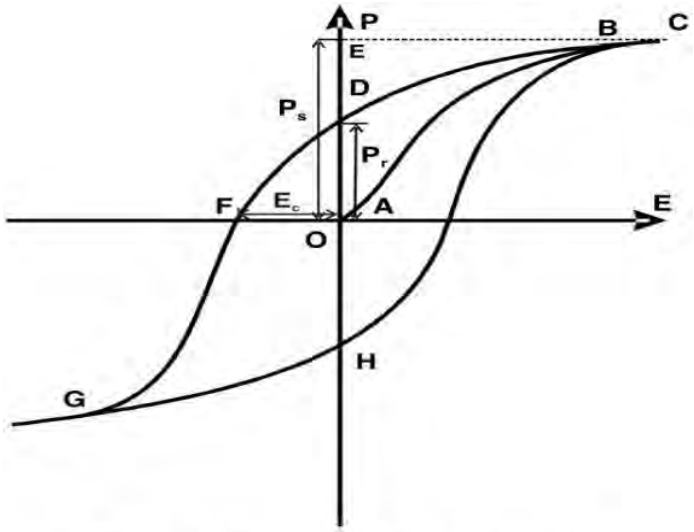


Figure 2.1.6: Ferroelectric Hysteresis plotted as polarization vs. electric field

On the figure 2.1.6 ABC represents the increase in polarization from 0 to saturation. AE shows the saturation polarization, P_S. after saturation, if we try to lower down the applied field, the curve does not follow the path CBA. Rather, it follows CBD. It happens because the polarization ferroelectric materials follow is orientation polarization, so the atoms have to move from one place to another. It is a sluggish process, therefore, even if the electric field is reduced, the atoms cannot come to its original position and results in a phase lag between the electric field and the change in orientation of domains. That is why, even in 0 electric field there remains a positive polarization and this phenomena is called remnant polarization, E_R. The distance AD from the figure 2.1.4 shows the remnant polarization. To make the polarization 0 again, a negative electric field needs to be applied known as coercive field, EC. AF shows the coercive field. If we go further in the negative direction, the curve will saturate again and the domains will be aligned in parallel with the negative electric field and here FG shows the path of change. After that if we go to zero electric field again, we will get negative polarization. If we further increase the electric field, the polarization will again meet the saturation point C. This continuous process with the change of electric field is known as the hysteresis loop of ferroelectric material.

2.2 NCFET

In 2008, Salahuddin et al. published that if we use negative capacitance material as gate insulator in MOSFET (NCFET), the sub-threshold swing can be reduced below the fundamental limit of 60mV/decade [14]. This means small change in gate voltage creates a larger change in the surface potential. But achieving this negative capacitance depends on the ability to drive ferroelectric material away from its local minimum to non-equilibrium state. In the non-equilibrium state, its capacitance is negative but the stage is very unstable. By adding a series capacitance it can be stabilized [15] making it possible for the channel potential, ψ_s on an internal node to change more than the applied voltage.

The structure of NCFET is basically same as MOSFET, except that the gate insulator is replaced by a ferroelectric material. A ferroelectric MOS capacitor can be modeled by a series connection of a ferroelectric capacitance and a channel capacitance.

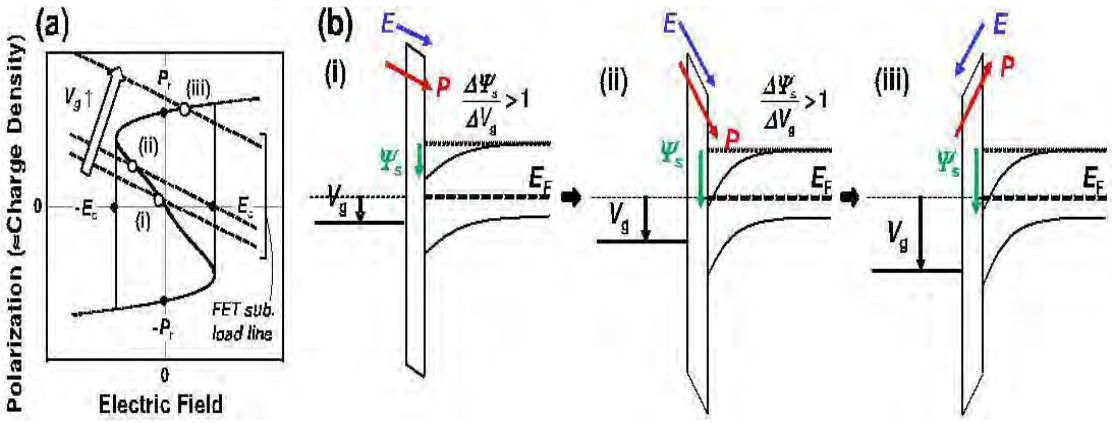


Figure 2.2.1: (a) shows the ferroelectric polarization (P), electric field (E) characteristics and channel charge as a function of Vg. (b) shows the band diagram corresponding to the operation points of (a) [15].

In the ferroelectric MOS capacitor, the ferroelectric polarization charge density and the channel charge density should match. Therefore, a static operation point of the NCFET is determined by the cross-point of the P-E curve and the channel charge load line. The negative capacitance region is where the slope of the P-E curve is negative. If these two curves have a single cross-point in the negative capacitance region, the ferroelectric MOS transistor works as NCFET. The operation principle of NCFET can be also qualitatively understood from the band diagram of NCFET. From the *Figure 2.2.1(b)*(i) as Vg is applied, a negative oxide field is induced on the gate insulator in the NCFET as opposed to the conventional MOSFET. As Vg is increased the operation point moves to (ii) in *Figure2.2.1 (a)*, and the negative oxide field becomes even larger. The silicon band bends more than applied Vg, that is $\Delta\psi_s$ /ΔVg>1 as shown in Figure 2.2.1 (b-ii). This means that the surface potential is effectively amplified against Vg, more channel charges are induced and thus higher current is driven in the NCFET than in conventional MOSFETs. As Vg is even further increased, the operation point moves to (iii) in Figure 2.2.1(a) and the oxide field flips and the band diagram looks same as conventional MOSFETs as shown in Figure 2.2.1(b-iii).

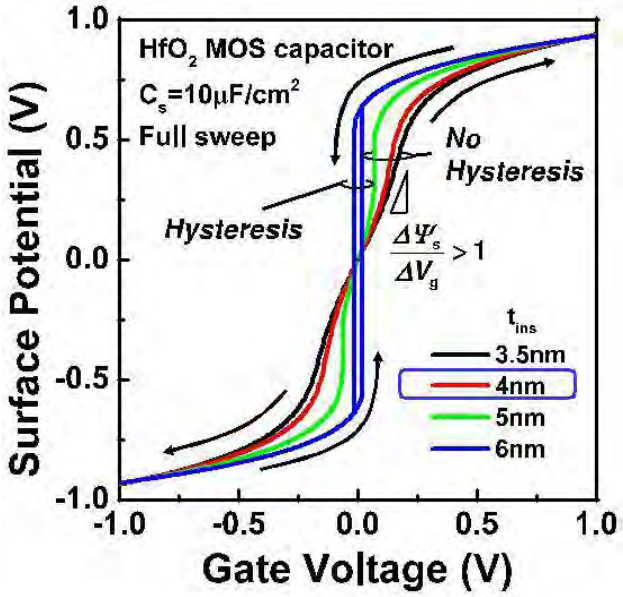


Figure 2.2.2: ψ_s vs. Vg characteristics of the ferroelectric MOS capacitor as a function of the ferroelectric thickness. Vg is swept in both directions, from negative to positive and vice versa. 4nm is chosen as a reference parameter. [16]

However, the hysteresis of ferroelectric capacitor can be avoided as it is dependent on the thickness of the ferroelectric. For the reference material parameters, to find static operation points, the thickness dependence of ψ_s – Vg characteristics of MOS capacitor of the NCFET with ferroelectric positive voltage and vice versa. ψ_s is certainly amplified without hysteresis in the thickness range of 3-5nm. This is an encouraging result because the thickness of the ferroelectric is just a few nm. Moreover only 0.2V Vg is required to amplify ψ_s which enables low supply voltage operation. It should be noted that if the thickness is too thick, the static operation point is not properly set and the ψ_s vs. Vg curve shows hysteresis [16].

Despite hysteresis, negative capacitance FET seems to have a good potential to work below the SS limit. For negative capacitance, $\frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_S}{C_{OX}}$ which can be less than 1 if C_{OX} is negative [9].

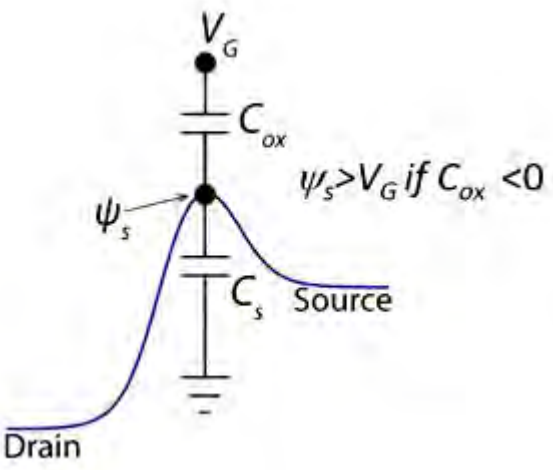


Figure 2.2.3: Equivalent circuit of an NCFET showing different capacitances.

For negative capacitance C_{OX} is negative which can result in SS less than 60mV/decade breaking the theoretical limit of MOSFET.

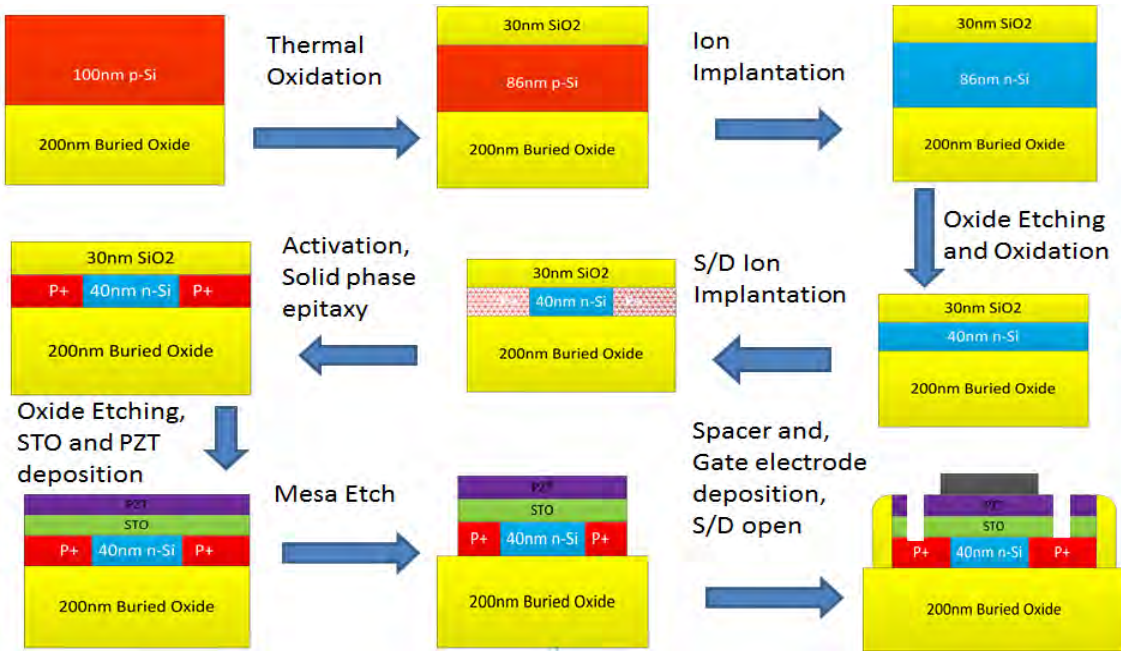


Figure2.2.4: Process flow of negative capacitance FET fabrication [22]

Figure 2.2.4: The fabrication steps of a negative capacitance field effect transistor [22]

The fabrication process of an NCFET is a long process. At first the source and drain doping and activation are done [22]. The high thermal steps are done before gate stack to minimize damage. Therefore, an SOI wafer is thinned down to desirable thickness by using dry thermal oxidation and DHF etching. Active area is defined by patterning dry etching. After that a thermal oxide is grown to remove the defects caused by etching. Then the thermal oxide is removed by DHF and the wafer is immediately loaded into a furnace to grow a good quality thermal oxide. Next, the wafer is patterned followed by source/drain ion implementation and RTA (Rapid Thermal Annealing) is used to activate dopants. Then blanket STO buffer is deposited using Molecular Beam Epitaxy (MBE) where native oxide removal is also done. Then the wafer is cut into 10mm by 10mm dies and another blanked layer of PLD PZT ferroelectric is deposited. Finally, the gate metal is deposited by ebeam deposition and the source/drain contact is etched using a combination of dry and wet etch process.

2.3 Literature Review

Though ferroelectricity was 1st noticed in 1920s, the concept of negative capacitance in a ferroelectric material is not very old. R. A. McKee, F. J. Walker, M. F. Chisholm proposed that if an increased capacitance beyond classical limit is obtained, it can generate novel super capacitance structures [17]. In 2008, S. Salahuddin et al. first published that using negative differential capacitance as gate insulator in MOSFET, the SS can be lowered below the fundamental limit [14]. Later A. I. Khan with his fellow researches demonstrated the effect of negative capacitance in a nanoscale ferroelectric dielectric heterostructure on 2011 [18]. They used a bilayer of ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$and dielectric $SrTiO_3$. In the same year, A. I. Khan, C. W. Yeung, C. Hu and S. Salahuddin proposed a new mode of NCFET operation named antiferroelectric mode [19]. Though it had hysteresis, it achieves sub-60mV/decade sub-threshold swing and boosts the on current. They showed that controlled hysteresis is designable through simulation.

In 2012, C. W. Yeung et al. achieved sub-30mV/decade SS in non-hysteretic NCFETusing body profile engineering [9]. They have gained28.3mV/decade SS for six orders of magnitudewhen I_{OFF}=10pA/μm, I_{ON}=0.3mA/μm at V_{DD}=0.3V at LG=100nm (without strain mobility enhancement). They said that the performance will be improved in shorter gate length on mobility enhancement. They proposed a thin T_{TSOC} layer design to get this result that also makes C_{DEP} large and insensitive to gate bias.

In the next year in 2013, C. W. Yeung with his colleagues proposed a new concept with ultra-thin body transistor to suppress the short channel effects that also reduces the power loss significantly [20]. They used TCAD simulation to show NCFET works best in ultra-thin body using a 1nm Si body as example (without considering mobility enhancement by strain). This non-hysteretic NCFET can achieve I_{ON}=250A/μm at 0.3V V_{DD}, I_{OFF}=10pA/μm and 21mV/decade swing from 10pA to 10μA per micron.

N. Chowdhury, S. M. Azad, Q. D. M. Khoshru from Bangladesh University of Engineering and Technology modified the structure of TFET incorporating ferroelectric oxide as the complementary gate dielectric operating in negative capacitance zone in 2014 [21]. They called it Negative Capacitance Tunnel FET (NCTFET). They also provided a simple analytical tunnel current model of NCTFET that demonstrates on high ON current at low V_{GS} with lower ss. The important part to notice here is that this device has all the improved

characteristics that can be achieved without sacrificing commercially well-matured silicone substrate.

Another important step for the negative capacitance trend happened in 2014 which is the first fabrication of pNCFET. According to the thesis work by C. W. Yeung and his colleagues, they fabricated a SOI MOSFET with PZT and STO deposition [22]. They found the swing of almost 100mV/decade as they fabricated the device with very low gate leakage. Unfortunately, when they attempted different temperature to get I-V measurement, the thin gate compact pad (almost 100nm Au) was damaged and they were not able to conduct any further annealing experiment.

In 2015 A. I. Khan reported a method for direct measurement of negative capacitance in an isolated ferroelectric capacitor [23] with his colleagues. This was an important achievement. Because measuring negative capacitance in practical was a challenge until that time. They have also introduced two new fundamental concepts in negative capacitance called the characteristic negative capacitance transients and the dynamic hysteresis loop. In this report, they established the theoretical concept of negative capacitance experimentally. In the same year C. Hu et al. simulated first negative capacitance FinFET [24]. Through this simulation they showed 0.2V operation with 0.6mA/μm on current and 100pA/μm leakage current. This experiment confirmed NC-FinFET also shows high performance and very low power dissipation (low leakage of 0.2V V_{DD} is obtained).

In the year of 2016 a good number of researches have conducted regarding negative capacitance. Such as; S. Khandelwal et al. presented a model of NC FinFET where they extracted the values of parameters. However, the effects of trapped charges were not included [25]. After that a spice compatible model for NC-FinFETs device was published but it did not have the implications of ferroelectric parameters on device characteristics [26]. In 2017 they published another work with enhanced model for NC-FinFET including the effects they ignored in their previous work of 2016 though simulation [27]. However, in 2016 A. I. Khan also published a work on the change in charge balance if the ferroelectric material is leaky [28]. They theoretically studied this with Landau-Khalatnikov description of ferroelectric dynamics in presence of an intermediate metallic layer between the ferroelectric and dielectric material.

A direct measurement of negative capacitance in polycrystalline HfO_2 based thin film was presented for 18nm and 27nm thin Gd:HfO_2 capacitor in series with an external resistor [29]

in 2016. In the same year NC UTB-DG-TFET was also proposed with a simulation model by C. Lie et al. [30].

In 2017, X. Li et al. designed a nonvolatile NCFET D flip-flop (DFF) that maintains its state during power outrage [31]. They also fabricated an NCFET that shows hysteresis edges less than 10mV/decade up to seven orders of magnitude. Their device is energy efficient and has an ultralow energy delay overhead (below 2.1%) in normal operations. In the same year, a simple model of NCFET with monolayer MoS2 as channel material is proposed by Z. Dong and J. Guo [32]. They showed a simulation model that treats 2-D electrostatic effects and quantitative agreement with numerical device simulation describing the DIBL and Negative Output Differential conductance effects (NDC) for scaled down NC MOSFET. They contacted an ultrathin quantum metallic layer to the source and with that they got a significant improvement in DIBL and NDC.

Later, to be published in Solid-State Electronics, Volume 136, Pages 1-120, October 2017 which is based on the selected papers from ISDRS 2016, K. Jang et al. stated that the energy efficiency and scalability of ferroelectric HfO_2 based NCFET with GAA nanowire channel structure has five times higher I_{ON}/I_{OFF} ratio than classical nanowire MOSFET and 2 times higher than DG NCFET based on analytic simulation [33]. Among the other works of 2017, experimentally demonstrated ferroelectric HfZrOx (FE-HZO) NCFET with high temperature annealing (hysteresis free) by M. H. Lee et al [34], NC MoS_2FET incorporating with ferroelectric Al doped HfO_2 by A. Nourbakhsh et al. [35], comparative study on SS of UTB NCFET with Ge/Si channel showing high permittivity channel to be more suitable due to its high C_{CH} and GeOI NCFET to be better than Si by H. –P. Lee et al. [36]

CHAPTER 3

Development of Simulation Model

3.1 Silvaco Atlas

Silvaco is the short form of Silicon Valley Company which is considered as one of the pioneer vendor in technology computer aided design known as TCAD. It was established in 1984. Its head quarter is in Santa Clara, California, USA. A good number of CAD simulation tools has already been developed by Silvaco to aid in semiconductor process and device simulation. To assist in the broad area of semiconductor technologies, Silvaco has an extensive support team. The ability to accurately simulate a semiconductor device is somehow critical to industry and research arena. In Silvaco, the ATLAS 2010 version [37] device simulator is specially designed for 2d and 3d modelling with the ability to include electrical, optical and thermal properties within a semiconductor device. An integrated platform based on physics, is provided by ATLAS to analyze DC, AC and also time domain responses for all semiconductor based technologies.

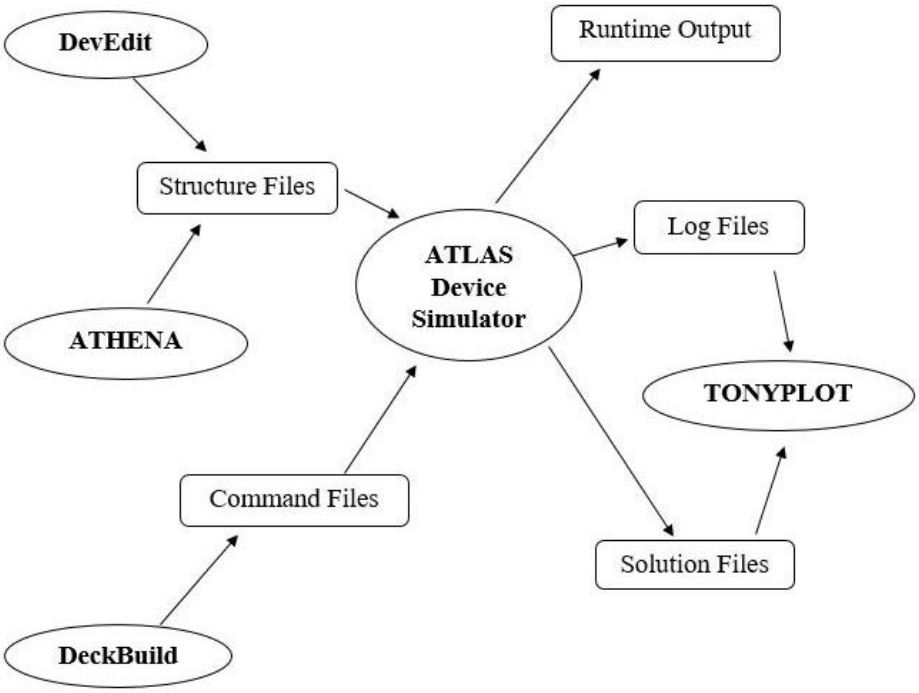


Figure 3.1: ATLAS Inputs and Outputs

The excellent input syntax always allows the user to design any semiconductor device of any size and design using both user-defined and standard material. There are a good number of examples in ATLAS to give assistance its user. DeckBuild is the run time environment used here in Silvaco ATLAS to input a command file or deck and it has got an extension of ‘‘.in’’.

In order to run the ATLAS in the DeckBuild, one must call the ATLAS simulator first. The command of calling ATLAS simulator is:

go atlas

ATHENA and DevEdit are two other simulation software which can be used with DeckBuild. Here in our work we have used Silvaco ATLAS only.

3.2 Commands in ATLAS

After calling ATLAS, a syntax structure is to follow so that the ATLAS could execute the command file successfully. Table shows the primary group list and their statement structure specifications. The basic format of the input file statement is:

<STATEMENT><PARAMETERS>=<VALUE>

There may be a few input exceptions. Here a point to be noted that the order of the statements is very important in ATLAS input file in order to run properly. The order that should be followed is given on table 4.1. In ATLAS, there are five groups of statements that must occur in the right order for simulation a device. They are:

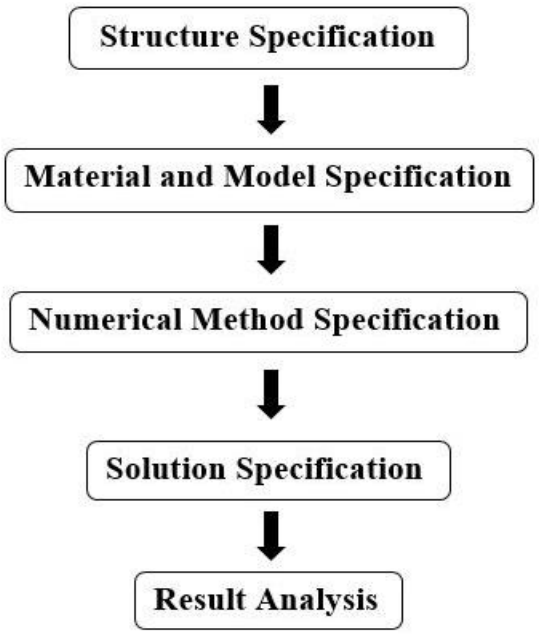


Table 3.1

Group	Statements
Structure Specification	MESH, REGION, ELECTRODE, DOPING
Material Models Specification	MATERIAL, MODEL, CONTACT, INTERFACE
Numerical Method Selection	METHOD
Solution Specification	LOG, SOLVE, LOAD, SAVE
Results Analysis	EXTRACT, TONYPLOT

Table 3.1: ATLAS command groups with primary statements in each group [38]

3.3 Model Development in ATLAS

3.3.1 Structure Specification

3.3.1.1 Meshing

The mesh statement is used to define the structure in an inverted 2D or 3D Cartesian grid. The x-axis is positive from left to right, the y-axis is negative from bottom to top. The reason for the inverted y-axis is that the manufacturing coordinates are usually described as depth below the surface. All coordinates are entered in microns and the spacing is used to refine the sharpness and accuracy at an assigned location. ATLAS producesa series of triangles to form the mesh based on the user input parameters. Meshing is done by this command:

The first statement:

MESH SPACE.MULT=<VALUE>

This is followed by a series of X.MESH and Y.MESH statements:

X.MESH LOCATION=<VALUE> SPACING=<VALUE>

Y.MESH LOCATION=<VALUE> SPACING=<VALUE>

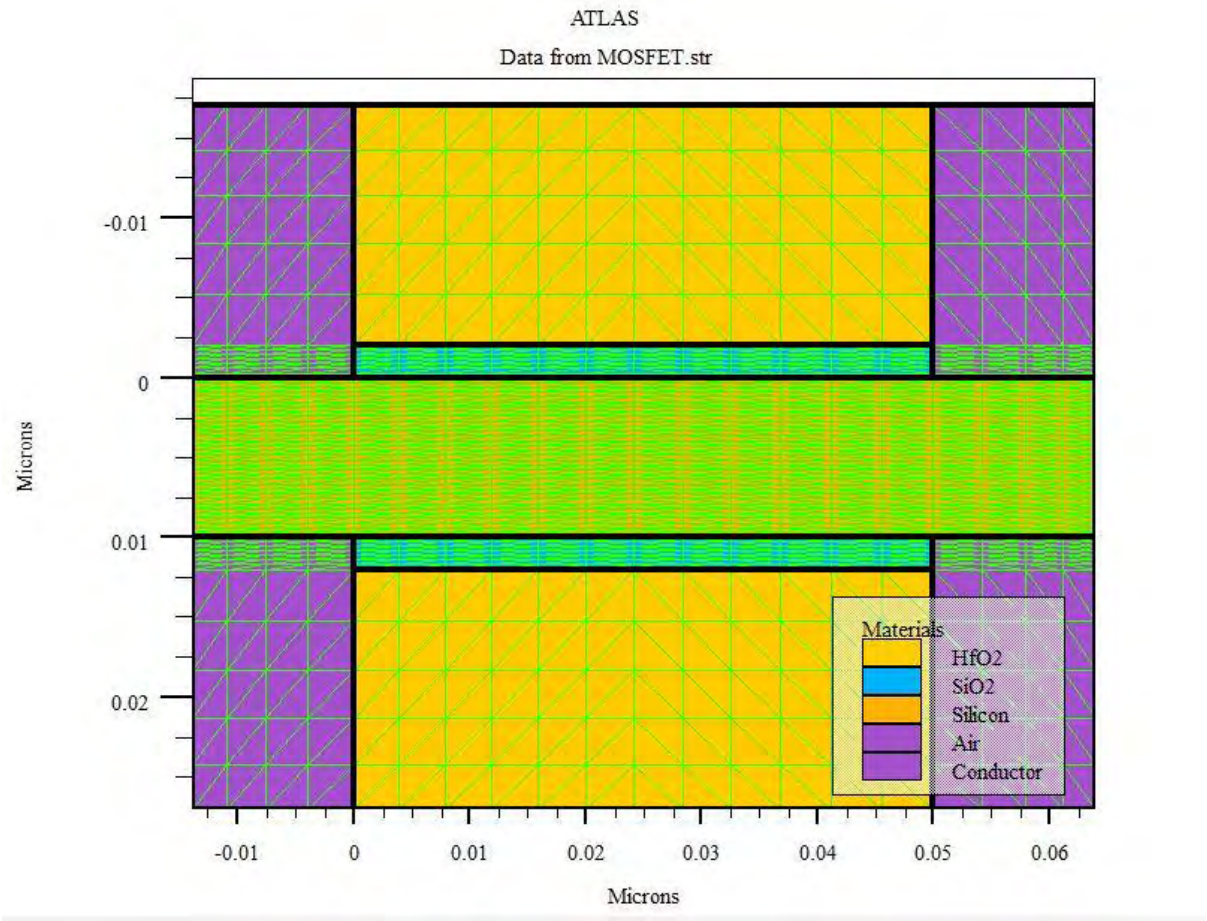


Figure3.3.1.1:Meshing of a semiconductor device

3.3.1.2 Regions

The region statement is used to separate the initial mesh statement into distinct blocks and sets the initial material parameters that can be referred to later by region number. All meshed areas of a structure must be assigned a region and the regions must be ordered from lowest to highest region. For instance, region 3 cannot be defined before region 2. The region command is:

REGION number=<integer><material_type><position parameters>

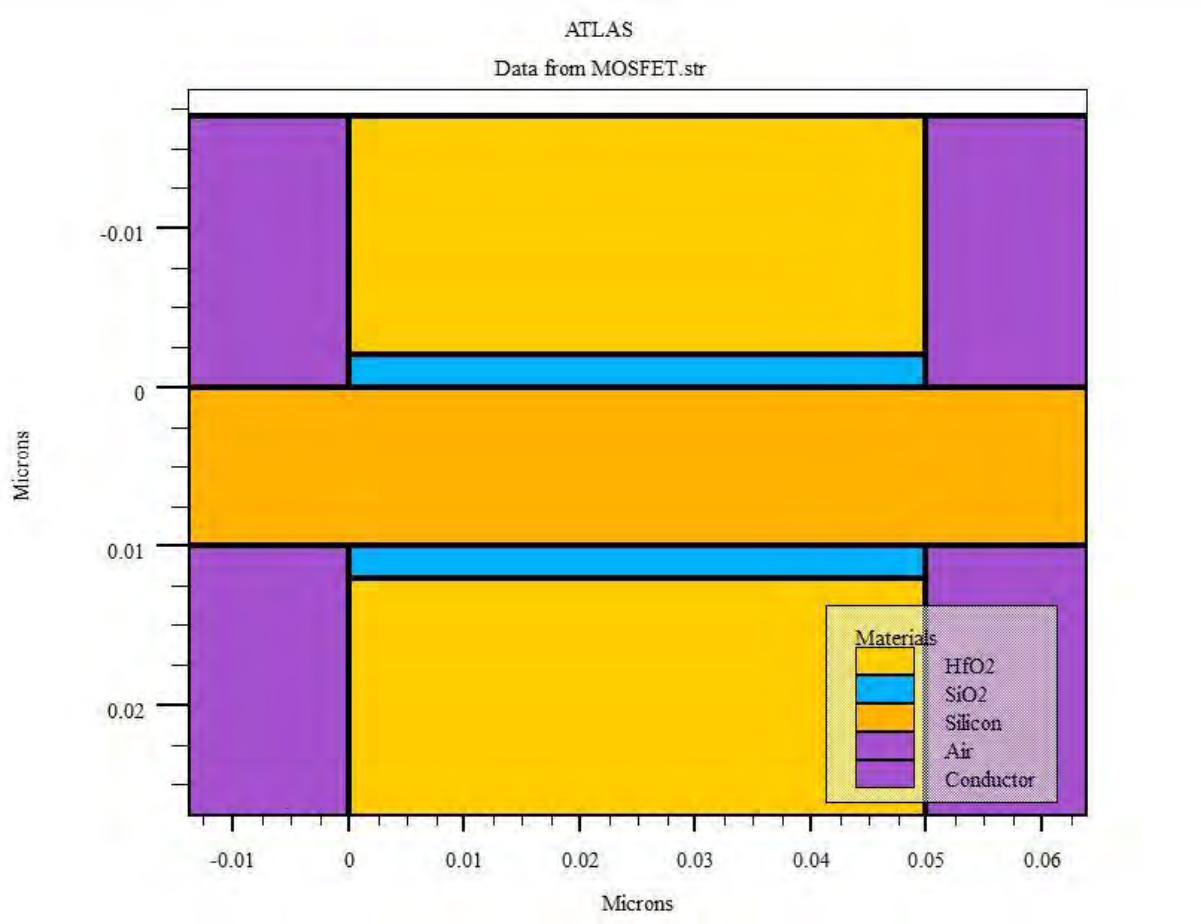


Figure3.3.1.2:Different regions of a semiconductor device

Region numbers must start at 1 and are increased for each subsequent region statement. We can have up to 15000 different regions in Atlas.

3.3.1.3 Electrode

Once the regions are set, the electrodes must be assigned to the desired region so that it can be electrically analysed. The electrodes can be assigned to any region or portion of a region. ATLAS has some fixed names for electrodes e.g. Anode, Cathode, Gate, Source, and Drain. The following statements were used to define these parameters:

ELECTRODE <position_parameters>NAME=<electrode name>

The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters. Multiple electrode statements may have the same electrode name. Nodes that are associated with the same electrode name are treated as being electrically connected.

3.3.1.4 Doping

The last required input of the structure specification is the doping statement. The doping statement is used to assign the doping level within the previously assigned regions. Various properties can be appended to the doping statement to specify how the semiconductor was doped and of whether the region is n or p type. The following statements were used to define doping parameters:

DOPING <distribution_type><dopant_type><position_parameters>

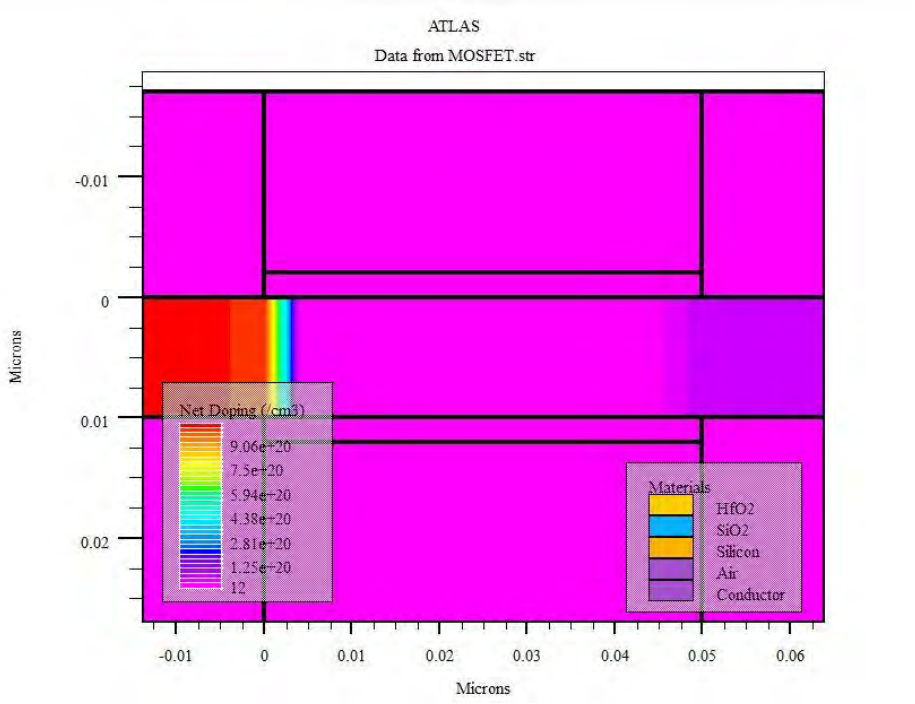


Figure 3.3.1.4: Doping in different regions in a semiconductor device

Analytical doping profiles can have uniform or Gaussian forms. The position parameters X.MIN, X.MAX, Y.MIN, and Y.MAX can be used instead of a region number. With the doping statement complete, the structure specifications are complete and it is possible to continue withthe simulation following the guidelines in Table 4.1. Unlike the structure specifications, the remaining four groups to be specified do not require all statements to run without error.

3.3.2 Material Model Specification

3.3.2.1 Material

The material statement relates physical parameters with the materials assigned to the mesh. The important material parameters for most standard semiconductors are already defined by ATLAS and therefore do not require any changes. We utilized the extensive model libraries

in ATLAS since the developed were based in HfO_2 which is very well researched and documented. For ferro-electric material, the material statement would be like this:

MODELS REGION=1 FERRO

MATERIAL REGION=1 FERRO.EPS=30.25 FERRO.PR=7.25e-6/

FERRO.PS=7.63e-6 FERRO.EC=1.05e6

For user defined materials, the statement is:

USER.MATERIAL=MATERIAL_NAME

3.3.2.2 Models

The models statement is essential to the accurate modelling of a particular phenomenon because it sets flags for ATLAS to indicate the inclusion of different mathematical models, physical mechanisms and other global parameters. The model statement used here is:

MODELS MOS PRINT

Here several models have been used:

Fermi-Dirac Carrier Statistics

Electrons in thermal equilibrium at temperature T with a semiconductor lattice obey the Fermi-Dirac statistics. That is the probability f (ε) that an available electron state with energy ε is occupied by an electron is:

$f(\varepsilon) = 1/(1+\exp(E-EF)/KT)$

Where EF is a spatially independent reference energy known as the Fermi level and k is Boltzmann constant. Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials. The 'FERMI' syntax enables this model in ATLAS.

Shockley-Read-Hall Model

Phonon transitions occur in the presence of a trap (or defect) within the forbidden gap of the semiconductor. This is essentially a two-step process, the theory of which was first derived by Shockley and Read [39] and then by Hall [40]. The Shockley-Read-Hall recombination is included in the device model using 'SRH' command.

Lombardi CVT Model

The inversion layer model from Lombardi [41] is selected by setting CVT on the MODELS statement. This model overrides any other mobility models which may be specified on the MODELS statement. In the CVT model, the transverse field, doping dependent and temperature dependent parts of the mobility are given by three components that are combined using Matthiessen's rule. These components are $\mu_{AC,}$ $\mu_{SR}$and $\mu_b$and are combined using Matthiessen's rule as follows:

$\mu_T{}^{-1}=\mu_{AC}{}^{-1}+ \mu_{SR}{}^{-1}+ \mu_b{}^{-1}$

3.3.2.3 Contact

CONTACT statement used for shorting the two gates. These can be also done by naming the two electrodes. Two gates are shorted by this statement for double gate structure.

CONTACT NAME=<contact_name> COMMON=<contact_name>

In ATLAS, an electrode in contact with semiconductor material is assumed by default to be ohmic. If a work function is defined, the electrode is treated as a Schottky contact. The 'CONTACT' statement is used to specify the metal work- function of one or more electrodes. In this case, workfunction of gate metal is set to 4.4eV. It is possible in ATLAS to tie two or more contact together so that voltages on both contacts are equal.

3.3.3 Numerical Method Selection

Several different numerical methods can be used for calculating the solutions to semiconductor device problems. Numerical methods are given in the 'METHOD' statements of the input file. For each of the model types, there are basically three types of solution techniques:

(a) GUMMEL: Decoupled

(b) NEWTON: Fully Coupled

(c) BLOCK

3.3.3.1 GUMMEL METHOD

The GUMMEL method will solve for each unknown in turn keeping the other variables constant, repeating the process until a stable solution is achieved. Usually, the GUMMEL method is useful where the system of equations is weakly coupled but has only linear convergence.

3.3.3.2 NEWTON METHOD

The NEWTON method solves the total system of unknowns together. The NEWTON method is useful when the system of equations is strongly coupled and has quadratic convergence. The NEWTON method may, however, spend extra time solving for quantities, which are essentially constant or weakly coupled. NEWTON method also requires a more accurate initial guess to the problem to obtain convergence.

3.3.3.3 BLOCL METHOD

The BLOCK methods will solve some equations fully coupled while others are de-coupled.

3.3.3.4 SUMMARY

GUMMEL can often provide better initial guesses to problems. It can be useful to start a solution with a few GUMMEL iterations to generate a better guess. Then, switch to NEWTON to complete the solution. In this work this techniques has been applied to find the electrical characteristics of the NCFET device.

The command line for this:
METHOD GUMMEL NEWTON TRAP MAXTRAP=20

3.3.4 Solution Specification

ATLAS can calculate DC, smallAC signal, and transient solutions. Obtaining solutions is similar to setting up parametric test equipment for device tests. User usually defines the voltages on each of the electrodes in the device. ATLAS then calculates the current through each electrode. ATLAS also calculates internal quantities, such as carrier concentrations and electric fields throughout the device. In all simulations, the device starts with zero bias on all electrodes. Solutions are obtained by stepping the biases on electrodes from this initial equilibrium condition. Due to the initial guess strategy, voltage step sizes are limited. In DC solutions, the voltage on each electrode is specified using the 'SOLVE'. In ATLAS, when the voltage on any electrode is not specified in a given SOLVE statement, the value from the last SOLVE statement is assumed. To obtain convergence for the equations used, a good initial guess should be supplied for the variables to be evaluated at each bias point. The ATLAS solver uses this initial guess and iterates to a converged solution. If a reasonable grid is used,

almost all convergence problems in ATLAS are caused by a poor initial guess to the solution. During a bias ramp, the initial guess for any bias point is provided by a projection of the two previous results. Problems tend to appear near the beginning of the ramp when two previous results are not available. If one previous bias is available, it is used alone. Generally, the projection method for the initial guess gives good results when the I-V curve is linear. But it may encounter problems if the I-V curve is highly non-linear or if the device operating mode is changing. Typically, this may occur around the threshold or breakdown voltages. At these biases, smaller voltage steps are required to obtain convergence.

3.3.4.1 Output

Several quantities are saved by default within a structure file. For example, doping, electron concentration, and potential. We specified additional quantities such as conduction band potential, valence band, potential by using the OUTPUT statement.

OUTPUT CON.BAND VAL.BAND

3.3.4.2 Run Time Output

Run-time output is provided at the bottom of the DeckBuild Window. If it runs as a batch job, the run-time output can be stored to a file. If someone specifies the 'PRINT' option within the MODELS statement, the details of material parameters and constants and mobility models will be specified at the start of the run-time output. This is a useful way of checking what parameters values and models are being applied in the simulation. After achieving convergence, ATLAS lists the results by electrode. One column lists the voltage at the contact surface. This will differ from the applied voltage if external resistors or the curve tracer are used. All relevant current components are listed. Electron, hole, conduction and total currents are also found in simulation.

Log Files

Log files store the terminal characteristics calculated by ATLAS. These are current and voltages for each electrode in DC simulations. Terminal characteristics from all SOLVE statements after the LOG statement are then saved to this file along with any results from the PROBE statement. Typically, a separate log file should be used for each bias sweep. Then those files are overlaid in TonyPlot. Log files contain only the terminal characteristics. They are typically viewed in TonyPlot. Parameter extraction of data in log files can be done in

DeckBuild. Log files cannot be loaded into ATLAS to re-initialize the simulation. In TonyPlot, unit of current is Amperes per micron. This is because ATLAS is a two-dimensional simulator. It sets the third dimension to be one micron.

The log/solve/save statements are used to create data files in ATLAS simulations. These statements work together to be provide data to be analysed by other functions. Here we used these statements to analyse drain current with respect to gate voltage or drain voltage.The LOG statement allows all terminal characteristics generated by a solve statement to be saved to a file.

Solve

The SOLVE statement specifies which bias points are to be applied to produce an output. The bias points can be set in a number of different way including step, initial and lambda depending on what stimulus is desired.

Save

The SAVE statement is used to save all node point data into an output file. A common use of the LOG/SOLVE/SAVE statements for the device is like this:

LOG OUTF=Id_vs._Vgs.log

SOLVE VGATE=-2 VFINAL=2 VSTEP=0.05 NAME=GATE

Here the log file has been set aside to store data from the solve statements and then saved so that the data can be called at a later time. The solve statements simply sweep the voltage from -2V to 2V in varying voltage steps depending on the degree of accuracy at the desired range. With the date stored in an out file, it is ready to be displayed so that it can be analysed.

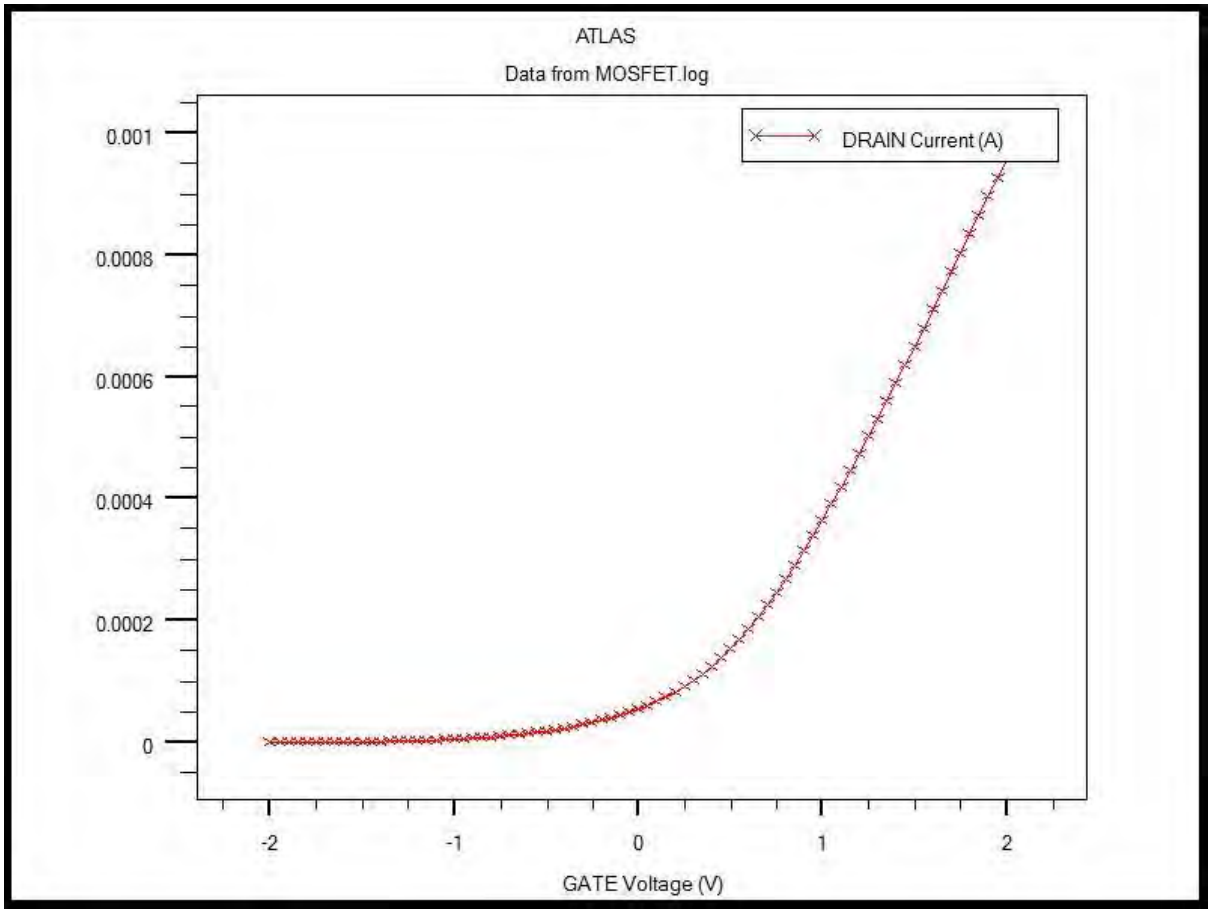


Figure 3.3.4.1:I_D-Vgs Curve of a semiconductor device

3.3.5 Result Analysis

3.3.5.1 Solution Files

Solution files or structure files provide an image of the device at a particular bias point (DC solution or transient solution point). This gives someone the ability to view any evaluated quantity within the device structure in question, from doping profiles and band parameters to electron concentrations and electric fields. These files should be plotted using TonyPlot. Some quantities saved in the solution files are not evaluated at the node points during solutions. They are evaluated at the centre of the sides of each triangle in the mesh. Values of quantities at each node are derived from averaging the values from the sides of triangles connected to that node. The weighting method used to do the averaging can be selected with

options in the OUTPUT statement. It is possible that for some meshes, smoother contour plots can be obtained by choosing a non-default averaging method.

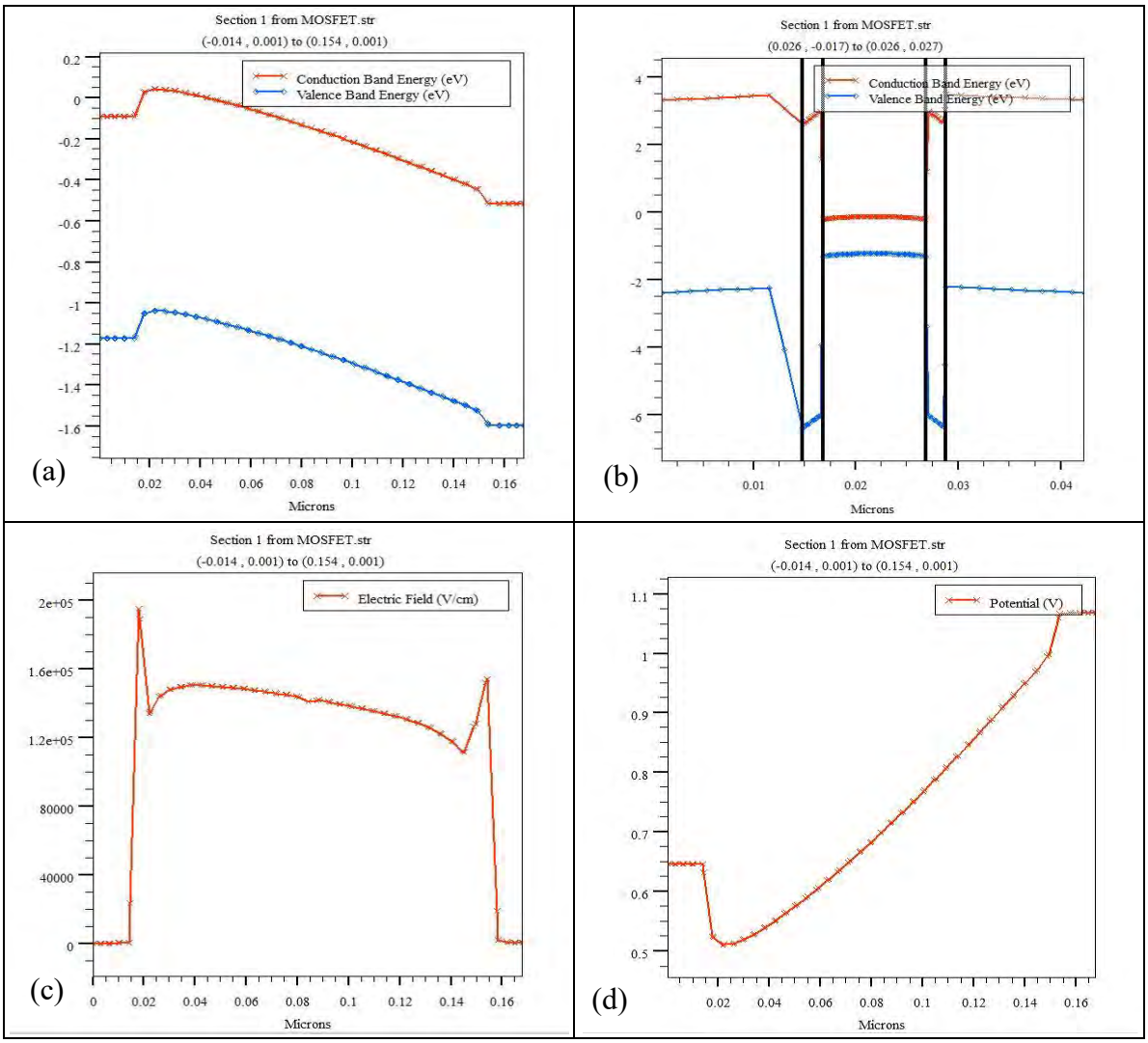


Figure 3.3.5.1: (a) Conduction and valance band energy along the channel

(b) Conduction and valance band energy perpendicular to the channel

(c) Electric field along the channel

(d) Potential variation from the source to drain terminal

3.3.5.2 TONYPLOT

The TONYPLOT statement is used to start the graphical post-processor tool.When interpreting the contour plots, it's important to remember that the solution file contains values only at each node point. The colour fills seen in TonyPlot are simply interpolations based on the node values. The primary solution variables (potential, carrier concentration etc.) are calculated on the nodes of the ATLAS mesh. Therefore, they are always correct in TonyPlot. But since ATLAS doesn't use nodal values of quantities, such as electric field and mobility, the actual values used in calculations cannot be determined from TonyPlot or the structure files. The PROBE statement allows to directly probe values at given locations in the structure. This provides the most accurate way to determine the actual values used in ATLAS calculations.

Chapter 4

Result and Discussion

4.1 Si doped HfO_2 as Ferro-Electric Material

4.1.1 Advantages and Disadvantages of HfO_2 as Ferro-Electric Material

In search of a new steep slope transistor to overthrow the classical limit of 60mV/decade, Salahuddin [42] came with the idea of negative capacitance field effect transistor which has the same structure of a normal MOSFET and the only difference in building criteria is to replace the gate insulator oxide with thin film of ferroelectric material. The nonlinear characteristic of ferroelectric material which is known as negative capacitance plays a vital role to exceed the value of $\partial\psi s/\partial Vg$ more than 1. While in non-equilibrium, a ferroelectric material can show negative differential capacitance due to its energy barrier that actually forms during the phase transition and separates the two degenerate polarization states. Though the state of negative capacitance is unstable, by using a series die-electric capacitor the negative differential capacitance state can be stabilized. It may be noted that negative capacitance has already been experimented on thin ferroelectric film [43] which surely indicates a new way in the semiconductor industry. It is well known that the mechanism that works behind electron transport system in MOSFET is drift and diffusion and these very same technique also works as the working principle in negative capacitance MOSFET. NCFET can drive higher current than tunnel FET due to its higher charge density on the interface which works as an amplifier in the same off-current. Actually ferroelectric material works as a 'transformer' to boost up the input voltage. As a result, NCFET can successfully exceed the drive current of conventional MOSFET as well as it can surely overcome the limit of 60mV/decade. Moreover it is interesting to note that pass-gate CMOS circuits which actually flow the electricity in both ways between drain and source and standard pull-up and pull-down CMOS logic circuits both can be built by negative capacitance FET. So there is no reason to hugely modify the logic circuit architecture and IP macro design from the conventional MOSFET as it will be simply replaced by the new NCFET.

NCFET got significant impact on semiconductor industry yet it has got some limitations too. The main barrier comes on the process of integration. In order to balance the large

polarization charge density and FET charge density, the thickness of the insulator layer needs to be more than hundreds nanometer in case of traditional ferroelectric material such as Lead Zirconate Titanate and Barium Titanate. And here comes the real challenge as those are not compatible to advanced scale complementary MOS (CMOS) frond-end technologies. In addition to that, heavy metal contamination to the manufacturing line is also a big issue here in this case.

In recent study, by controlling crystalline phase of thin films of Hafnium Oxide, ferreoelectricity has been observed in HFO_2. By using 28 nanometer CMOS technology, thin films of Hafnium Oxide has already been implemented in Ferroelectric Random Access Memory (FeRAM) successfully [44]. Thereafter if the ferroelectric thin film of Hafnium Oxide is used in NCFET, the fabrication process will fully compatible with CMOS technology. Just by introducing ferroelectric HfO_2 gate insulator NCFET can be fabricated by any CMOS technology from the mature to most advanced technology.

4.2 Numerical Modeling

NCFETs are implemented by adding a ferroelectric material layer in the gate stack of MOSFETs. A lower SS is achieved in NCFETs with the help of "negative capacitance" which is contributed by the deposited ferroelectric layer. Ferroelectrics are materials with a high polarizability while ferroelectric capacitors tend to exhibit nonlinear capacitance, where the change in voltage produces a negative change in polarizability. The free energy of ferroelectric is represented by the Laundu Theory and the electrostatic dynamics of this negative capacitance can also be well described by LK (Landau-Khalatnikov) equation:

$$\rho \frac{d\vec{P}}{dt} + \nabla_i U = 0 \tag{1}$$

Where, ρ is material dependent parameter that accounts for dissipative process during the ferro electric switching, P is the polarization charge in per unit area and U is the Gibbs free energy. We can express it in terms of anisotropy energy:

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - \vec{E}_{ext}\vec{P} \tag{2}$$

Here the energy due to the external field is $\vec{E}_{ext}$ and α, β and γ are the material dependent parameters. In general at 0 bias the U vs P graph looks like a W like the one in Fig. 4.2.1 which tilts due to increase in Vg. From equation (1) and (2) we can write that:

$$E_{ext} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt} \tag{3}$$

here the vector signs have been dropped assuming the spatial variations to be one-dimensional. It is easy to see that if we set, at steady state operation dP/dt≈ 0 and for FE material P ≈ Q while the external electric field is Eext = V/t_{ins} them taking all these into consideration and mingling (2) and (3) we get

$$V = 2\alpha t_{ins} Q + 4\beta t_{ins} Q^3 + 6\gamma t_{ins} Q^5 \tag{4}$$

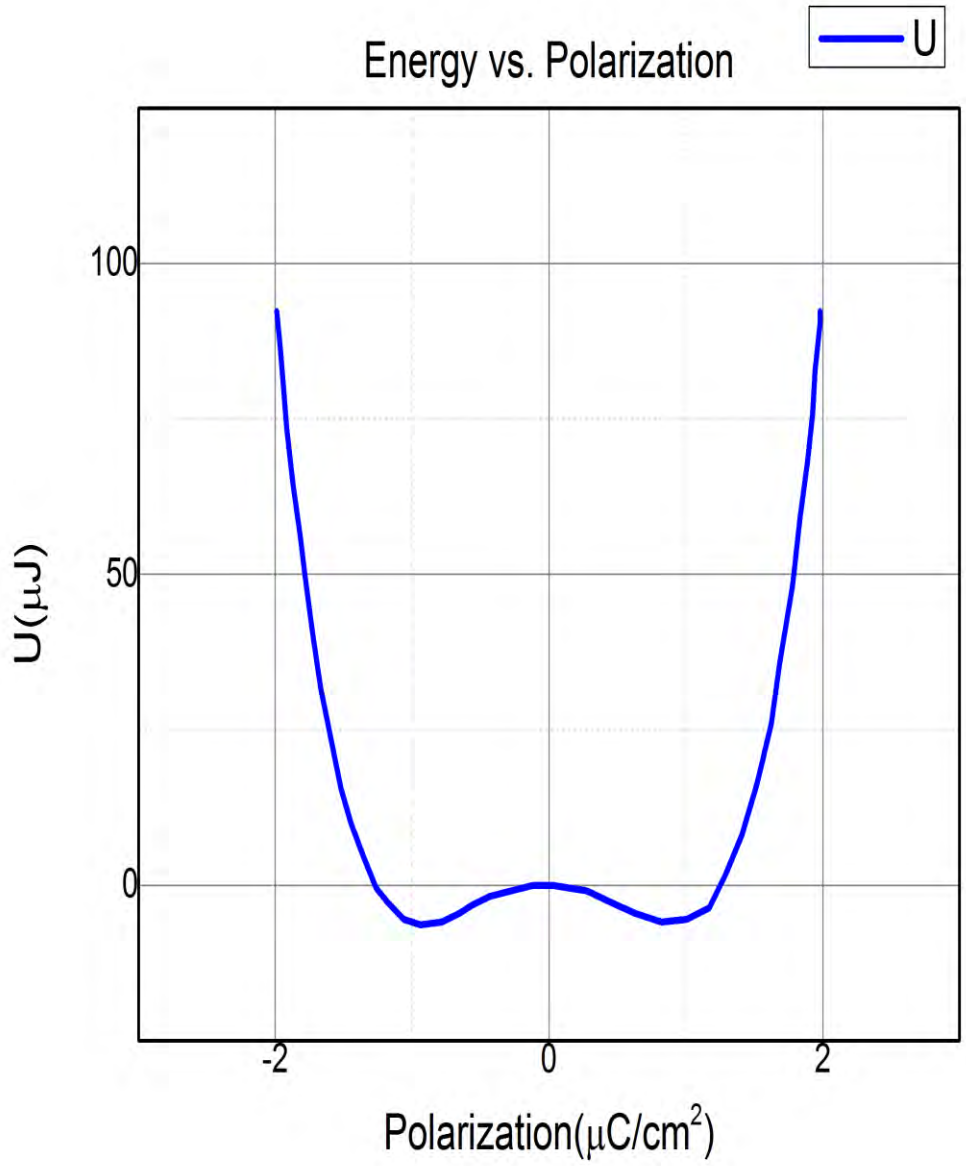


Figure 4.2.1: Energy vs. Polarization

where, t_{ins} is the FE insulator thickness and α, β and γ are the material dependent parameters. For, HfO_2 the values of these parameters are -1.5877 x 10^{11} m/F, 9.8007 x 10^{20} $m^5/F/Coul^2$ and 0 $m^9/F/Coul^4$ respectively. The plot of the steady-state polarization P versus E_{ext} and V vs P are shown in Fig. 4.2.2 and 4.2.3 were obtained from equation (3) and (4) respectively.

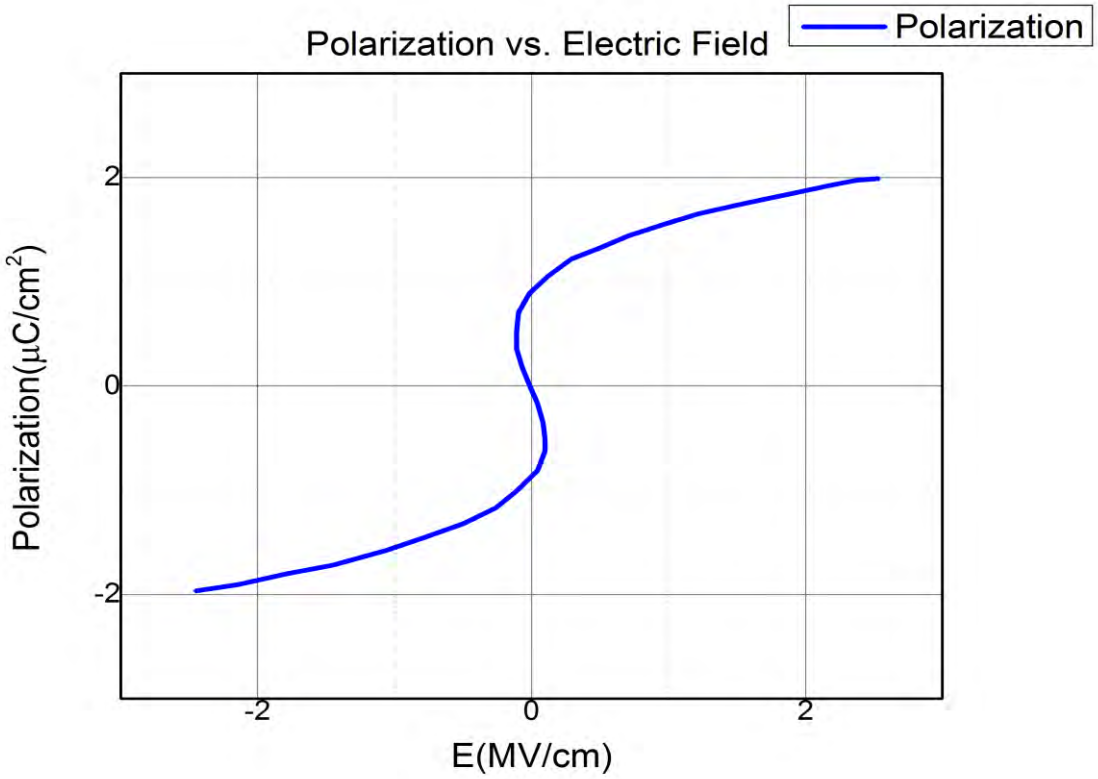


Figure 4.2.2: Polarization vs. Electric Field

We will consider that the FET has a ferroelectric insulator rather than an ordinary insulator at the gate. So the gate circuit can be assumed to be a series combination of the ferroelectric capacitor and another capacitor that we will call Cs, representing semiconductor, channel-to-source and channel-to-drain capacitances. For this series combination, a voltage ψ_s appears across Cs, while the rest $Vg - \psi_s$ appears across the ferroelectric such that both have the same charge Q and we can write

$$\psi_s = Q/C_S \tag{5}$$

$$Vg - \psi_s \approx \alpha_O Q + \beta_O Q^3 + \gamma_O Q^5 + \rho_O \frac{dQ}{dt} \tag{6}$$

Considering α_O=$2\alpha t_{ins}$

β_O=$4\beta t_{ins}$

γ_O=$6\gamma t_{ins}$

Reconsidering equation (3) and by combining these expressions, we can relate the applied voltage Vg to the potential ψ_s that appears inside the channel:

$$\tau \frac{d\psi_s}{dt} + (1 + a_1)\psi_s + a_2{\psi_s}^3 + a_3{\psi_s}^5 = Vg \qquad (7)$$

Here we are considering,

$\tau = \rho C_S t_{ins}$

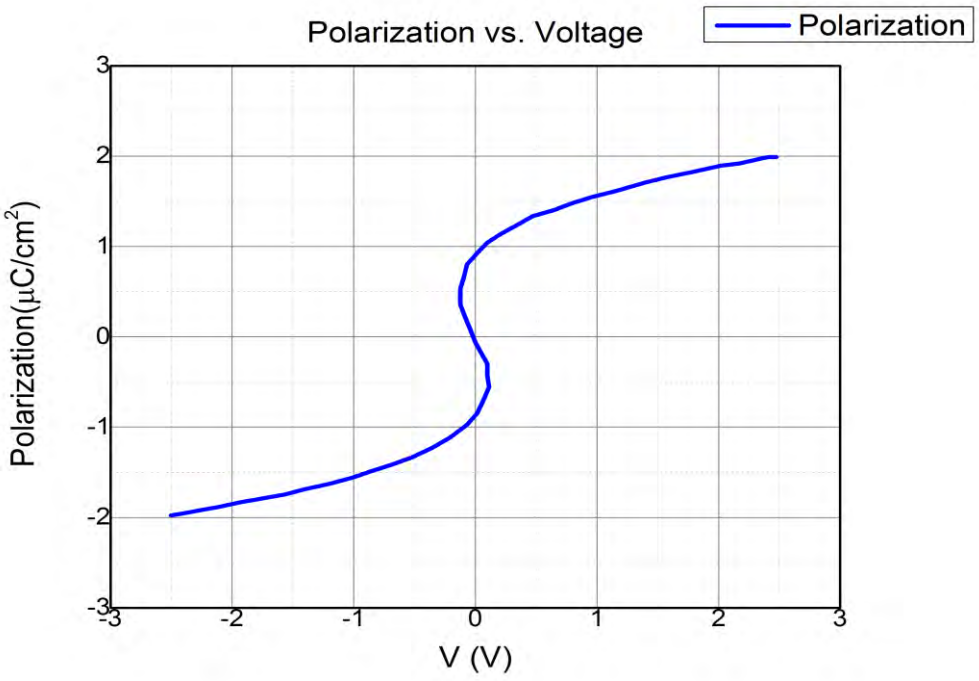


Figure 4.2.3: Polarization vs. Oxide Voltage

$$a_1 = 2\alpha C_S t_{ins}$$

$$a_2 = 4\beta {C_S}^3 t_{ins}$$

$$a_3 = 6\gamma {C_S}^5 t_{ins}$$

By setting $d\psi s/dt = 0$, the steady-state ψ_s versus Vg is obtained from equation 7 which is

$$(1 + a_1)\psi_s + a_2{\psi_s}^3 + a_3{\psi_s}^5 = Vg \tag{8}$$

There is no doubt that the nature of the ψ_s vs Vg characteristics will very much depend on the three co-efficients a_1, a_2, and a_3 which are scaled versions of the material parameters α, β and γ. If the parameter values are such that the nonlinear terms a_2 and a_3 are very small compared to a_1, which only ensures the relation between ψ_s and Vg is linear

$$\partial Vg/(\partial\psi_s) \approx 1 + a_1 \tag{9}$$

This is nothing but exactly same as $\frac{\partial Vg}{\partial \psi_s} = 1 - \frac{Cs}{Co}\,(\alpha_f\, C_o - 1)$ which represents the negative capacitance while it seems that we are neglecting the nonlinear terms. But the point to be noted that even though a_2 and a_3 are non-negligible, $(1 + a_1)$ represents the slope close to the origin $\psi_s = 0$ and $Vg = 0$ and should be positive if we wish the origin to represent a stable operating point. With the help of a_1, it is easy to find that the condition $(1 + a_1) > 0$ requires the thickness of the ferroelectric insulator to be less than a critical thickness defined as

$$t_{ins} \leq \frac{1}{2|\alpha|C_S} \equiv t_C \tag{10}$$

This condition ensures that the ferroelectric capacitor is large enough or the series capacitor Cs is small enough that the combination forms a stable positive capacitor, and there is no hysteresis at the origin unlike Figure 4.2.4, which corresponds to a very thin ferroelectric. All results we present below assume $t_{ins} < t_C$, because a hysteresis at the origin seems undesirable for our device applications.

Fig 4.2.4 shows ψ_s vs Vg for different values of t_{ins}, directly obtained from equation (8) using appropriate values of α, β and γ for HfO_2, in series with a linear capacitance Cs=25 x 10^{-7} F/cm^2. The plots are obtained starting from an initial state with the ferroelectric capacitor fully negatively polarized, sweeping the voltage toward the positive maxi-mum, and then sweeping it back again to the negative maximum. Each point is obtained by solving the full time dependent equation (1) and then finding ψ_s as the system reaches a steady state. Here also one thing may be noted that the insulator thicknesses we use are less than the critical thickness.

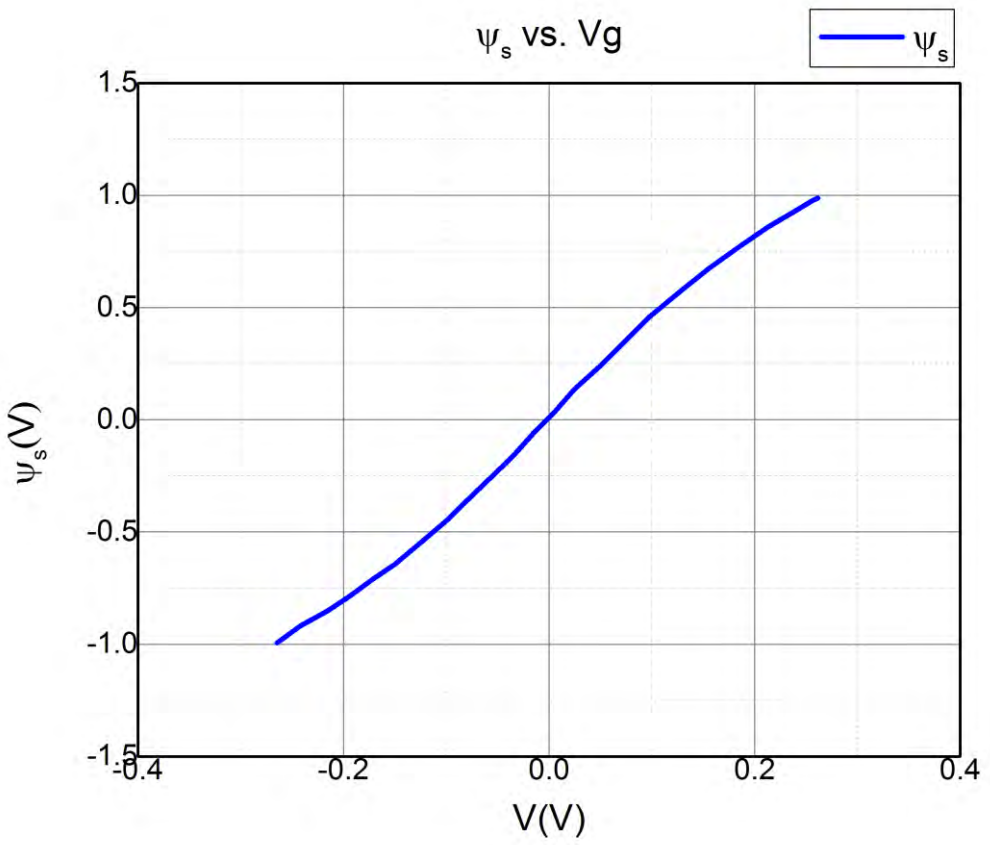
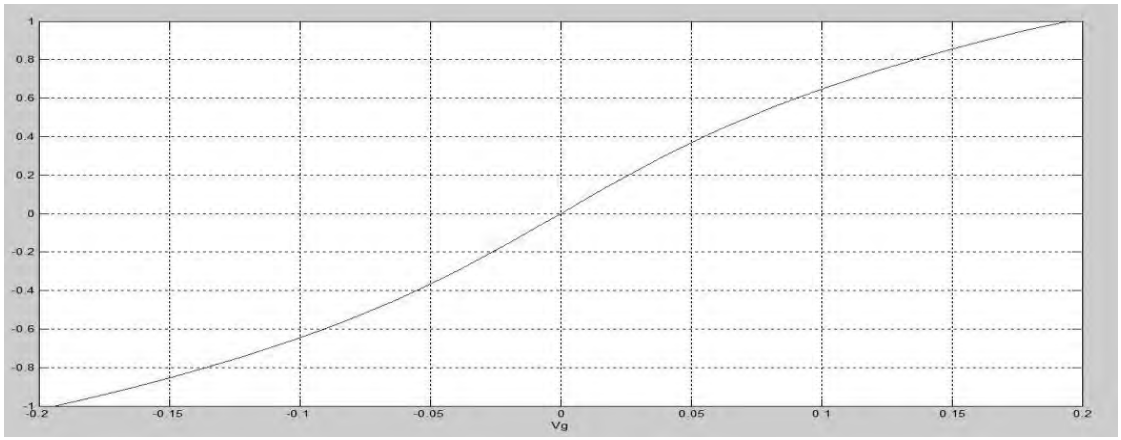
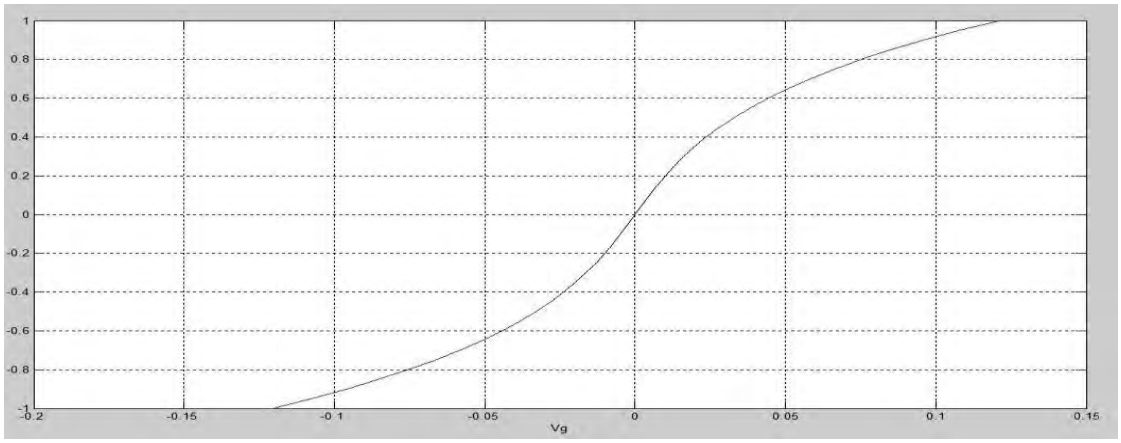


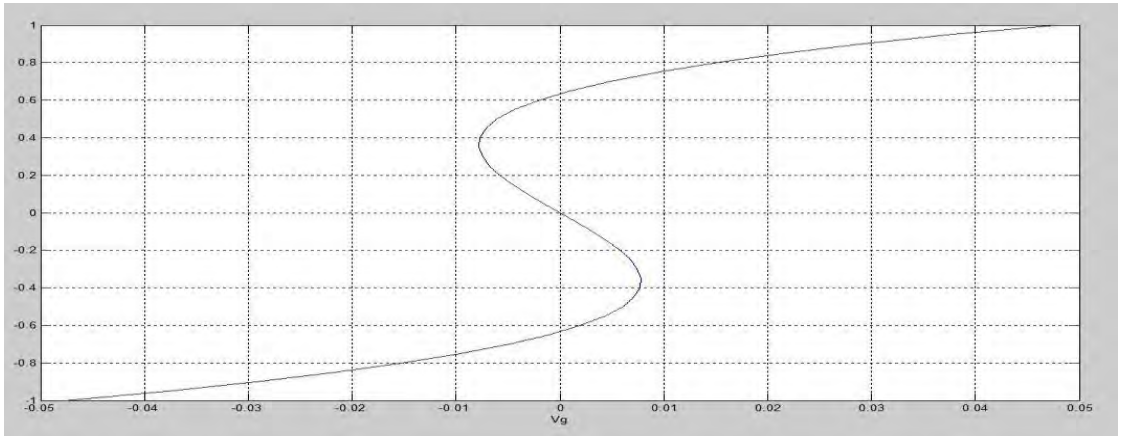
Figure 4.2.4: ψ_s vs Vg



(a)



(b)



(c)

Figure 4.2.5: Change in hysteresis with the change in thickness of the ferro-electric for

(a) 10 nm, (b) 11 nm and (c) 13 nm

As the insulator thickness is increased, the plots become progressively steeper but at the same time, they start to show more and more hysteresis away from the origin but not at the origin due to the nonlinear terms a_2 and a_3. Figure 4.2.5 (c) shows that with more insulator thickness there is a hysteresis in ψ_s vs Vg away from the origin, but it is small. In general, a trade off will take place between steepness and hysteresis, unless materials can be engineered to minimize the nonlinear term β relative to the linear term α so as to avoid hysteresis even at large steepness.

It will be noted from a_1 and a_2 and a_3 that if Cs were smaller, the nonlinear terms a_2 and a_3 would become smaller in com-parison to the linear term a_1 making the hysteresis negligible in our voltage range of interest. The value for Cs that we have used in this paper is more appropriate for ultra small FETs [45] where the short channel effects are significant. For a present day commercial device, the value of Cs should be roughly a factor of 10 lower than that used in this paper and as such should show steep ψ_s vs Vg with negligible hysteresis. However, because the critical thickness is in-versely proportional to Cs, the thickness of the ferroelectric insulator will have to be roughly a factor of 10 larger than those shown in Fig. 4.2.5.

The voltage amplification we are discussing here arises from an internal interaction commonly described by the Landau theory in terms of a free energy functional. Such interactions are quite general in metal oxides and commonly lead to the development of a spontaneous order parameter below a transition temperature. For example, the giant enhancement of longitudinal piezoelectric response recently modeled using the Landau-Ginzburg-Devonshire theory can be attributed to similar mechanisms, the precise correspondence between the effective field in the Landau approach in equation (3) and the effective voltage in a capacitor with positive feedback suggests that any microscopic mechanism that can provide the necessary positive feedback can be used to implement a step-up voltage transformer that would allow low-voltage/low-power operation of conventional FETs. For a ferroelectric capacitor, it is the dipole interaction that provides the positive feedback while avalanche breakdown, polaronic effect, etc. within the oxide can possibly provide the positive feedback needed for negative capacitance as well. The parameters α_O, β_O, γ_O and ρ_O will be determined by the specific mechanism involved.

4.3 Derivation of Anisotropy Constant Expressions

At steady state dP/dt≈ 0 and avoiding the higher term of P to ease the calculation, from equation (3) we get

$$E_{ext} = 2\alpha P + 4\beta P^3 \tag{11}$$

Again, Eext = V/t_{ins} and considering dV/dP=0 when P= -Pr we get

$$P_O = \sqrt{-\frac{\alpha}{6\beta}} \tag{12}$$

Now when E_{ext}= E_C then $P = -P_O$ and we get $\alpha = -\frac{3\sqrt{3}}{4}\frac{E_C}{P_O}$ (13)

And as $\alpha = -2\beta {P_O}^2$. So $\beta == -\frac{3\sqrt{3}}{8}\frac{E_C}{{P_o}^3}$ (14)

The α vs E graph is showed on Fig. 4.3.1 which is obviously linear with a negative slope while β vs E is also linear with a positive slope showed in Fig. 4.3.2. Again, α vs P got a reciprocal relation and. It is showed in Fig. 4.3.3 and β vs P is a cubic function graph showed in Fig. 4.3.4.

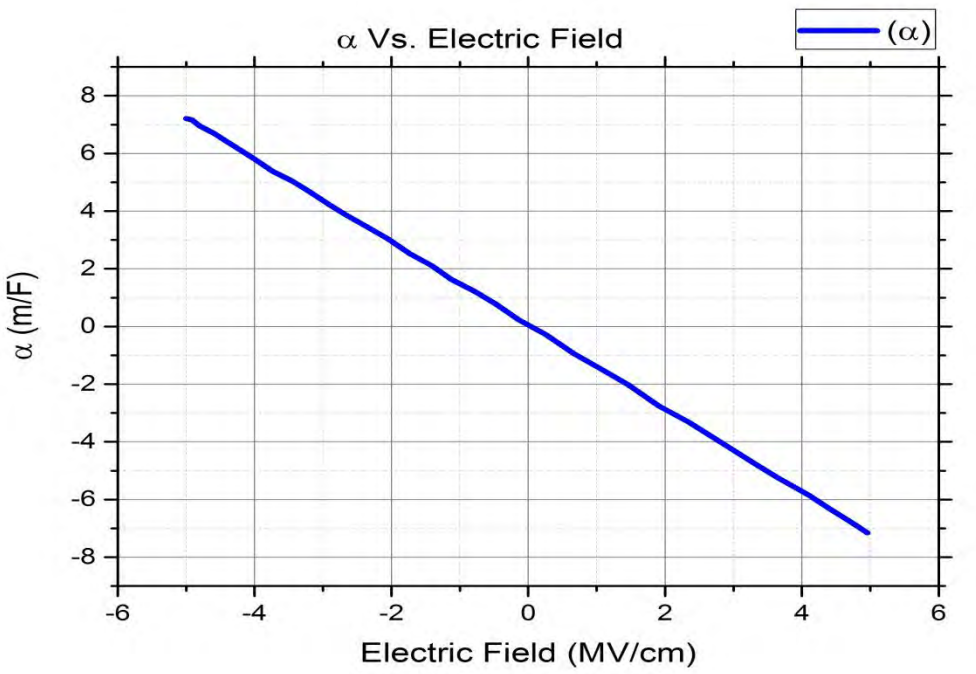


Figure 4.3.1: α vs Electric field

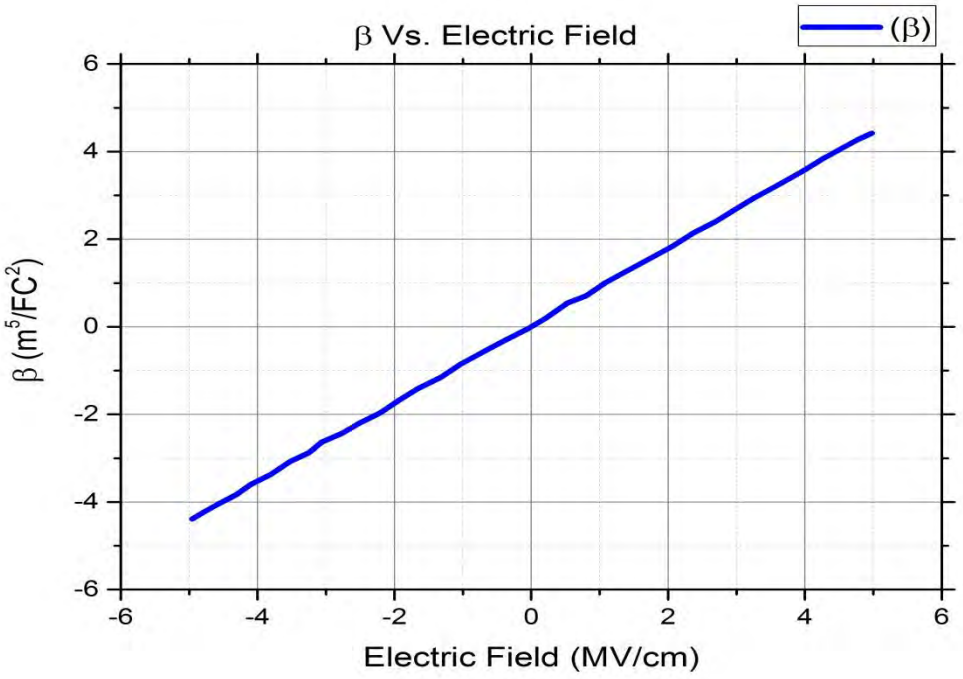


Figure 4.3.2: β vs Electric field

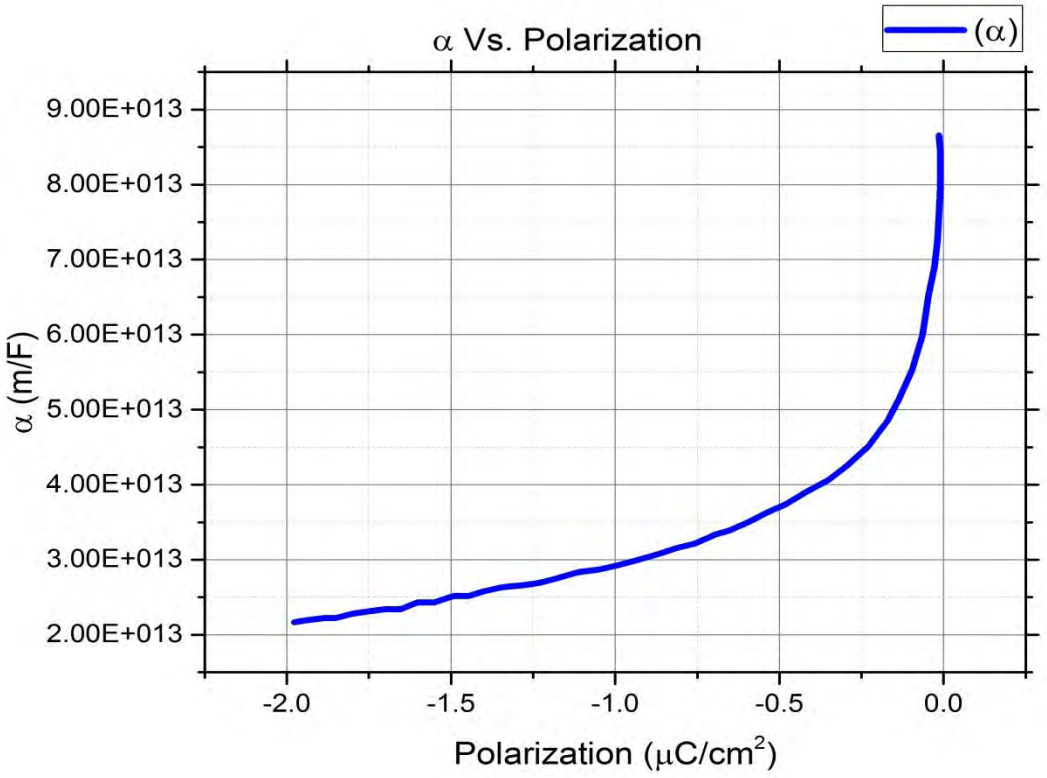


Figure 4.3.3: α vs Polarization

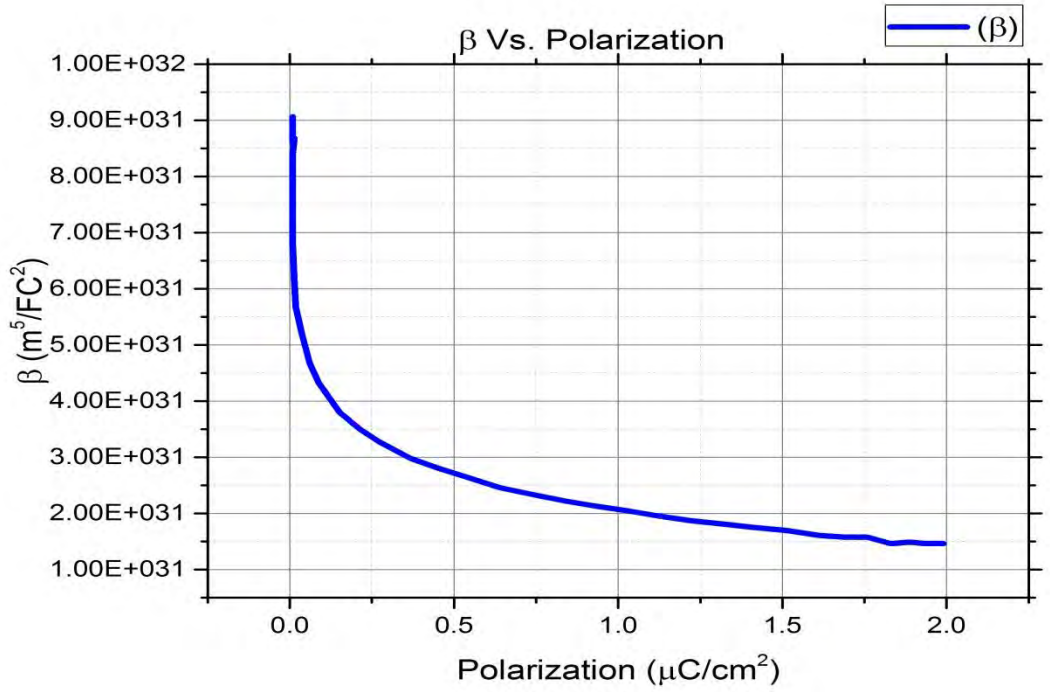


Figure 4.3.4: β vs Polarization

4.4 Permittivity Characteristics

Ferroelectric materials exhibit high dielectric constants, polarization and hysteresis. To simulate these effects, a modified version of the ferroelectric model from Miller has been implemented. To enable the Ferroelectric Model, we set the FERRO parameter in the MODELS statement. In this model the permittivity used in Poisson's Equation is given the following functional form:

$$\in (E) = FERRO.EPSF + FERRO.PS.2\delta.sech^2\left[\frac{E-FERRO.EC}{2\delta}\right] \quad (15)$$

where FERRO.EPSF is the permittivity, E is the electric field and δ is given as follows:

$$\delta = FERRO.EC[log\frac{1+FERRO.PR/FERRO.PS}{1-FERRO.PR/FERRO.PS}]^{-1} \quad (16)$$

The graph of ∈ vs. Electric field is shown on Fig. 4.3.5. At 0 electric field ∈ is maximum. The FERRO.EPSF, FERRO.PS, FERRO.PR, and FERRO.EC parameters can be modified in the MATERIAL statement which have been discussed in the previous chapter.

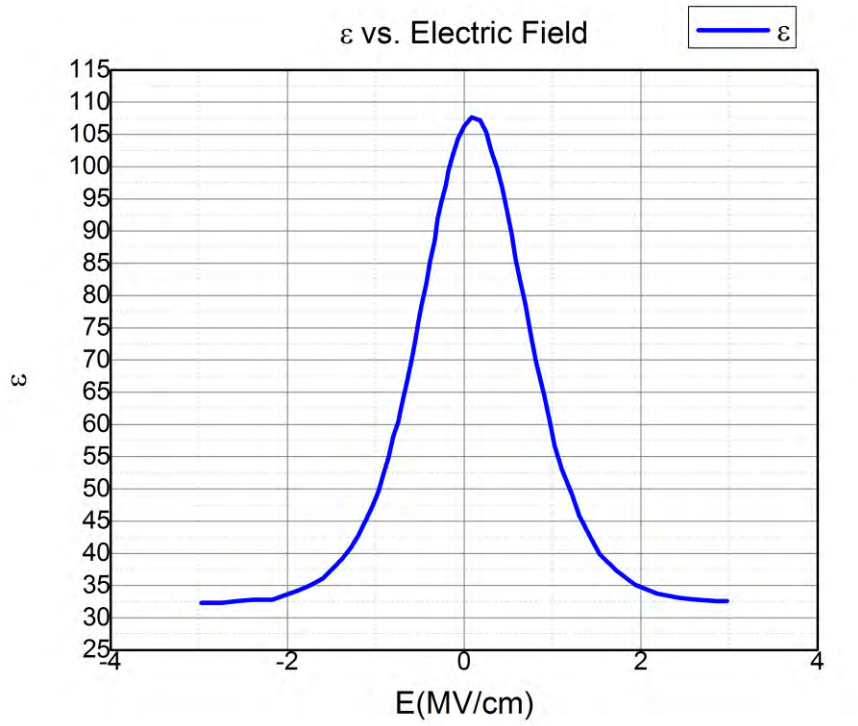


Figure 4.3.5: ε vs Electric field

Table 4.4 shows the permittivity characteristics of each thickness and the theoretical maximum memory window (MW max) that can be accomplished at each thickness. Permittivity characteristics of HfO_2 material have been measured by Stefan Mueller et al for 10 nm and 30 nm thicknesses. A calculator was developed to estimate these characteristics for any thickness

Permittivity characteristics of HfO_2 ferro-electric material for different thickness and the calculated maximum memory window values are given in the box below:

Table 4.4

Thickness of ferro-electric	Pr (μC/cm2)	Ps (μC/cm2)	Ec (MV/cm)	εf	tb (nm)	εb	MWmax=2Ectf
25 nm	**3.75**	**3.8787**	**0.95**	**26.75**	**0.8**	**25**	**4.75V**
20 nm	**5.5**	**5.7525**	**1**	**28.5**	**0.8**	**25**	**4V**
15 nm	**7.25**	**7.63**	**1.05**	**30.25**	**0.8**	**25**	**3.15V**
12 nm	**8.3**	**8.75**	**1.08**	**31.3**	**0.8**	**25**	**2.59V**
10 nm	**9**	**9.5**	**1.1**	**32**	**0.8**	**25**	**2.2V**
8 nm	**9.7**	**10.25**	**1.12**	**32.7**	**0.8**	**25**	**1.9V**

4.5 Negative Capacitance Region

Capacitance C at a given charge Q_F is related to the potential energy U by the relation $C = [\frac{d^2U}{dQ_F{}^2}]^{-1}$. The parabolic graph is in Fig. 4.5.1. So we can call the negative capacitance as negative differential capacitance. For a ferroelectric material, as shown in Fig. 4.5.2 (a), the capacitance is negative only in the barrier region around P=0 [Considering $Q_F \propto P$]. Starting

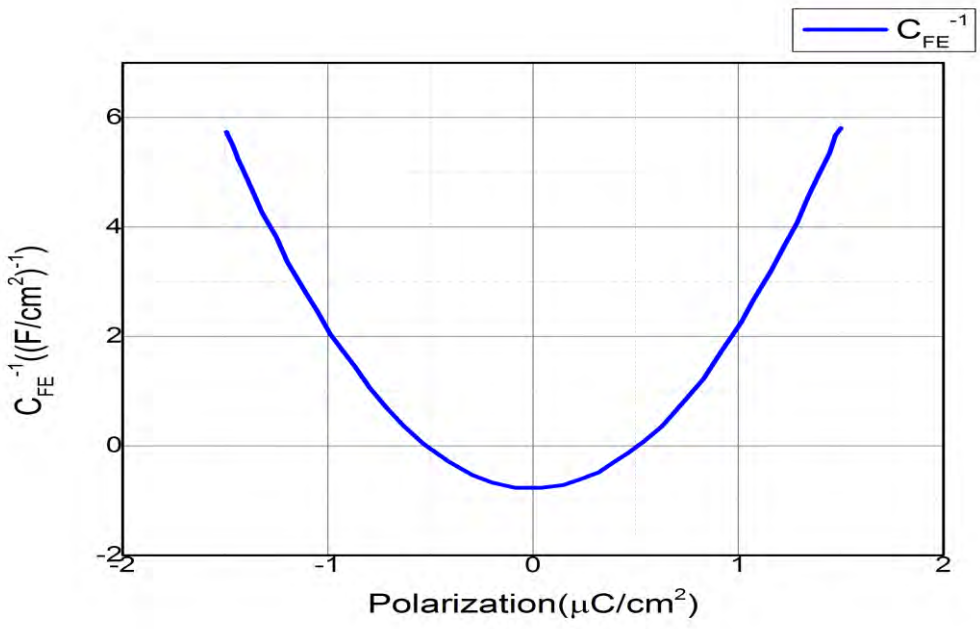


Figure 4.5.1: Capaitance^{-1} vs Polarization

from an initial state X, as voltage is applied across the ferroelectric capacitor, the energy landscape is tilted and the polarization will move to the nearest local minimum. Fig. 4.5.2 (a),

Fig. 4.5.2 (b) are the graph for less than the coercive voltage where as Fig. 4.5.2 (c), Fig. 4.5.2 (d), Fig. 4.5.2 (e) show this transition for a voltage that is greater than the coercive voltage Vc. If the voltage is larger than coercive voltage, one of the minima disappears and P moves to the remaining minimum of the energy landscape showed in the figure. Here may be noted that, as the polarization state descends, it passes through the region where $C = [\frac{d^2U}{dQ_F{}^2}]^{-1} < 0$. Therefore, while switching from one stable polarization to the other, a ferroelectric material passes through a region where the differential capacitance is negative. And this is the region where the device we are working on should work.

In case of P-E curve where the slope is negative we find the negative capacitance but it is unstable and not directly observed in experiments when it exhibits hysteric jumps in the polarization. Here is a solution for the unstable condition, if we place a ferro-electric capacitor series with a normal capacitor then the negative capacitance segment can be effectively stabilized. It is possible by making ψ_s on an internal node to change more than the voltage applied Vg externally working as a voltage amplifier aka step-up voltage transformer.

The structure of the device is shown in Fig. 4.1 is nothing but a bulk Si MOSFET with high K gate oxide is referred to as the intrinsic MOSFET. FE oxide is assumed to be deposited on a commensurate metallic template grown on the oxide. The intermediate metallic layer between the FE and the high-K gate oxide is chosen following the experimental device.

This layer averages out the non-uniform potential profile along the source-drain direction as well as any charge non-uniformity coming from domain formation in the Ferro-electric. This experimental structure therefore justifies using a 1-D Landau model for the Ferro-electric. The intrinsic MOSFET is simulated using TCAD Sentaurus software taking into account the 2-D electrostatics. NCFET with an MFIS structure cannot be simulated directly even with state-of-the-art device simulators such as Sentaurus and Silvaco TCADs, because of the lack of a corresponding accurate FE polarization model. In order to study the electrical performance of the NCFET, a metal-FE-metal-insulator-semiconductor (MFMIS) structure is used to approximate the MFIS structure, as shown in Fig.(). The suspended gate metal is assumed to have the same workfunction as the top gate metal, and there are no net charges on the suspended gate. It is obvious that for V_{ds} = 0 V or t_f = 0 nm, the MFMIS structure is completely reduced to the MFIS device and there are no errors for this approximation. Even though there are some reasonable errors (<10%) depending on specific circumstances for large Vds and tf values, the errors can be ignored for small Vds or tf values. And, the latter is

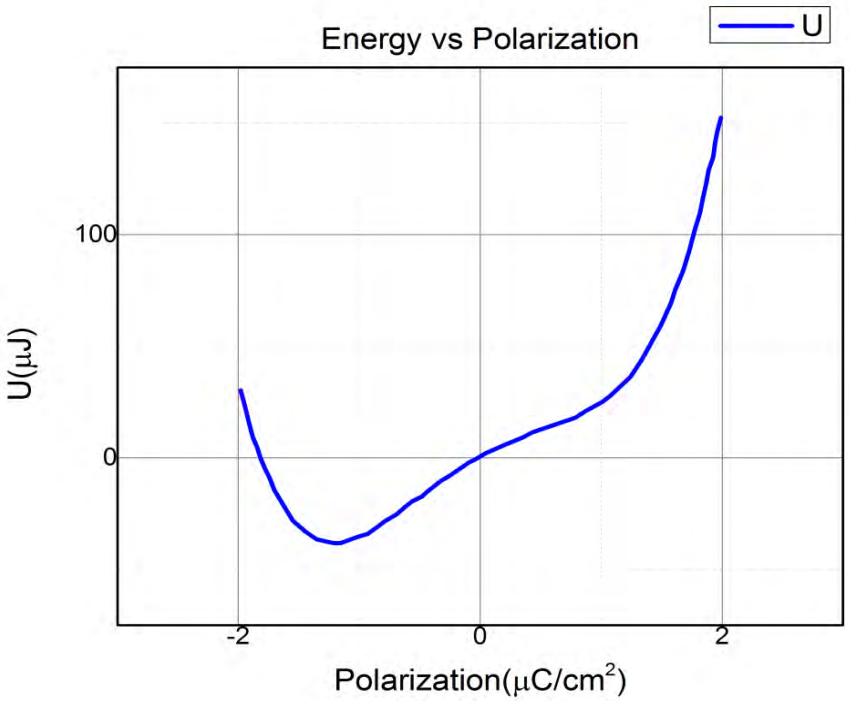


Fig. 4.5.2 (a): Energy vs Polarization curve at V_g= -6 V

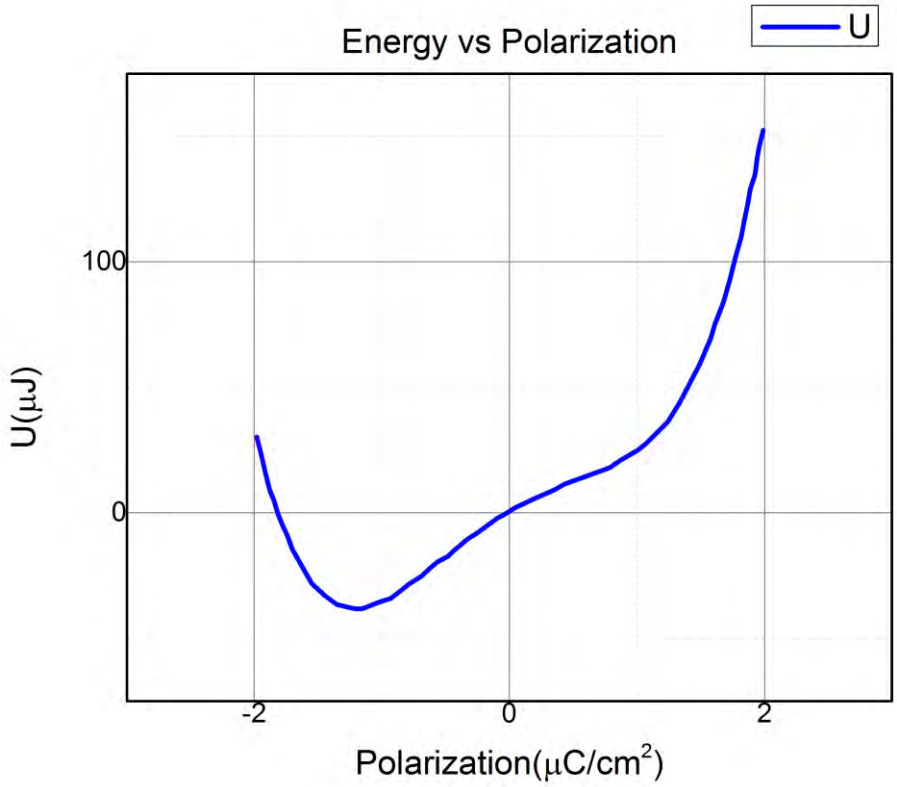


Fig. 4.5.2 (b): Energy vs Polarization curve at V_g = -3 V

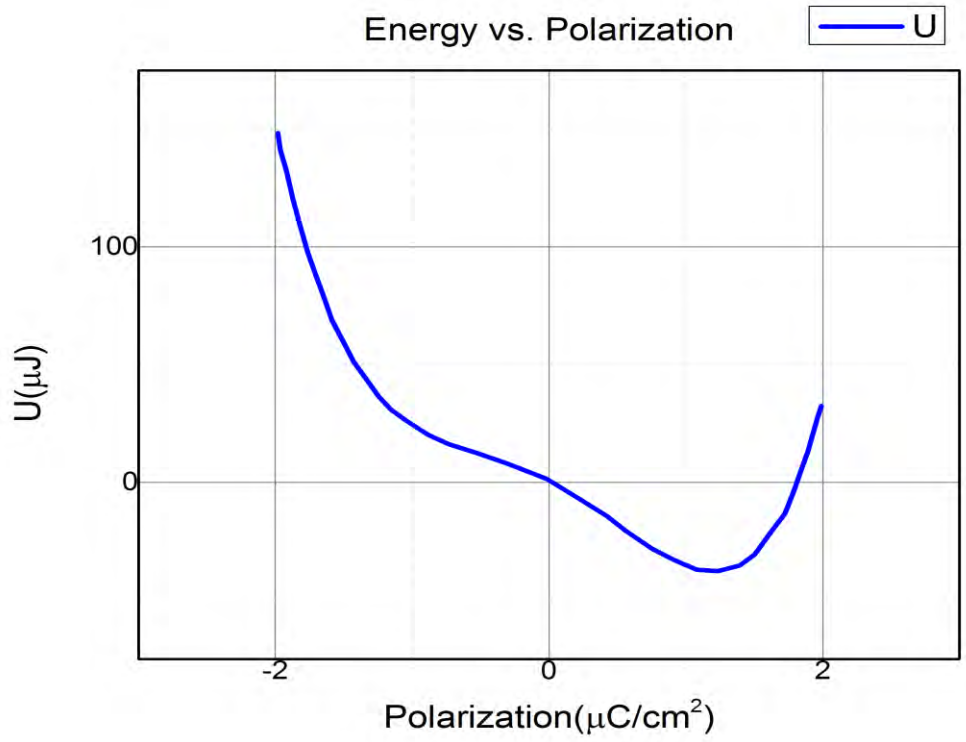


Fig. 4.5.2 (c): Energy vs Polarization curve at V_g = 3 V

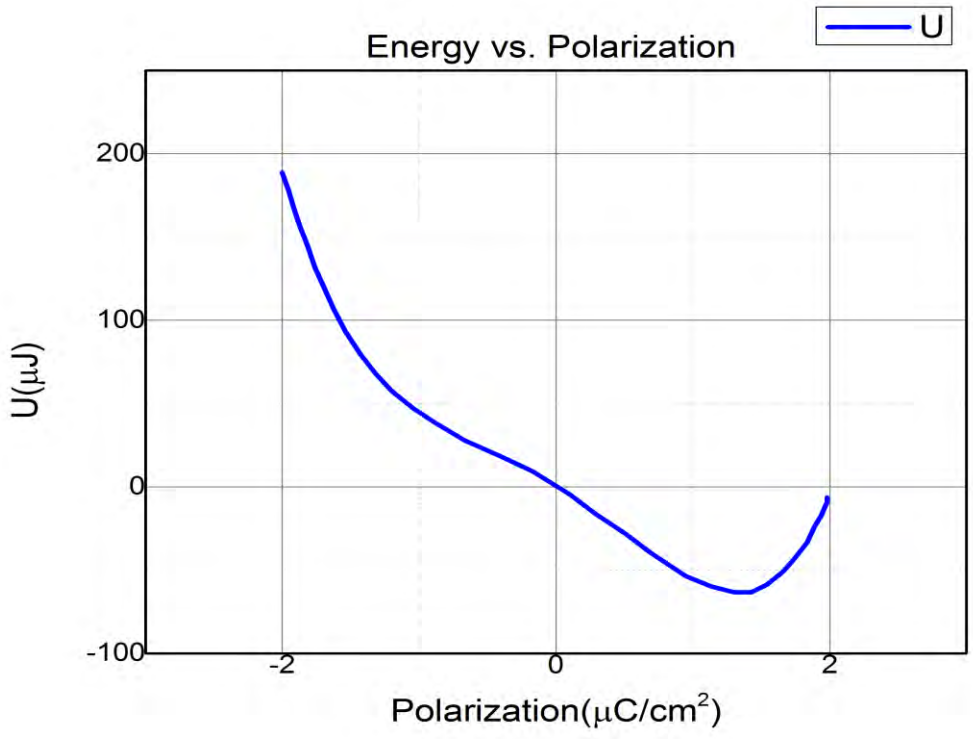


Fig. 4.5.2 (d): Energy vs Polarization curve at V_g = 5 V

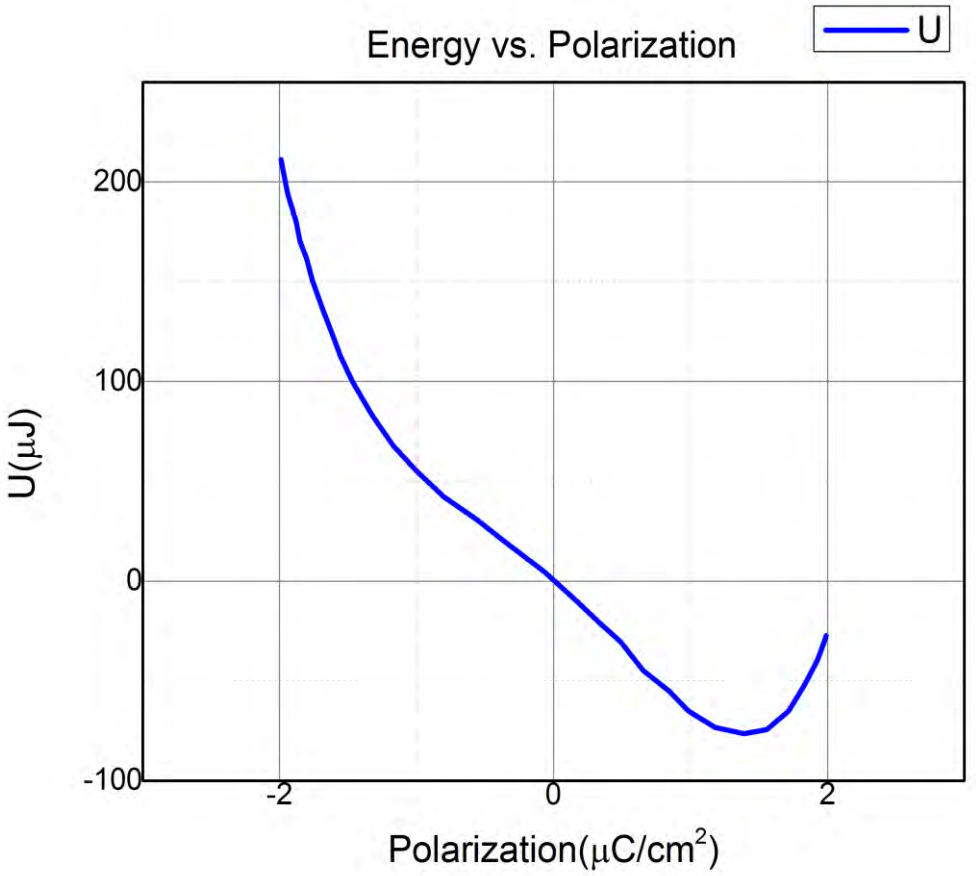


Fig. 4.5.2 (e): Energy vs Polarization curve at V_g = 6 V

the typical case (low power supply and ultrasmall dimension) of state-of the-art nano-scale devices being fabricated. Dynamic nonlocal path bandto-band model, standard Shockley-Reed-Hall recombination and drift-diffusion model are used and Fermi-Dirac statistics is assumed in the MOSFET simulation. This hybrid 2D electrostatics for MOSFET and 1-D Landau equations are solved self-consistently.

Negative capacitance regions are ordinarily unstable and not observed in experiments. But placing such a capacitor in series with a positive capacitor stabilizes it by making the effective α of the composite capacitor positive, provided its thickness is less than the critical thickness defined in equation (10). Because R is proportional to (T - Tc) with Tc being the Curie temperature, the series combination acts like a ferroelectric at a temperature above its Tc.

4.6 Device Model and Structural Parameters

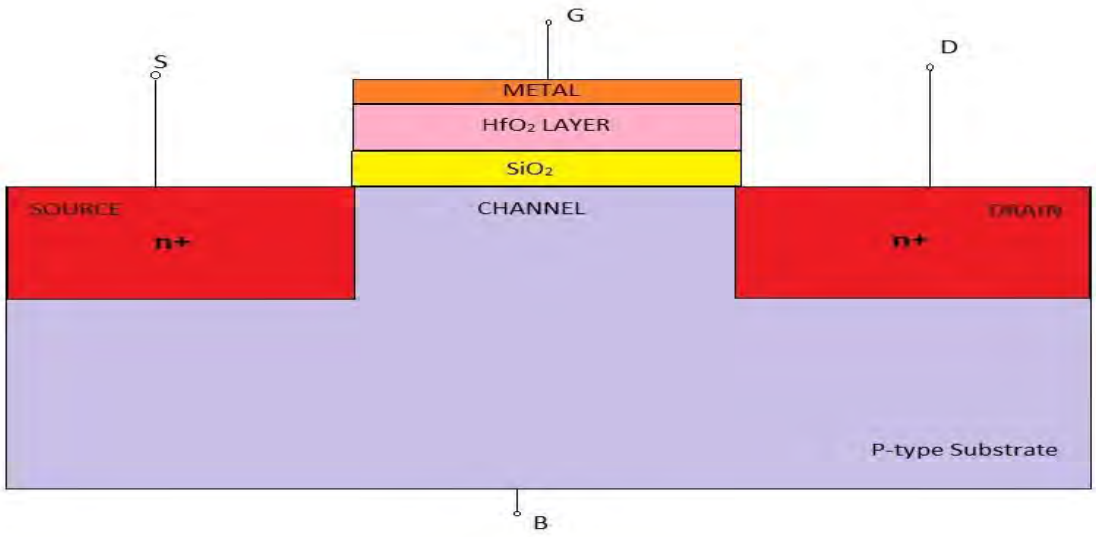


Figure 4.6: Schematics of the device

MODEL:

—Fermi-Dirac Carrier Statistics

—Shockley-Read Hall Model

—Lombardi CVT Model

Device Structure Parameters:

—Gate length: 28nm

—Channel Width: 50nm

—Gate Oxide Thickness: 2nm

—Ferroelectric Layer Thickness: 10nm

—Body Doping: 1x 10^{18} cm^{-3}

—Drain Doping: 1 x 10^{20} cm^{-3}

—Source Doping: 1 x 10^{20} cm^{-3}

—PR = 9 μC/cm2 , Ps = 9.5 μC/cm2 , EC = 1.1 MV/cm

4.7 Basic Operation

Bulk MOSFET is basically a four terminal device; Gate (G), Source (S), Drain (D) and Body (B). The body is connected with source terminal making it a three terminal device like FET. We'll discuss the basic operations of bulk MOSFET in this section.

4.7.1 Energy Band Diagram:

If we have a uniform semiconductor, then the conduction band and valence band are just constant in the space.

Accumulation Region: Accumulation mode is achieved by applying a negative gate voltage. If negative gate voltage is applied on the gate, holes are drawn to the semiconductor-insulator interface and a conductor surface extends from the bulk all the way to the interface. Since, the source and drain are n-type, it's like a n-p-n (source and drain are insulated by two reverse biased p-n junction) transistor in accumulation mode and electrons can't go to drain, which means, no conduction channel is formed. In the simulation process, we observed our results keeping the range of gate voltage from -2 to 2. The following Fig. 4.7.1.1 indicates the band diagram of accumulation region where the gate voltage is V_g= -2V.

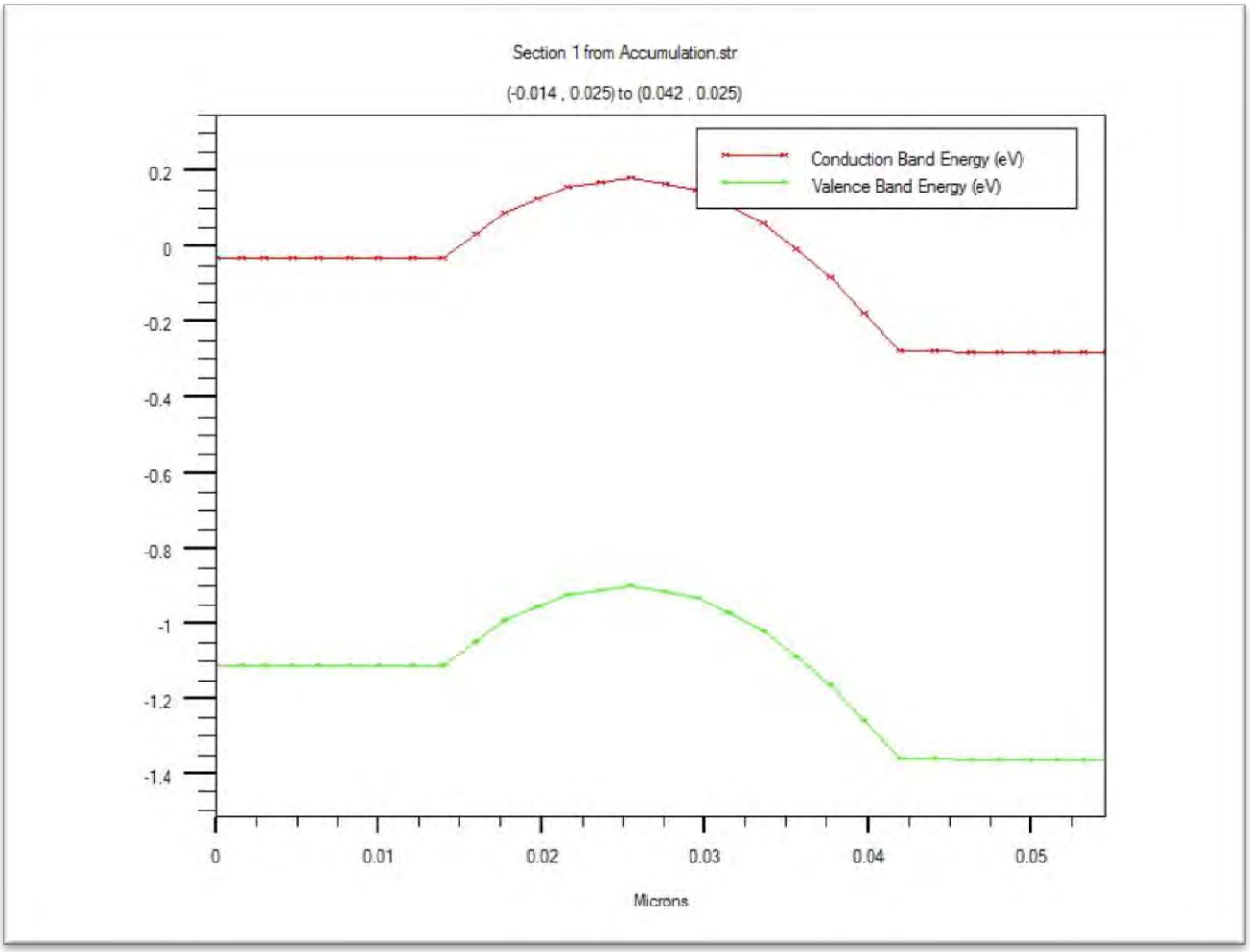


Figure 4.7.1.1: Energy Band Diagram in Accumulation Mode

With the application of V_g= -2V, the fermi energy level goes closer to the valence band and if fermi level is found near valence band, there will be significant number of empty states in the valence band. Holes start to accumulate in the oxide-semiconductor interface which is known as the potential wall. There are a few electrons even though the fermi level is away from the conduction band. Electrons will not be able to flow across the p-type body due to the barrier seen from the source to channel.

Depletion Region: Depletion mode is achieved by applying small amount of positive gate voltage. Fermi energy level goes up and holes leave behind immobile negative charge leaving behind immobile negative charge. The following Fig. 4.7.1.2 represents the depletion region at V_g=0.2V.

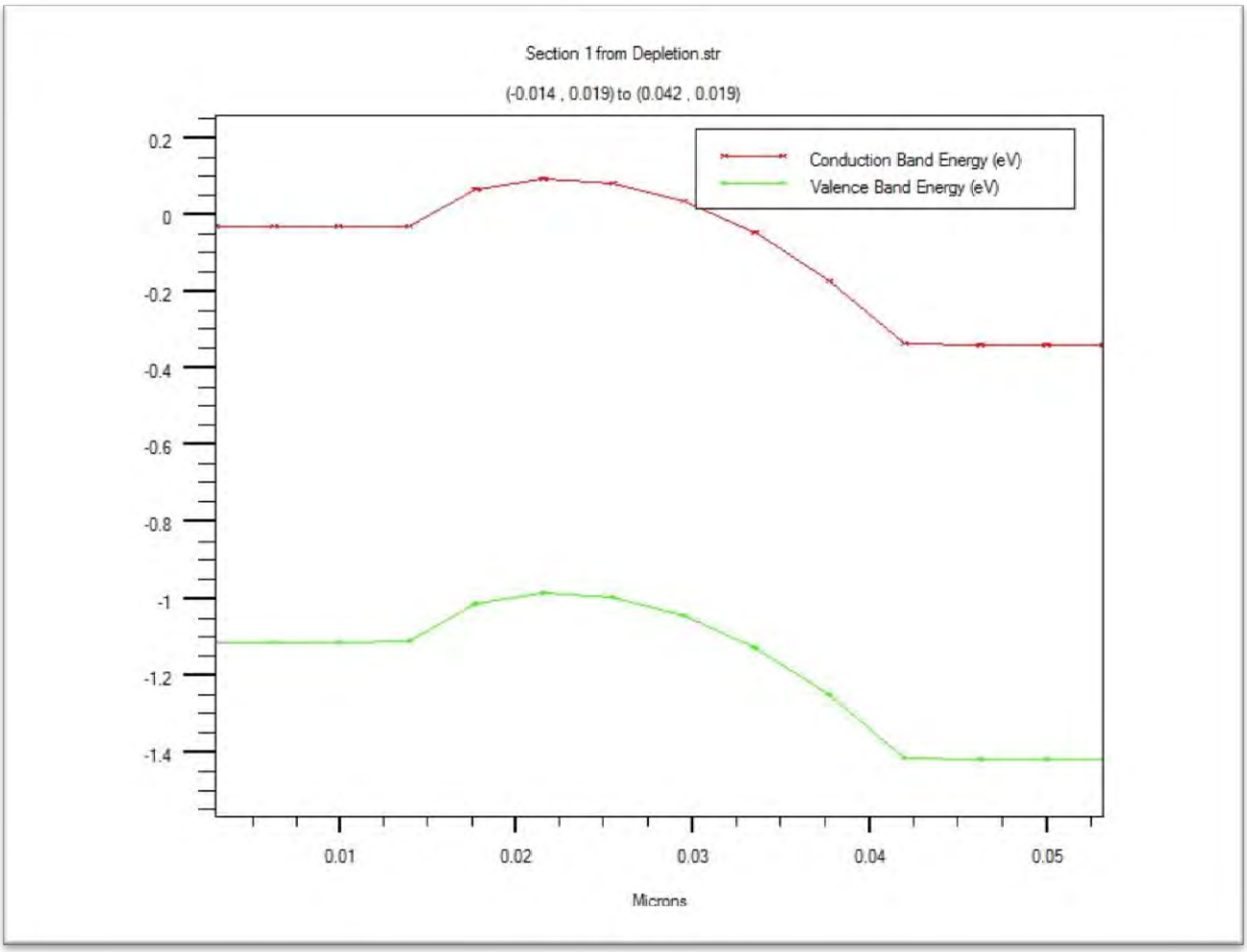


Figure 4.7.1.2: Energy Band Diagram in Depletion Mode

At depletion mode, there is no hole or electron concentration and so, it behaves like an intrinsic semiconductor.

Inversion Region: This mode is achieved by applying large gate voltage and fermi level goes upper than the depletion mode. At the interface it has become n-type because fermi energy level is closer to the conduction band. Band bending has converted the material from p-type to n-type at the interface. The following Fig. 4.7.1.3 indicates the inversion mode where the gate voltage is V_g=2V

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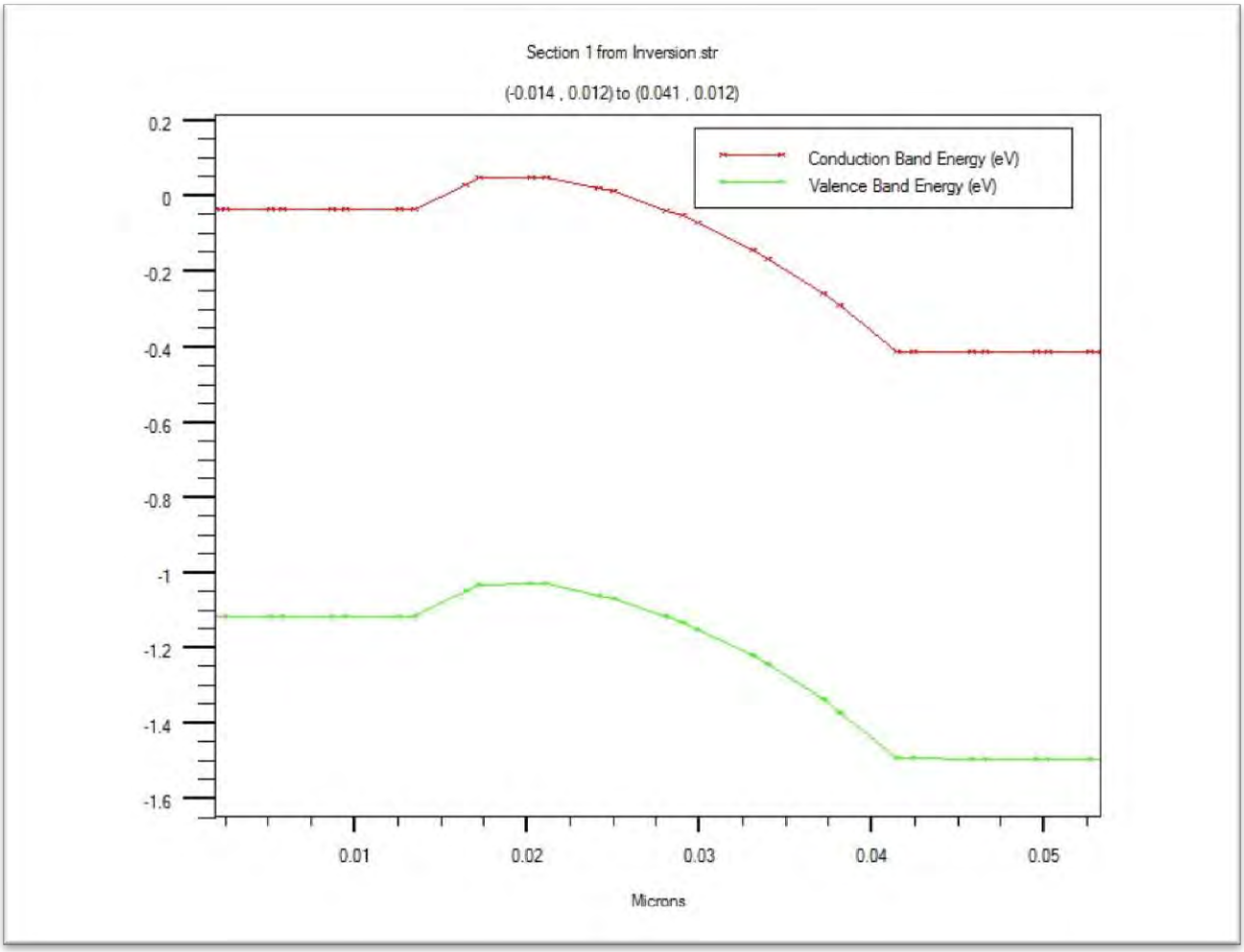


Figure 4.7.1.3: Energy Band Diagram at inversion region

This process yields to two types of electron; immobile ions (-ve) that causes depletion region and another is minority carriers (-ve) that accumulate just at the surface. The n-type channel connects the source to the drain and conducts. As the material converts from p-type to n-type, the mode is known as inversion mode.

4.7.2 Surface Potential:

A surface potential is achieved from the ATLAS simulation result. Surface potential becomes positive when the band bends down. For a surface potential larger than twice the bulk

potential the inversion layer charge increases exponentially with the surface potential. Consequently, an increased gate voltage yields an increased voltage across the oxide while the surface potential remains almost constant along the length of the channel under a specific metal. As doping concentration level is high in both source and drain, the width of the depletion layer will be comparatively small that is negligible for the simplicity of the model.

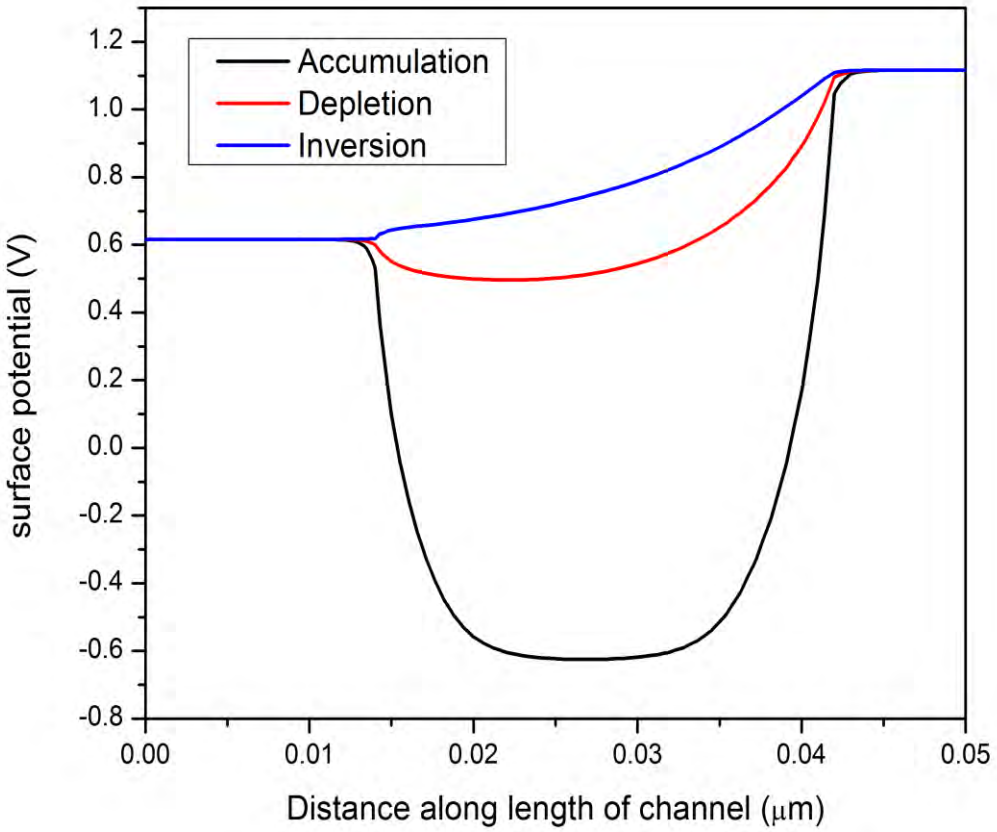


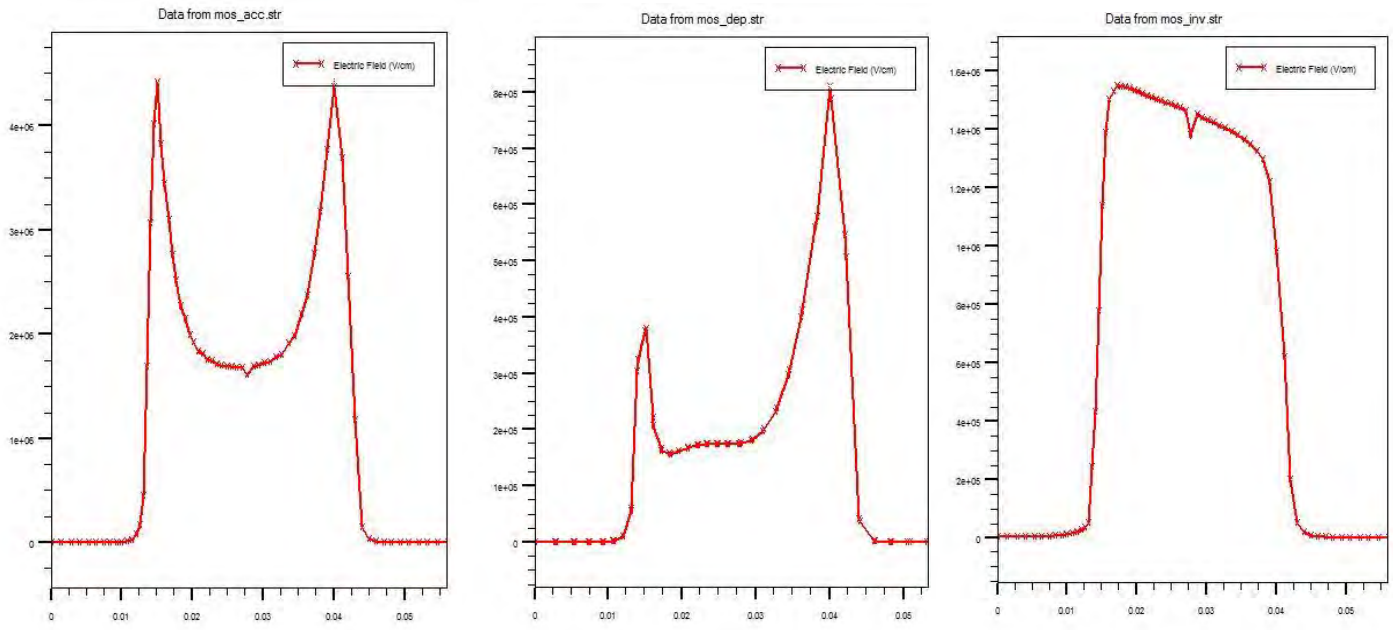
Figure 4.7.2: Surface potential in three regions of the device

If HfO2 is used as dielectric instead of SiO2, it will affect only the regions around the junction. With the increment of the permittivity of the oxide, potential becomes more flat towards the drain-body and source-body interface regions. Inside the channel, the effect of the dielectric change on the potential profile can be neglected.

4.7.3 Electric Field:

Fig. 4.7.3.2 shows electric field along the length of channel (at surface) in accumulation (V_{gs}=-2.5V), depletion (V_{gs}=0.1V) and strong inversion (V_{gs}=2.5V) of the device when V_{ds}=0.5Vpeak value occurs at source-body and drain-body junctions which means electric field exists only at three regions, drain-body junction, source-body junction and channel-body junction. Electric field is low elsewhere in the device

Like potential profile, electric field is also affected by changing gate dielectric. If high-k dielectric is used, the lateral field becomes more constant in the channel region.

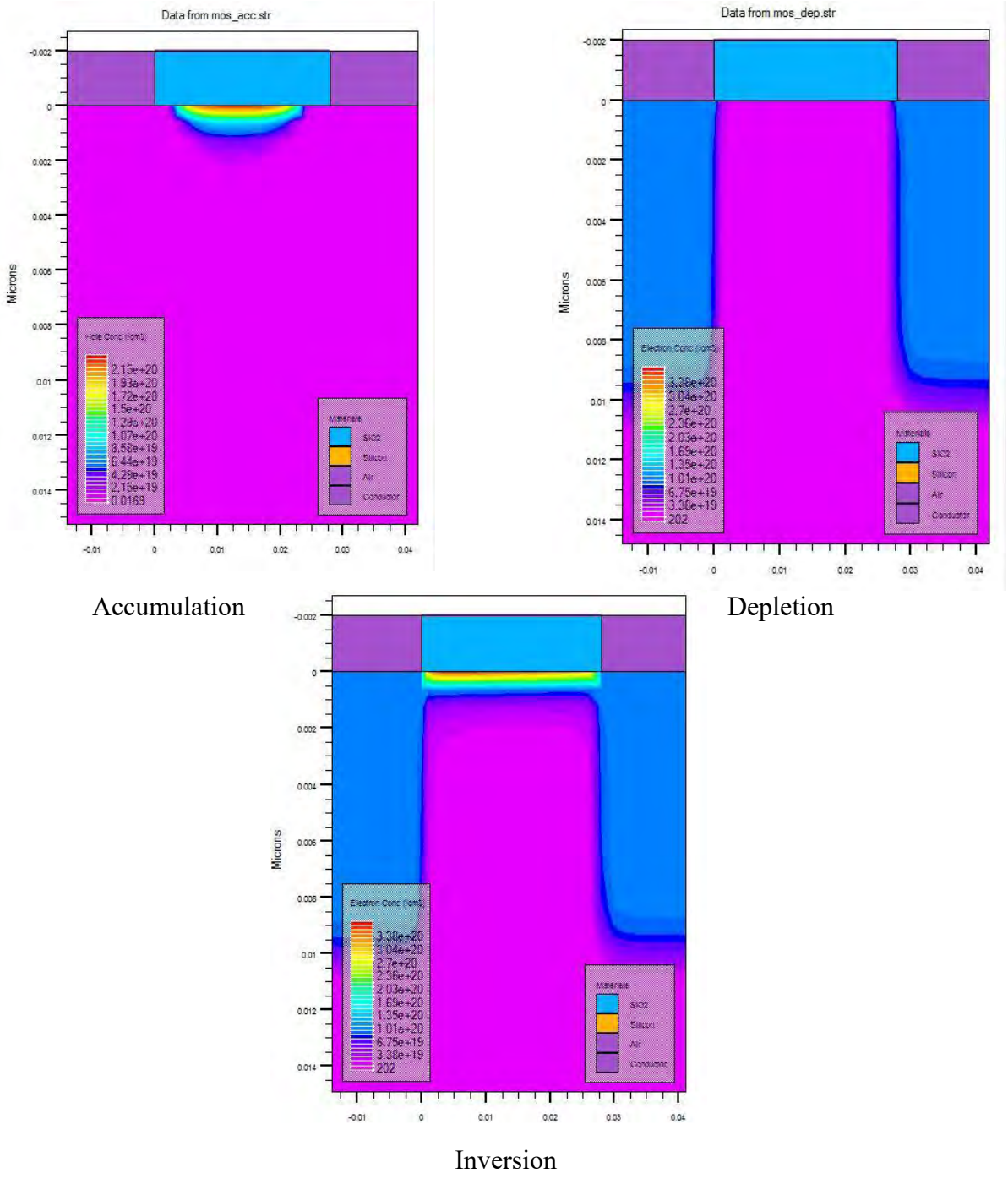


Accumulation Depletion Inversion

Figure 4.7.3: Electric field along the length of channel (at surface) in accumulation (V_{gs} =-2.5V), depletion (V_{gs}=0.1V) and strong inversion (V_{gs}=2.5V) of the device. V_{ds}=0.5V

4.7.4 Charge Concentration:

Fig 4.7.4.1 shows the structural pictures of charge concentration for different modes of operation .



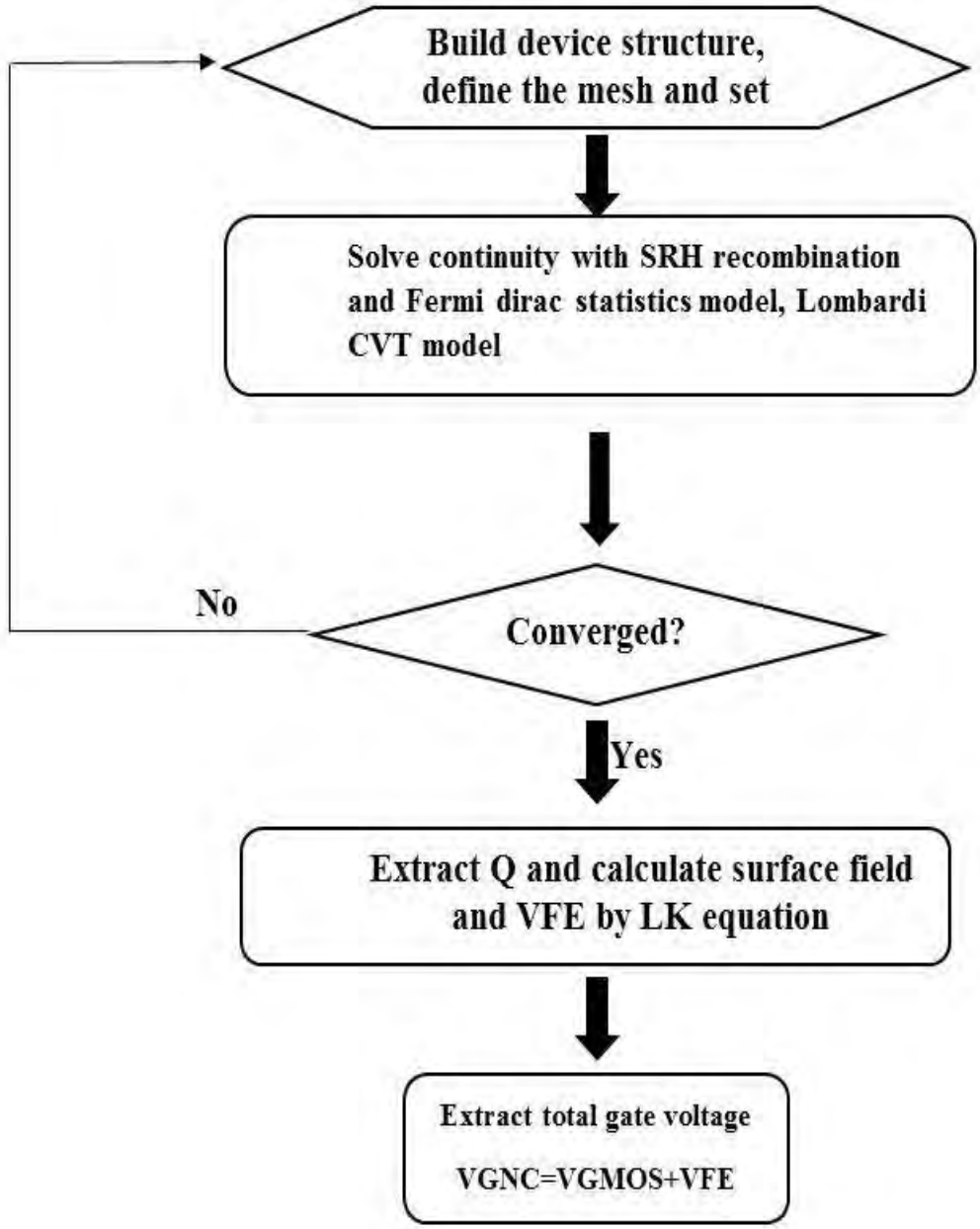
Accumulation

Depletion

Inversion

Figure 4.7.4: Charge distribution in accumulation (V_{gs}=-2.5V), depletion (V_{gs}=0.1V) and strong inversion (V_{gs}=2.5V) of the device. V_{ds}=0.5V

The flow chart that we followed to get the gate voltage of NCFET is given below:



And following previous flow chart we get the I_D-V_{gs} curve for in liner and in logarithimic scale below which clearly shows that the curve for NCFET device is much steeper than the curve for MOSFET device.

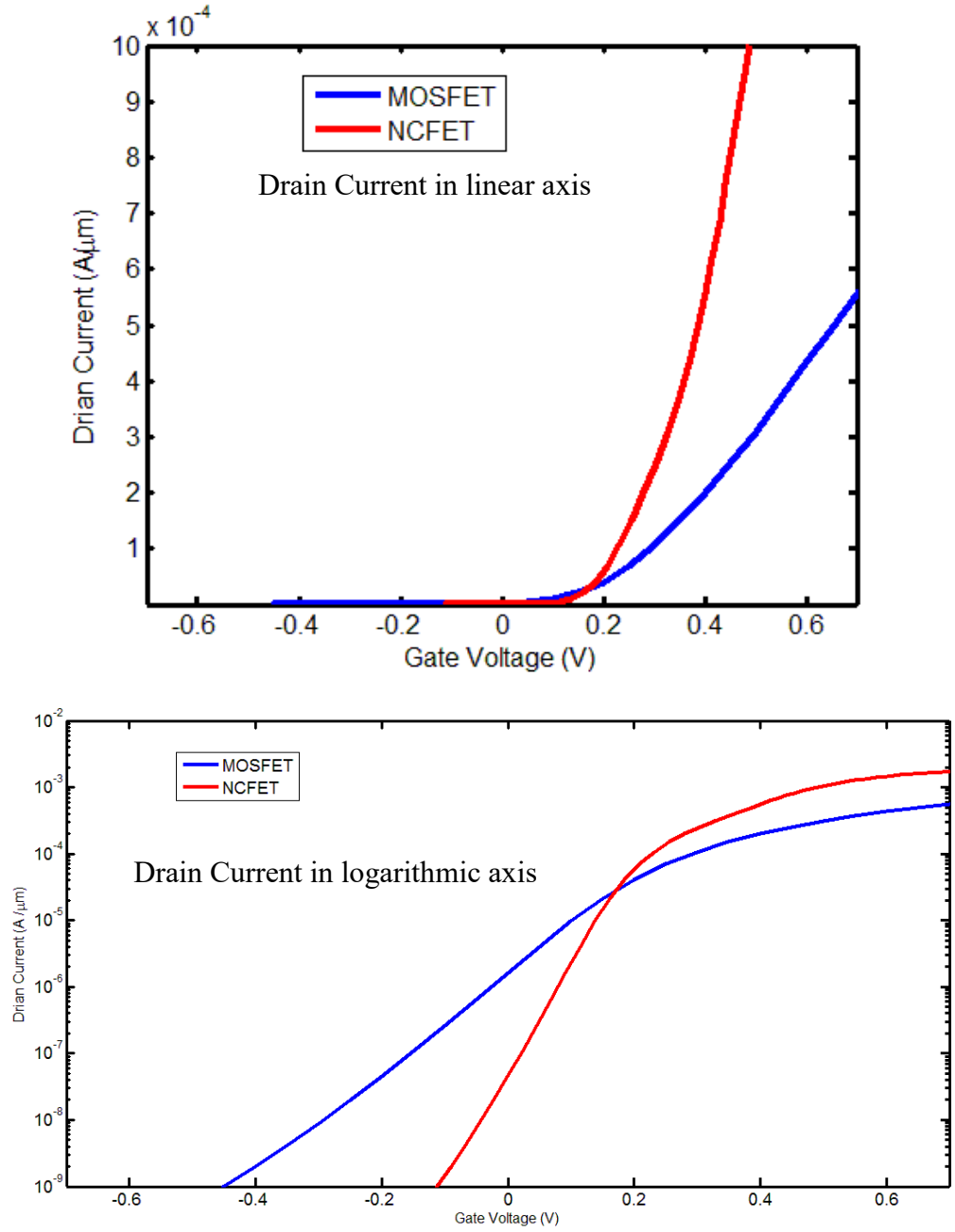


Figure 4.8: Drain current (in linear and logarithmic axis) for MOSFET and NCFET devices. V_{ds}=0.5V

Chapter 5

Conclusion and Future Scope

5.1 Conclusion:

In this thesis work, an analytical model for polarization, energy distribution, dielectric constant, anisotropy constant variation of the Ferroelectric material in NCFET has been proposed. The properties of ferroelectric material, advantages and operations have been briefly discussed. Charge distribution of baseline MOSFET has been extracted from TCAD model and incorporated in 1-D Landau model to find the voltage drop across ferroelectric material. Si doped HfO_2 has been used as ferroelectric material. Other ferroelectric materials have been also introduced and the reason behind not choosing those in this work has been explained with valid reasons. The thickness of HfO_2 has been varied for studying the hysteresis conditions properly.

A numerical model of the device has been developed in Silvaco, ATLAS where the structural properties. For different biasing conditions, simulation results have been observed. Moreover, I_D-V_{gs} graph has been extracted. Surface potential, Electric field, band diagrams and charge concentration for different operating regions have been extracted and compared.

Fermi-Dirac Carrier Statistics, Shockley-Read Hall Model, and Lombardi CVT models have been used to perform the simulation process properly and the charge on the ferroelectric material is obtained by using this models. From this charge, voltage drop across the ferroelectric has been found and using that gate voltage of NCFET has been calculated. It has been noticed that for a small change in gate bias, the surface potential increases more significantly, hence voltage amplification occurs.

The motive behind this work is to observe, if a ferroelectric insulator is introduced, it should be possible to obtain a value of sub-threshold slope (SS) lower than 60mV/decade. Due to this reason, relative improvement in the device performance especially in SS region using FE layer has been observed compared to the conventional MOSFET device.

5.2 Future Scope:

A promising device has been analyzed with a ferroelectric material which has comparatively better performance than other ferroelectric materials in voltage amplification and low power dissipation. Besides, NCFET overcomes the limitations and boundaries faced by other FET devices. In spite of these advantages, there are some limitations. The simulation of the NCFET device in ATLAS, Silvaco cannot be done directly by using only ferroelectric material parameters and structural parameters. If this work is further extended with Double Gate Negative Capacitance Field Effect Transistor (DG-NCFET) instead of bulk NCFET, more improvement in the device performance with lower SS can be achieved.

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