Modeling a DC to DC Converter and Design a Controller for the Converter

A Thesis Submitted to the Department of Electrical and Electronics Engineering of **BRAC University**
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Declaration

We hereby declare that this thesis paper titled 'Modeling a DC to DC converter and design a controller for the converter' is done only by our research along with the research's implementation results found by us. Any material of research or thesis used from other sources has been mentioned along with their references. This thesis has not been previously submitted for any degree by anyone else. This thesis report is being submitted to the Department of Electrical and Electronic Engineering of BRAC University.

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Date of Submission: 20th August, 2017

Acknowledgement

In performing our final semester thesis, we had to take the help and instruction of some respected persons, who would be worthy of our greatest admiration. The completion of this thesis gives us much satisfaction. We would like to show our gratitude to **Dr. Amina Hasan Abedin, Assistant Professor, BRAC University** for giving us a good guideline for our thesis throughout the three semester with frequent consultations, meeting and feedback sessions. We would also like to expand our sincere appreciation to **Md. Farhan Tasnim Oshim, Lecturer, BRAC University** who has guided in our thesis.

Many people, especially our classmates, lab technicians of hardware labs and for the very obvious reason the group members itself, have made valuable comment, propositions on this proposal which gave us an inspiration to improve our thesis. We owe a deep sense of gratitude all the people for their help directly and indirectly to complete our thesis.

Finally, we must convey our very deep thankfulness to our parents for providing us with constant support and continuous support all the way through the years of study and through the process of researching and writing this thesis. This accomplishment would not have been possible without them.

Thank you.

Abstract

DC-DC converters are some of crucial power electronic circuits. They are widely used in the power supply equipment for most electronic instruments and also in specialized high-power applications such as battery charging, plating and welding. As well, not only DC-DC switching regulators that meet the rugged requirements of industrial systems but also DC-DC switching regulator solves the difficult automotive requirements. In addition to a controllable and theoretically lossless DC voltage transformation, DC-DC converter circuits may also provide voltage isolation through the incorporation of a small high frequency transformer. But having efficient and stable value is a challenge for us. In our thesis, we come to the point that we need a systematic control approaches which will be anticipated as controller because controller is better to use in the converter which will vary our duty cycle to maintain steady output, even when the system voltages and currents are more distorted. Upcoming industrial revolution of Bangladesh can be helped by this kind of converter and controller where we can provide high power density and high efficiency along with energy recovery.

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Chapter 1
Introduction

1.1 Motivation:

The degree of dependence that mankind has come to grow on the precision and efficiency of modern machineries is hardly debatable. By the dint of modern technology, productivity has been increased by several folds and progress of mankind has advanced by decades. With this progress, the need for more efficient power systems has risen significantly. The loss incurred in distribution systems and modern machineries. Bringing down these losses will result in decreased expenses in power generation, increase productivity and decrease the detrimental effect on the environment as well. The ramifications on power regulation and consumption by power quality if distribution systems can scarcely be ignored. Various power quality issues like sags, under voltages, voltage transients, interruptions and harmonic distortions can drastically bring down the overall efficiency and precision of a systems, adversely affect the electronics on the load side.

In reality, realizable linear loads can also sometime show some form of nonlinearity. Real components sometimes exhibit some characteristics like saturation of a magnetic circuit, a rectifier circuit with capacitor filter. These loads can draw non-sinusoidal currents even when connected to sinusoidal voltages. As such, harmonics develops within the system which in turn, interacts with the system to produce voltage distortions in a power system and cause adverse effects to entrenched loads.

Thrystors and static power converters accounts for the largest number of nonlinear loads connected to power grids. These power converters are indispensable in various industrial applications such as variable speed drives, switch mode power supplies, uninterrupted power supplies etc. A Fourier analysis of such loads can show us the causes by decomposing the distorted waveform into

1. The fundamental frequency signal (50hz or 60hz according to area)
2. Combination of frequencies that are odd multiples of the fundamental frequency called harmonics

Harmonics can cause unwarranted rises in peak currents which can heat up equipment and wirings downstream of the current and cause power loss. Drastic peaks in current amplitudes can be detrimental to equipment lifetime. The 3^{rd} harmonic current accumulation in the neutral conductor in 3 phase systems can cause drastic overheating and cause power factor to fall. Ergo it is essential that these discrepancies be brought down to a bare minimum for increased stability of the system.

1.2 Objectives:

To avoid such problems while power conversion, proper steps need to be taken to filter harmonics out of the system or implement power factor correction to stop harmonics initially. This can be achieved by adding power factor circuitry into the system. There are several ways to achieve power factor correction. One is to compensate by adding reactive power with large banks of capacitors that can be instantly switched to the circuit. Such means of PFC is very expensive when small power systems are concerned and the size counts in as a big factor. An active PFC circuit most commonly used is a boost PFC converter. It is the most popular and easily implemented PFC circuitry, widely used in power generation plants and electronic devices.

Reason why boost converter is usually preferred because:

1. Attains very low THD, offering possibly the best power factor, PF
2. Higher output voltage
3. In size, efficient energy-storage capacitors
4. Easy switch current sense and gate drive, because of low-side boost switch
5. Relaxed surge management

1.3 Organization:

Firstly, we have observed rectifier circuits as ac to dc power supply are used within the construction of most modern electrical and electronic equipment. Then we have discussed about power factor correction of the rectifier circuits and we have introduced DC-DC converter for doing this. Later, we have presented that for making converter more efficient we need controller. After that we have showed the theoretical implementation of the controller with op-amps and then we have demonstrated the hardware setup of the DC-DC boost converter. Lastly, we have talked about the future field of work which will carry our thesis topic further away.

Chapter 2

Power Factor Correction

2.1 Introduction:

Gradual increase in electronics consumers and the unyielding occurrence of mains rectification circuits inside the electronic devices dominants the cause of mains harmonic distortion. Some form of ac to dc power supply are used within the construction of most modern electrical and electronic equipment and for each half cycle of the supply these supplies take pulses of current. Considering for single device, suppose a domestic television, the amount of reactive power drawn may be small. Nevertheless, for mass amount, perhaps 100 or more TVs the reactive power utilization from the same supply phase causing a flow of large amount of reactive current and hence harmonics generation. The advancement in power electronic converters reduces the weight and size and concurrently the performance and function of such converters preferable for industrial, commercial and residential purposes.

This reactive current cannot be recognized as the domestic tariff meter is concerned and it results loss of revenue due to the mismatch between the developed and that used power. In addition, the supply voltage waveform catches distortion due to the reactive current and for this reason an EMC problem happens. Furthermore, this cumulates supplementary losses and dielectric stresses in capacitors and cables because of the harmonic content and hence the increase in currents in windings of rotating machinery and transformers and noise in various products.

As it is the flourishing era of smart electronic devices- the rise and growth in use of apparatus like computers, laptops, telecom, biomedical equipment causing uninterruptable power supplies which is uncontrollable and additionally it is resulting to the high-power draw and small power density. However, industry or market demands the reduction of power sources with greater power density at reasonable value. As a consequence, it is compulsory to deliver additional power on a lesser cost and size for the telecom and computer applications. To resolve these concerns, it is desired to design the distributed power system (DPS) which will utilize isolated DC-DC converters for unraveling power factor correction and eliminating harmonics.

2.2 Non-linear loads and its effect:

The distortion of normal electric current waveform because of the nonlinear loads generates harmonics in AC distribution systems. Nonlinear loads take place for variable resistance as in resistance varies for each sine wave of the applied voltage, causing in a series of positive and negative pulses. Generally, in AC-DC system- the connected apparatus or device to the DPS needs some kind of power conditioning, rectification which creates a non-sinusoidal line current because of the non-linear input characteristic. The presence of nonlinear loads will make all the third harmonic exactly in phase and add, rather than cancels in all the phases. Thus, current and heat is developed on the neutral conductor. The harmonic loads decrease the distribution capacity and effects to the quality of the power of public utility systems. Perpetually, Computer equipment with switched mode power supplies, battery chargers, UPSs, variable speed motors and drives, fax machines, laser printers, photocopiers, medical diagnostic equipment etc. work as nonlinear loads.

2.3 Harmonics alleviation:

Practically, complete elimination of harmonics would be very tough and expensive. Considerate about the alternatives and their appropriate costs for harmonizing the real harmonic load in contradiction of the cost of the solution is the very important factor. For the minimization of the actual harmonic loads there are numbers of choices offered, however should be studied consciously.

2.4 Rectifiers:

One recent survey showed the percentage the total electrical consumption by non-linear loads will double from the year 1985 to 2000. The AC-DC converter used in the switching-type power supplies found in most personal computers and peripheral equipment, such as printers, is an example of a non-linear load. While they offer many benefits in size, weight and cost, the large increase of equipment using this type of power supply over the past fifteen years is largely responsible for the increased attention to harmonics.

Fundamentally, rectifier converts AC to DC. The purpose of a rectifier may be to produce an output that is purely DC, or the purpose may be to produce a voltage or current waveform that has a specified DC component. In practice, the half-wave rectifier is used most often in low-power applications because the average current in the supply will not be zero, and non-zero average current may cause problems in transformer performance **[1]**.

2.4.1 Half wave rectifier:

A basic half-wave rectifier with a resistive load is shown in Fig. 2.1 the source is AC, and the objective is to create a load voltage that has a nonzero dc component. The diode is a basic electronic switch that allows current in one direction only. For the positive half-cycle of the source in this circuit, the diode is on (forward-biased) **[2]**. However, there are some disadvantages of half wave rectifier which holds us back to apply the half-wave rectifier for smart and power consuming electronic devices.

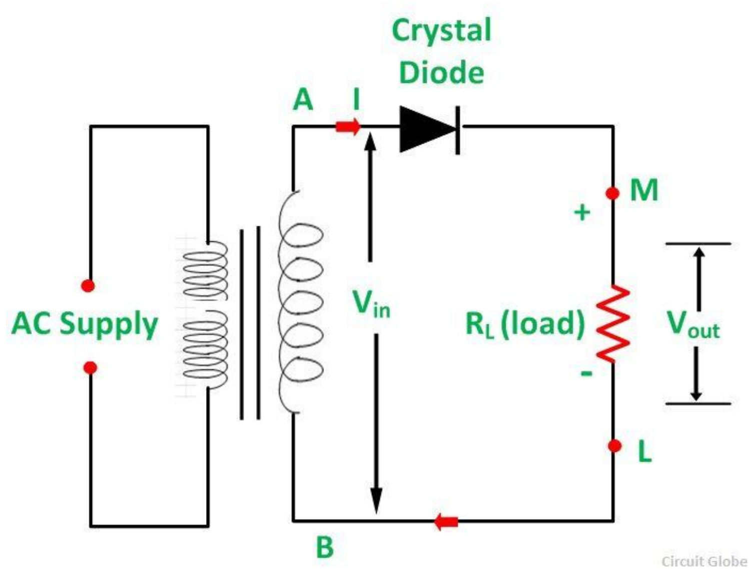


Fig: 2.1: Half wave rectifier

Rectification Efficiency, Ƞ = $\frac{P_{dc}}{P_{ac}} = \frac{4}{P^2} \times \frac{R_L}{R_F+R_L} = \frac{0.406}{1+[\frac{R_F}{R_L}]}$ if R_F is neglected, the efficiency of half wave rectifier is only 40.6%. Additionally, ripple factor is another predicament of half -wave rectifier and it is defined as the amount of AC content in the output DC. It nothing but quantity of AC noise in the output DC. Less the ripple factor, performance of the rectifier is more. The ripple factor of half wave rectifier is about 1.21 (full wave rectifier has about 0.48). Besides, it has other problems like less transformer utilization factor and so on so forth. Hence, due to all these problems half wave rectifier is not suitable for smart and power efficient electronic devices we are talking about. Half wave rectifier is primarily suitable for the low power circuits and very obvious reasons it has very low performance when it is compared with the other rectifiers.

2.4.2 Full wave rectifier:

In full wave bridge rectifier, an ordinary transformer is used in place of a center tapped transformer. The circuit forms a bridge connecting the four diodes D_1, D_2, D_3, and D_4. The circuit diagram of full wave bridge rectifier is shown below.

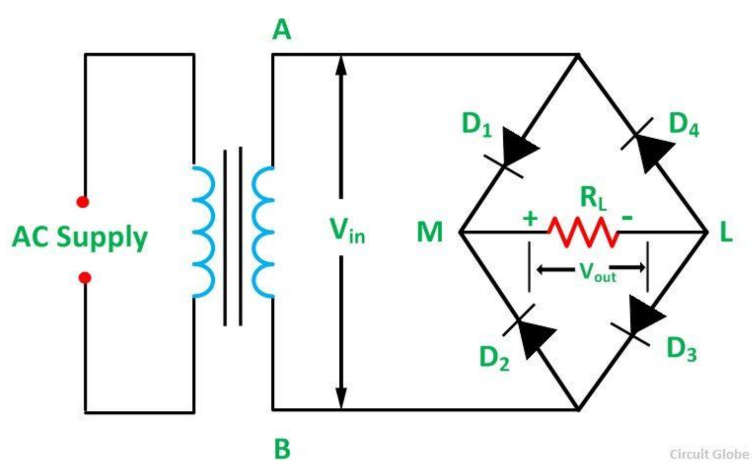


Fig. 2.2: Full wave rectifier.

The rectification efficiency of full-wave rectifier is double of that of a half-wave rectifier. Additionally, higher output voltage, higher output power and higher Transformer Utilization Factor in case of full-wave rectifier. Furthermore, the ripple voltage is low (full wave rectifier has about 0.48) and of higher frequency in case of full-wave rectifier so simple filtering circuit is required. Moreover, no center tap is necessary in the transformer. Secondarily, so in case of a bridge rectifier the transformer required is simpler. If stepping up or stepping down of voltage is not required, transformer can be eliminated even. Besides, for a given power output, power transformer of smaller size can be used in case of the bridge rectifier because current in both primary and secondary windings of the supply transformer flow for the entire AC cycle.

Though full wave rectifier is effective and efficient than half wave rectifier, it creates distortion, harmonics and to get rid of that we are going to arrange a Power Factor Correction (PFC) circuit topology which will contain a boost type DC to DC converter with controller.

2.5 Effects of non-PFC equipped circuit:

Non-PFC power supplies use a capacitive input filter, as shown in Fig. 2.3 when powered from AC power line.

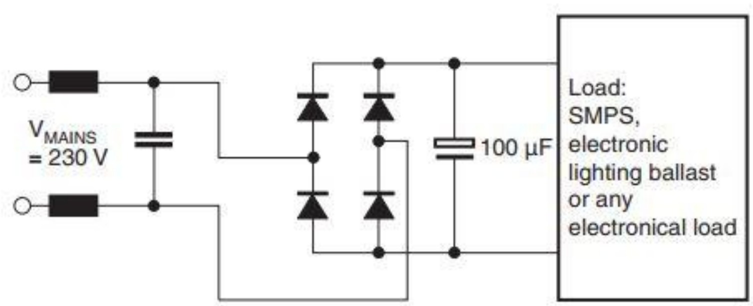


Fig.2.3: Standard bridge rectification of Line voltage.

This outcome in rectification of the AC line, which in turn causes peak currents at the highest point of the AC voltage. In addition, these peak currents lead to excessive voltage drops in the wiring and imbalance troubles in the three-phase power delivery system. This means that the full energy potential of the AC line will not be utilized.

2.6 Power factor correction:

Power factor correction (PFC) can be defined as the reduction of the harmonic content. By making the current waveform look as sinusoidal as possible. The power drawn by the power supply from the line is then maximized to real power. Assuming that the voltage is almost sinusoidal, power factor depends first of all on the current waveform.

$$Power\ factor\ PF = \frac{Active\ power(P)}{Apparent\ power(S)}$$

2.7 A standard PFC circuit:

The typical topology of a PFC pre-stage that is built of a standard boost converter with a controller. In addition, it is essential that at the output of the Rectifier, there will be no large smoothing capacitor with several µF connected as that would eliminate all efforts of the PFC circuit, even though it would run satisfactorily. The input voltage of the PFC is a rectified DC voltage.

2.8 Simulation and Analysis:

2.8.1 Half wave rectifier with Resistive load:

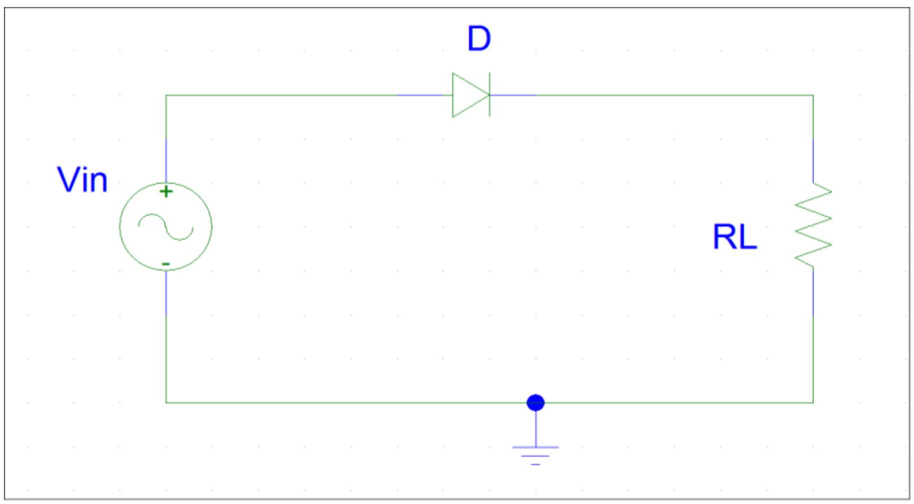


Fig 2.4 (a): Input and Output current

In this part we have showed the half wave rectifier with Resistive load circuit in Fig. 2.4 (a) and its input and output current Fig. 2.4 (b) as well as input and output voltage in Fig. 2.4(c).

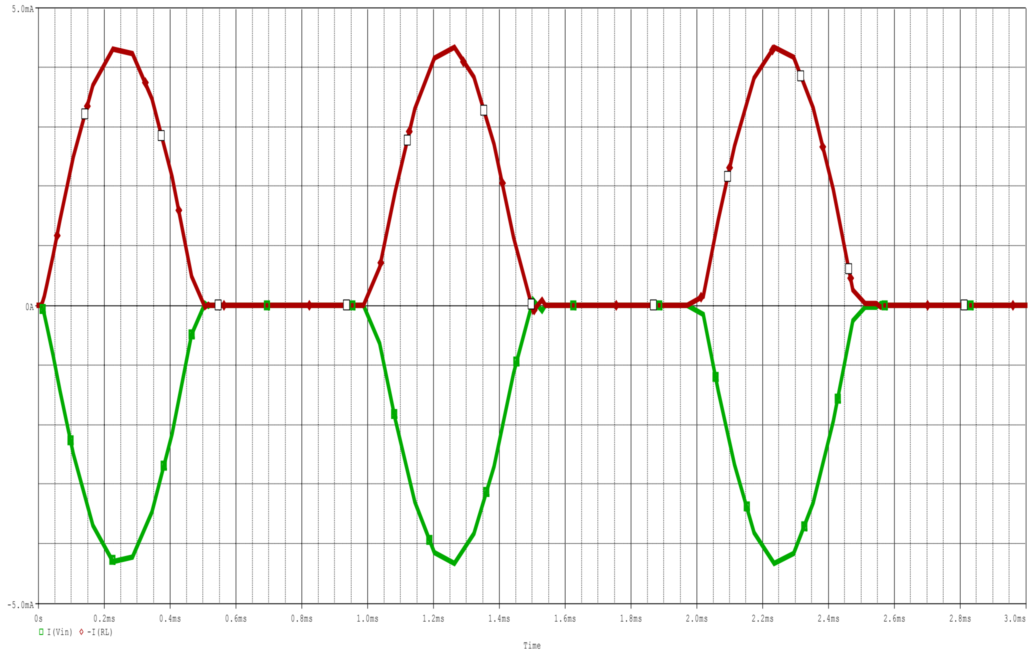


Fig 2.4 (b): Input and Output current

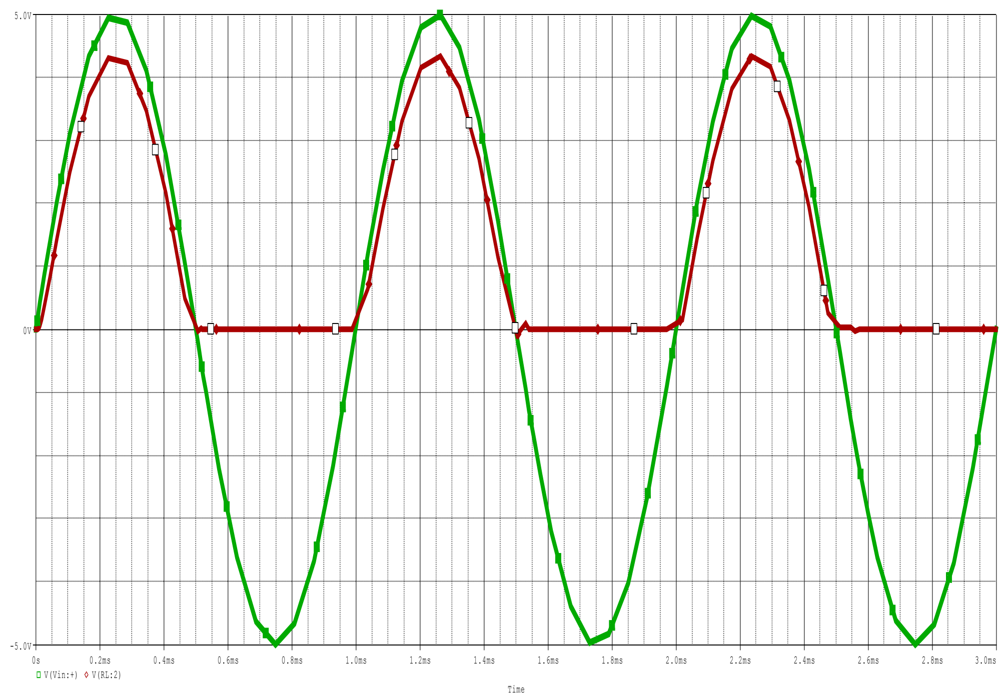


Fig. 2.4 (c): Input and Output voltage

2.8.2 Half wave rectifier with Resistance and Inductance load:

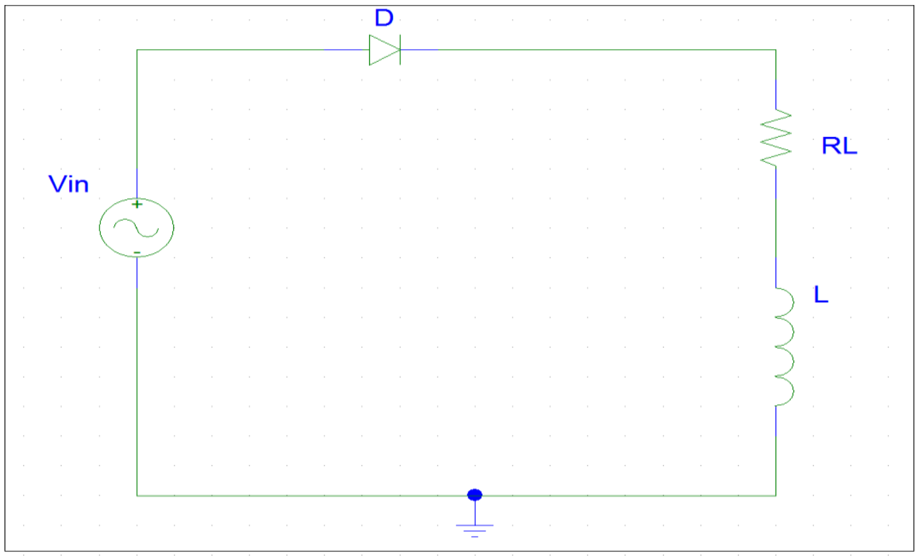


Fig. 2.5 (a): Half wave rectifier with Resistance and Inductance load

In this part we have showed the half wave rectifier with Resistive load circuit in Fig. 2.5(a) and its input and output current Fig. 2.5 (b) as well as input and output voltage in Fig. 2.5 (c).

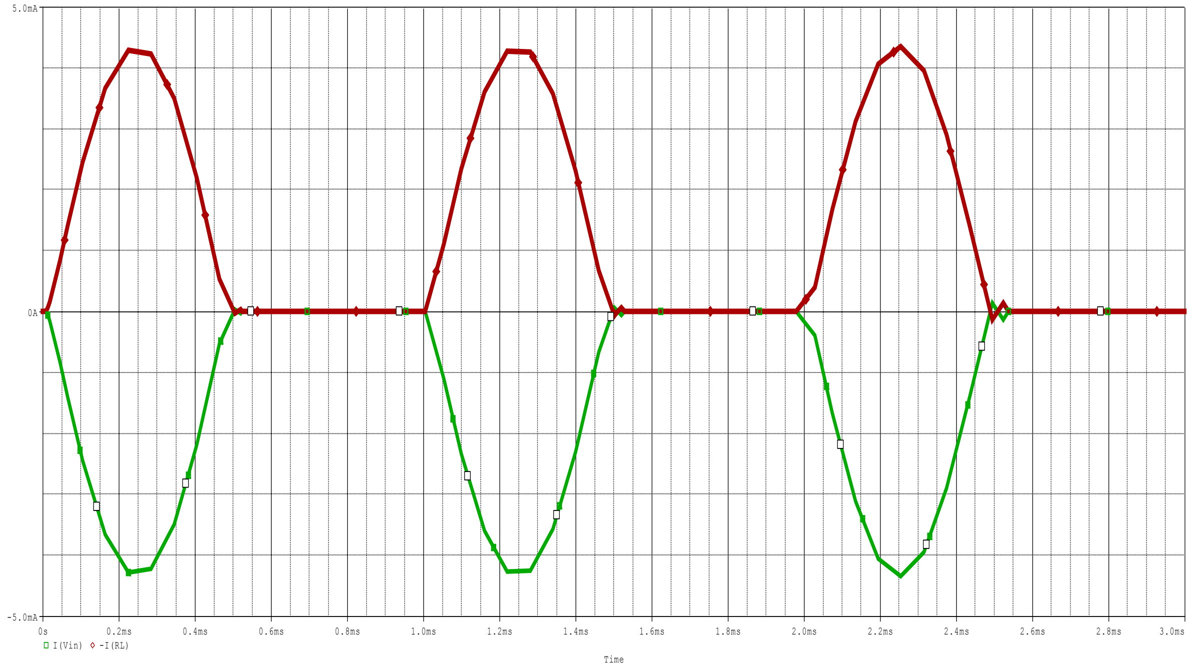


Fig. 2.5 (b): Input and Output current

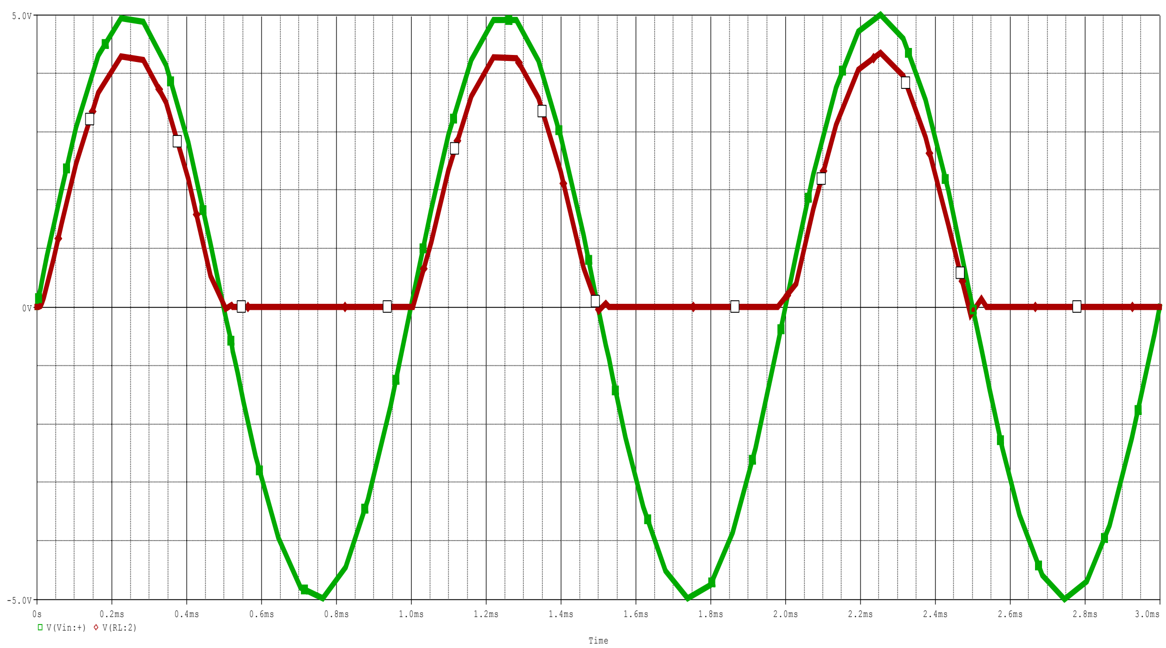


Fig. 2.5(c): Input and Output voltage

2.8.3 Half wave rectifier with Resistance, Inductance & Source load:

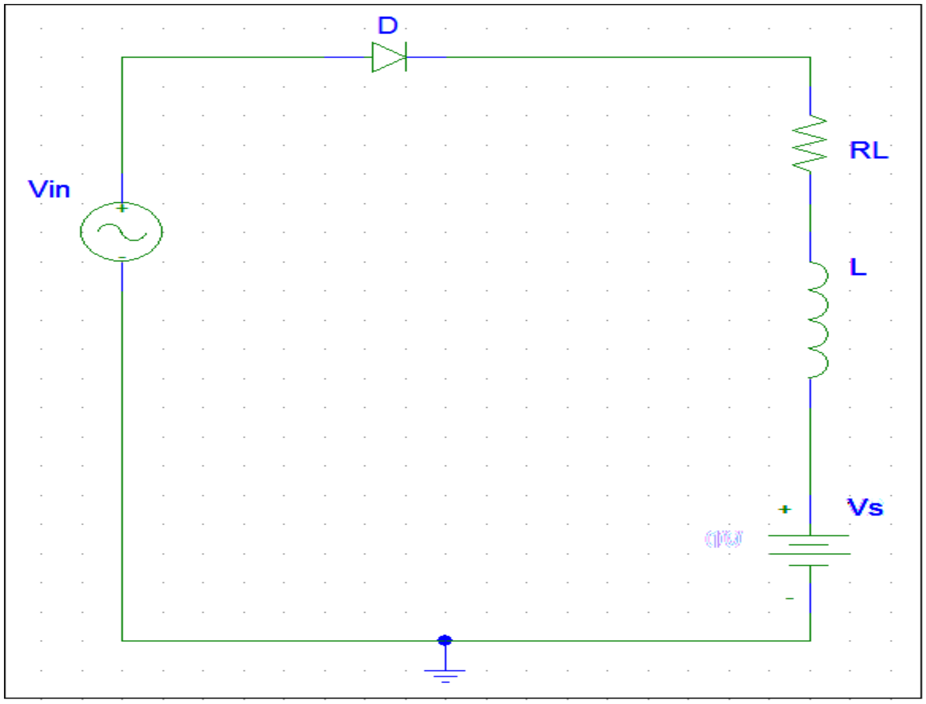


Fig. 2.6 (a): Half wave rectifier with Resistance, Inductance & Source load.

In this part we have showed the half wave rectifier with Resistive, inductive and source load circuit in Fig. 2.6(a) and its input and output current Fig. 2.6 (b) as well as input and output voltage in Fig. 2.6(c).

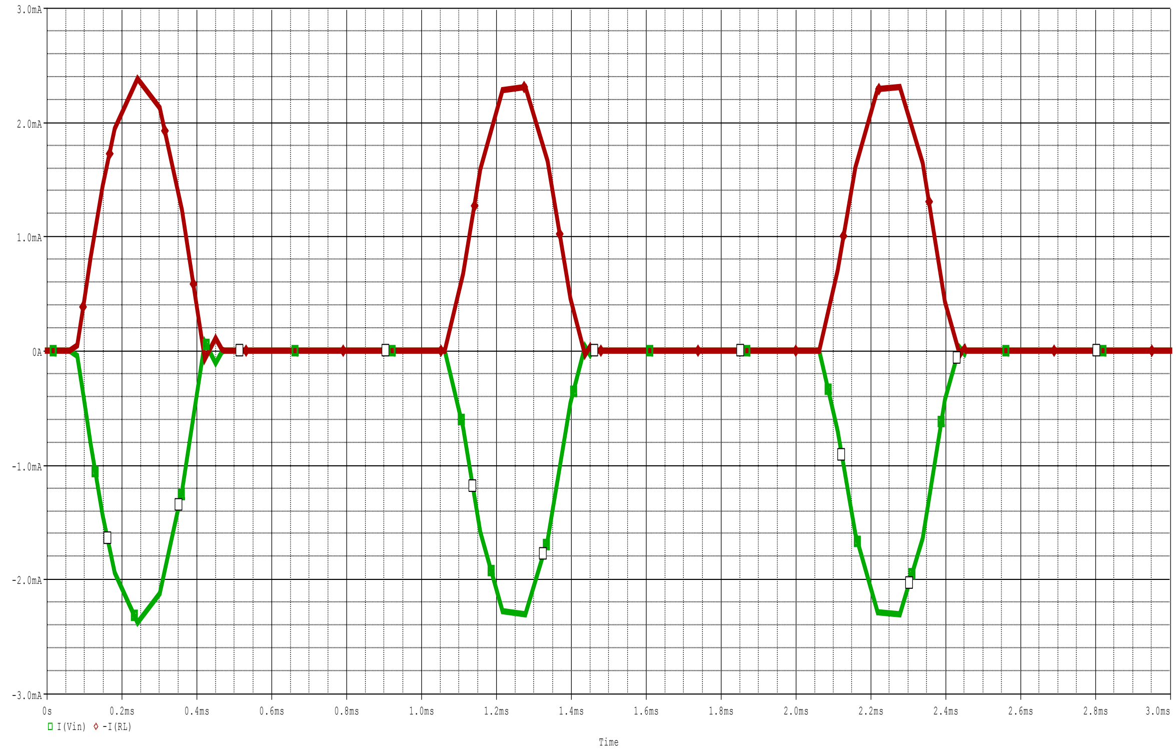


Fig. 2.6 (b): Input & Output current

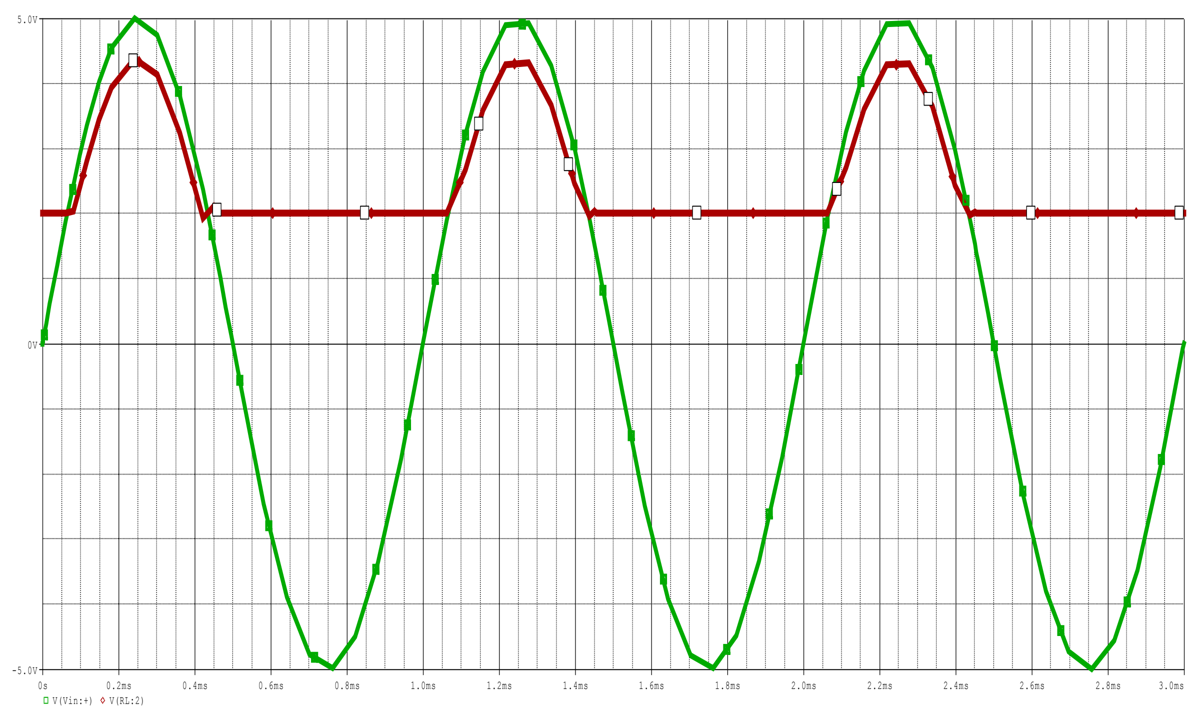


Fig. 2.6 (c): Input & Output voltage

2.8.4 Half wave rectifier with Resistance & Capacitance load:

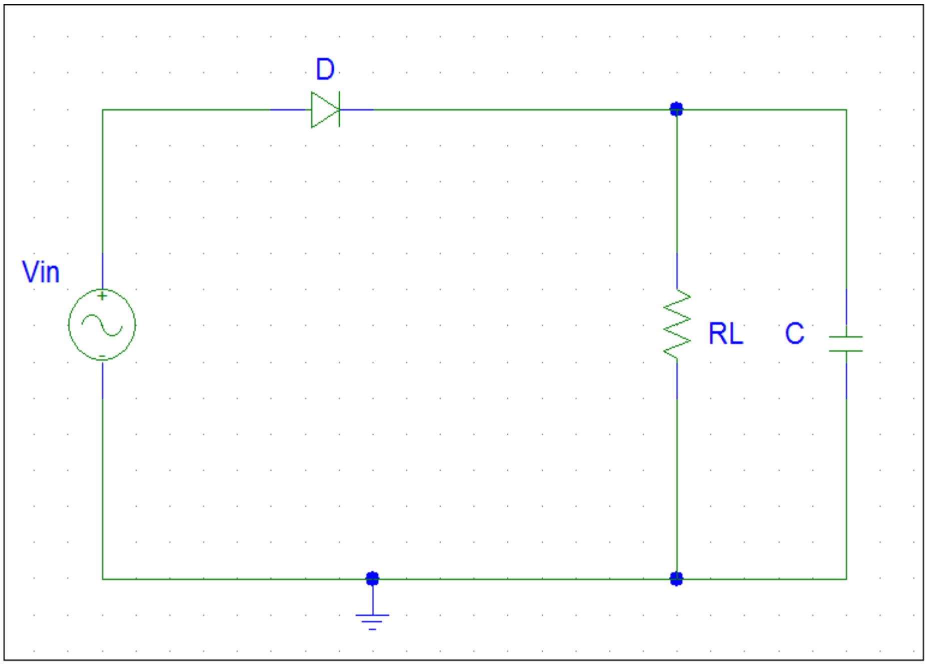


Fig. 2.7 (a): Half wave rectifier with Resistance and Capacitance load

In this part we have showed the half wave rectifier with Resistive and capacitive load circuit in Fig. 2.7(a) and its input and output current Fig. 2.7 (b) as well as input and output voltage in Fig. 2.7(c).

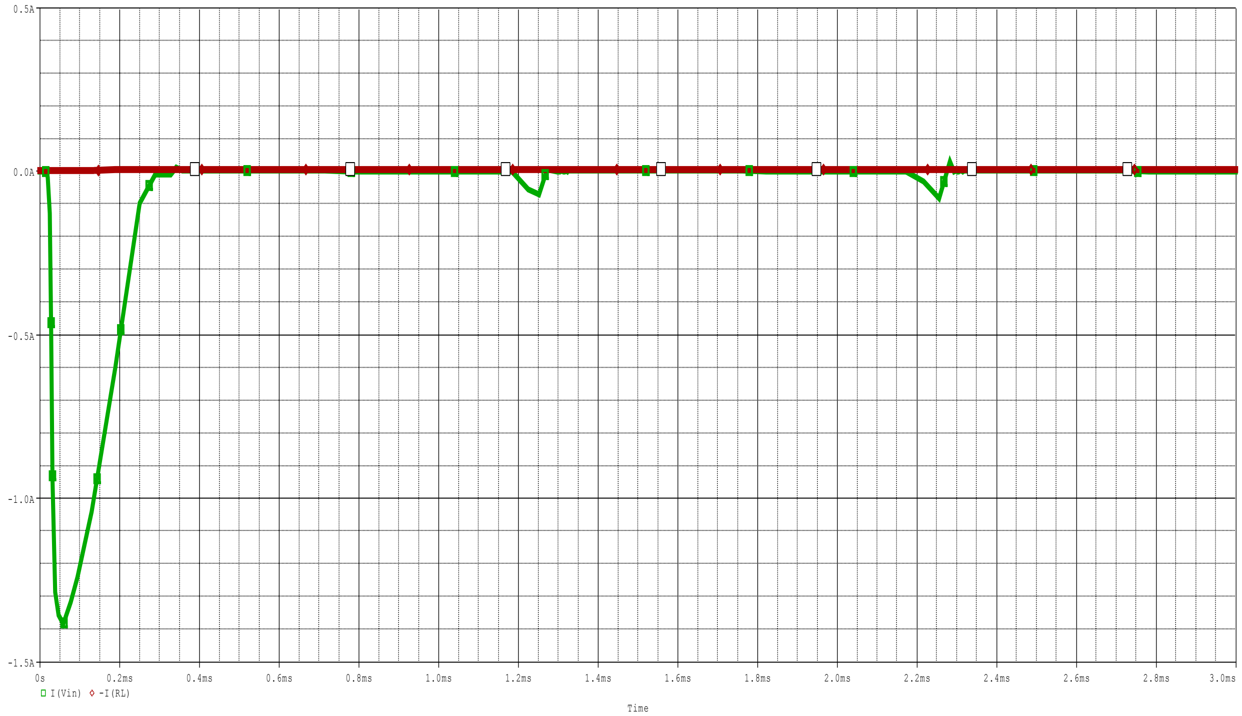


Fig. 2.7(b): Input & Output current

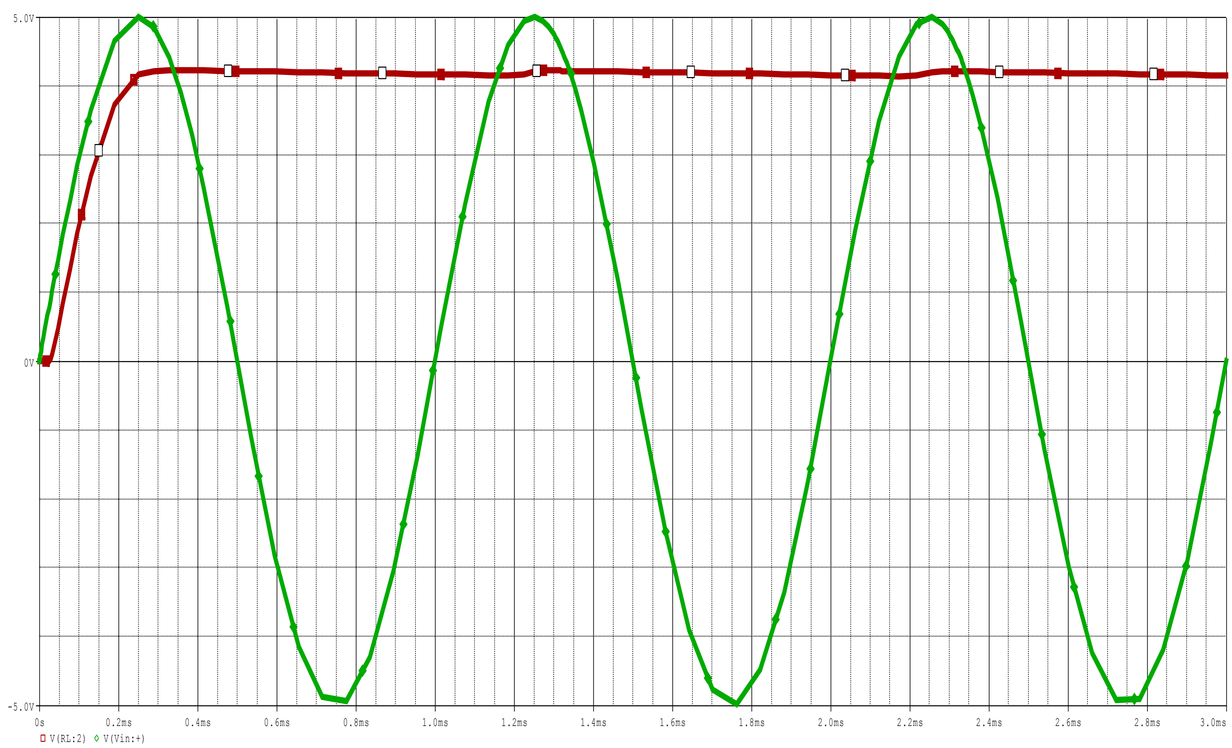


Fig. 2.7(c): Input & Output voltage

2.8.5 Full wave rectifier with Resistance load:

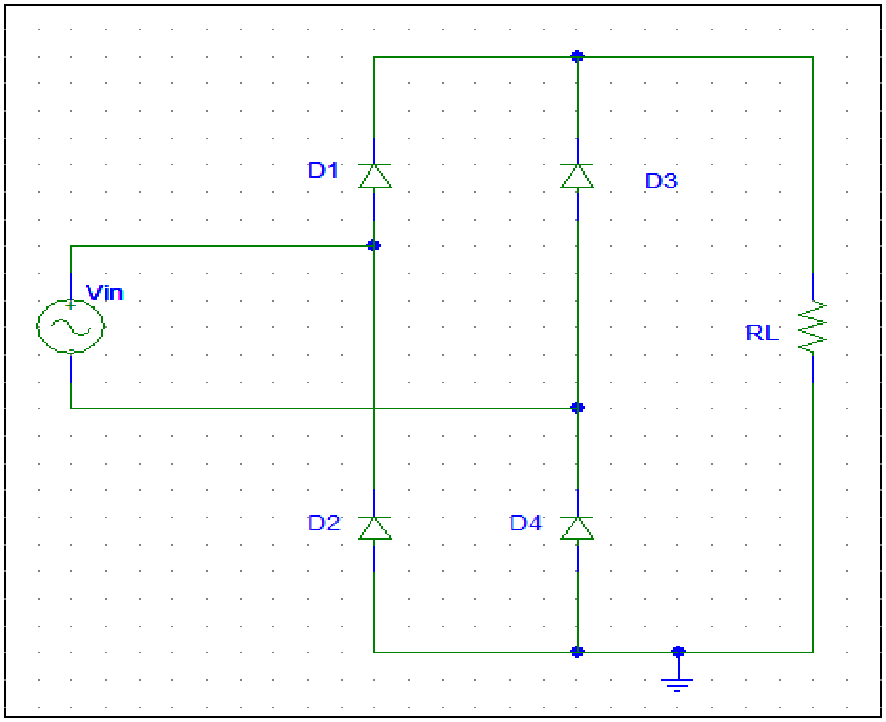


Fig. 2.8(a): Full wave rectifier with Resistance load.

In this part we have showed the half wave rectifier with Resistive and capacitive load circuit in Fig. 2.8(a) and its input and output current Fig. 2.8 (b) as well as input and output voltage in Fig. 2.8(c).

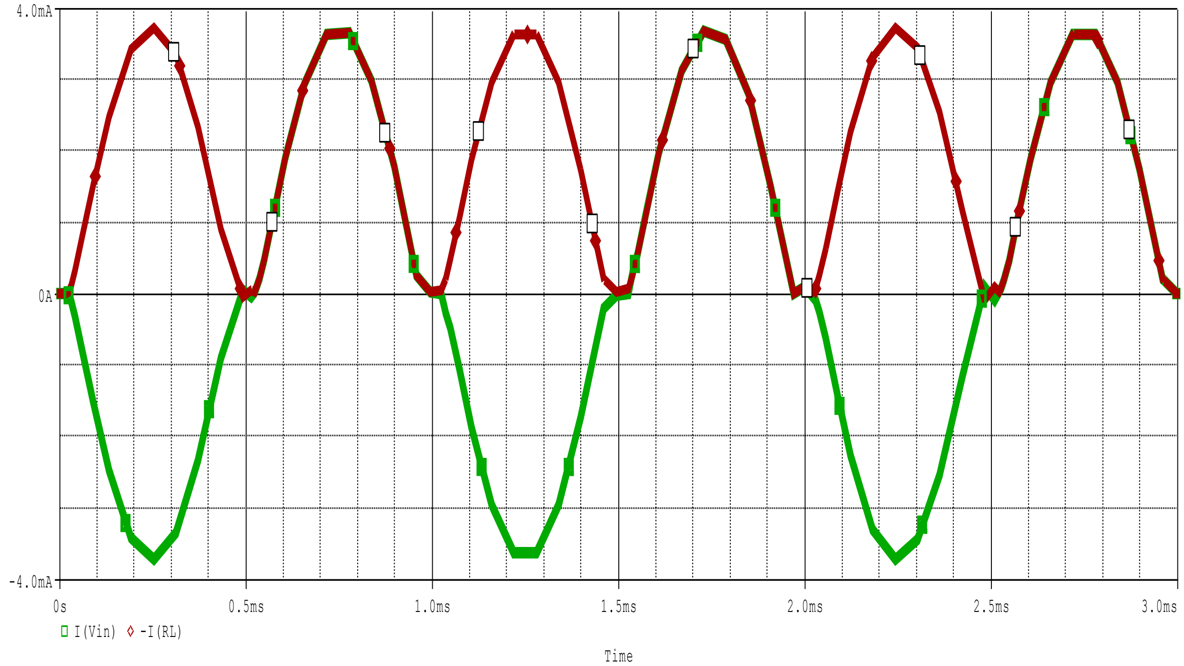


Fig. 2.8(b): Input vs. Output current

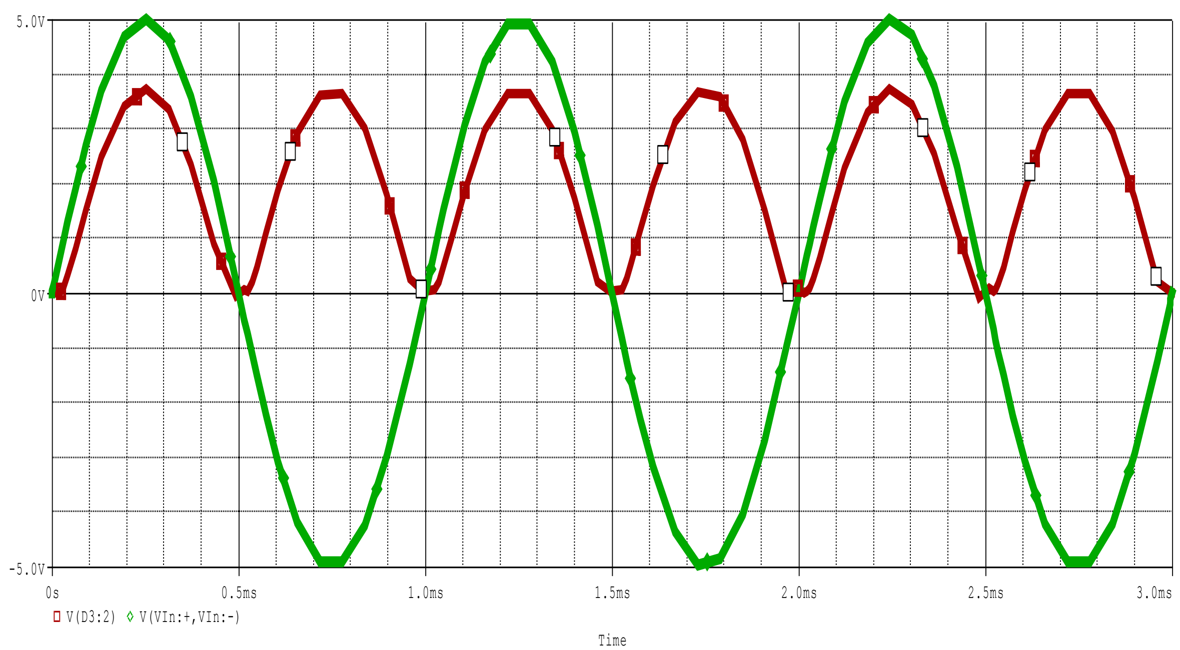


Fig. 2.8(c): Input vs. Output voltage

2.8.6 Full wave rectifier with Resistance and Inductance load:

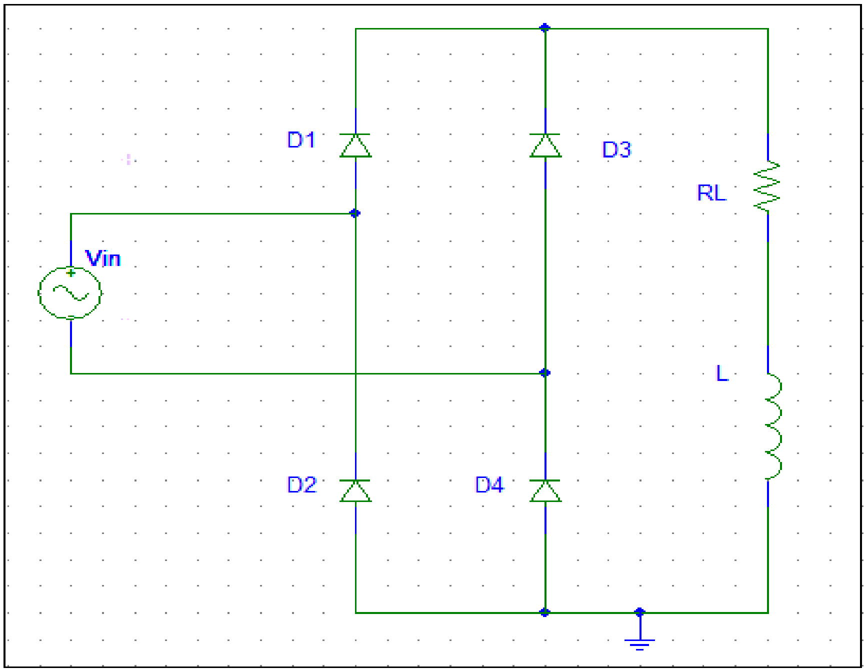


Fig. 2.9(a): Full wave rectifier with resistive and inductive load.

In this part we have showed the full wave rectifier with Resistive and inductive load circuit in Fig. 2.9 (a) and its input and output current Fig. 2.9 (b) as well as input and output voltage in Fig. 2.9 (c).

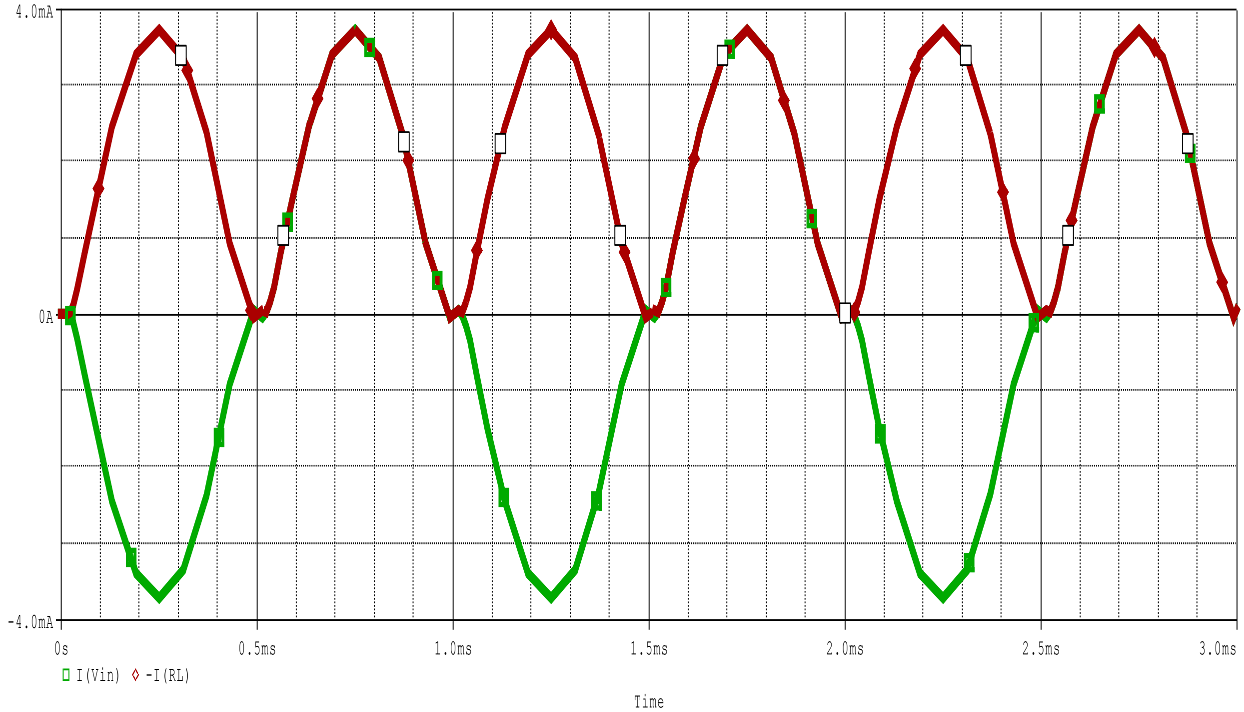


Fig. 2.9(b): Input vs. Output current

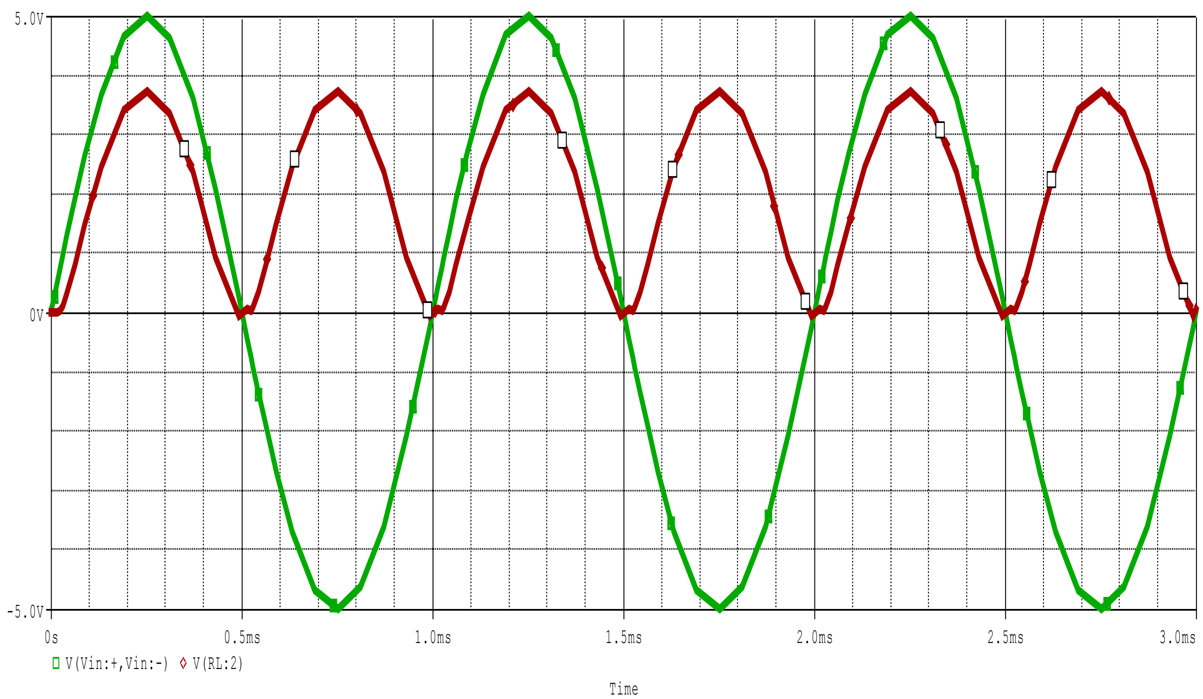


Fig. 2.9(c): Input vs. Output voltage

2.8.7 Full wave rectifier with Resistance, Inductance & Source load:

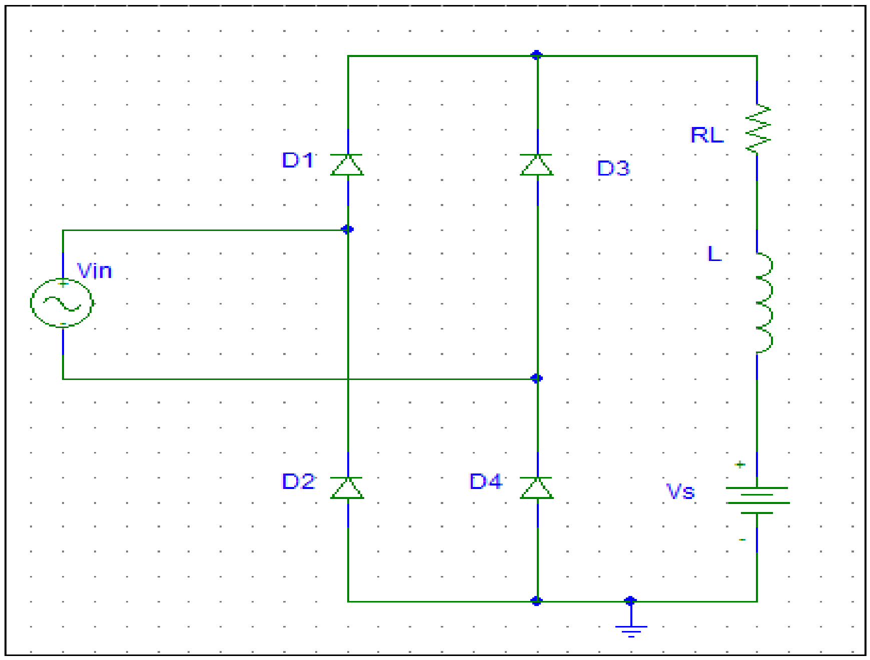


Fig. 2.10: Full wave rectifier with resistive, inductive and source load.

In this part we have showed the full wave rectifier with Resistive, inductive and source load circuit in Fig. 2.10 (a) and its input and output current Fig. 2.10 (b) as well as input and output voltage in Fig. 2.10 (c).

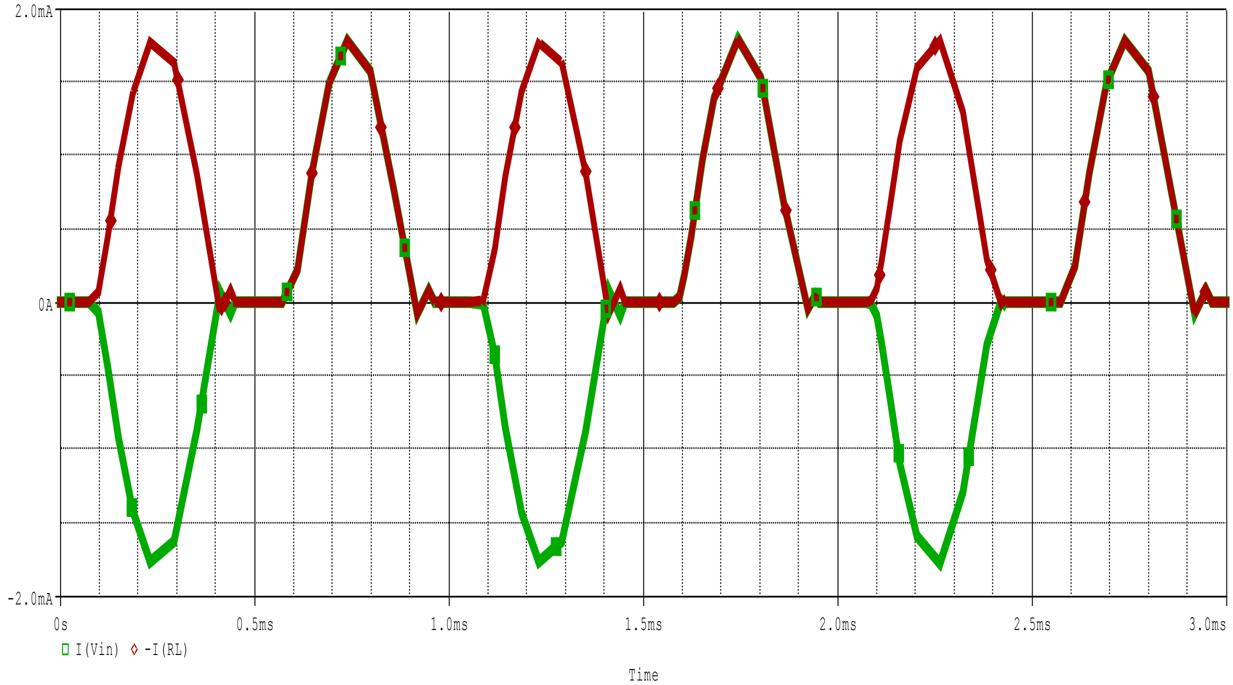


Fig. 2.10(b): Input vs. Output current

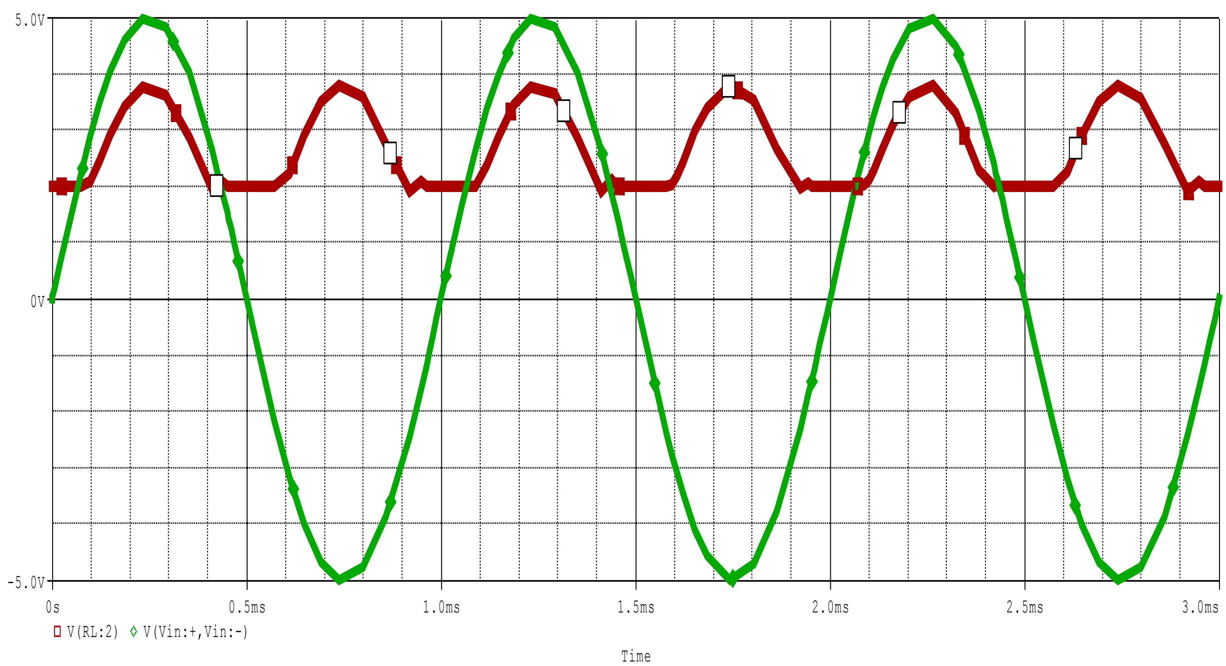


Fig. 2.10(c): Input vs. Output voltage

2.8.8 Full wave rectifier with Resistance & Capacitance load:

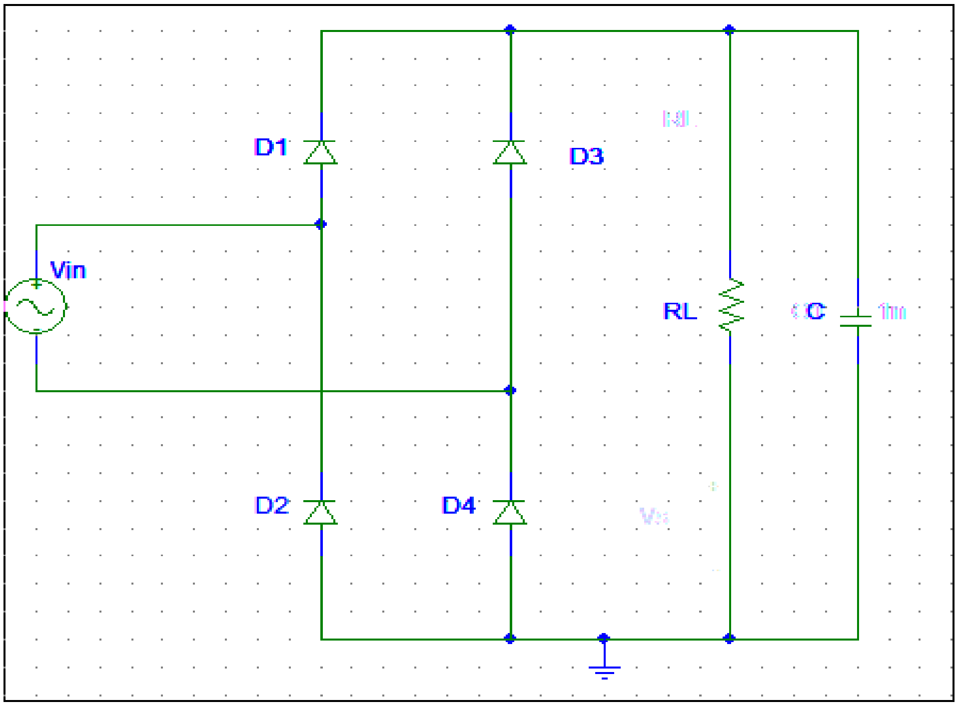


Fig. 2.11(a): Full wave rectifier with resistive and capacitive load

In this part we have showed the full wave rectifier with resistive and capacitive load circuit in Fig. 2.11(a) and its input and output current Fig. 2.11(b) as well as input and output voltage in Fig. 2.11(c).

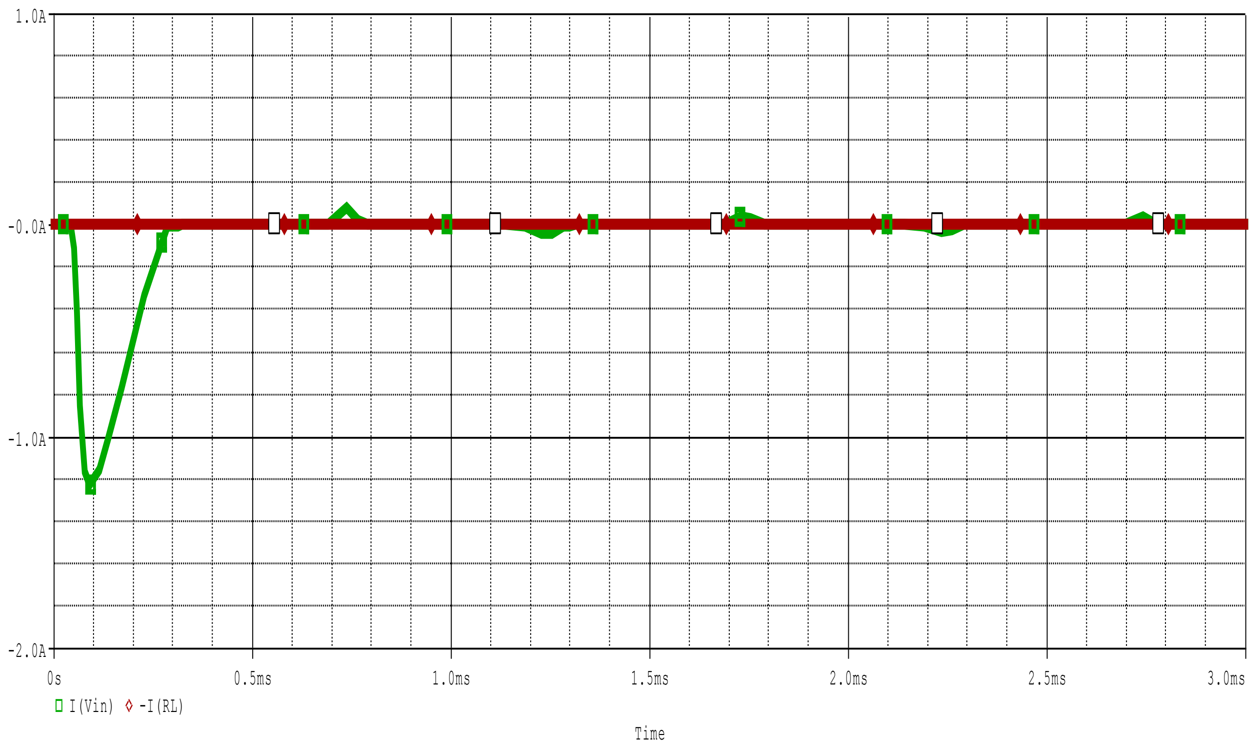


Fig. 2.11(b): Input vs. Output current

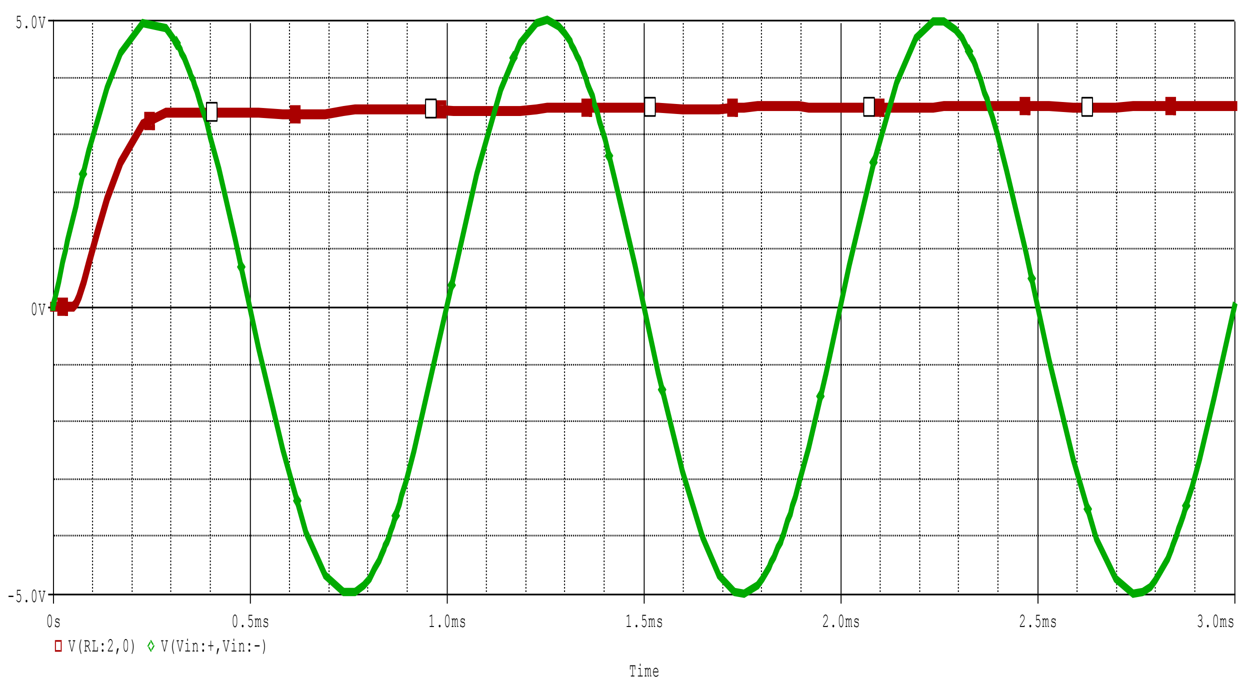


Fig.2.11(c): Input vs. Output voltage

Having so many advantages, rectifiers using switching devices create harmonics caused by the behavior of switching and we know that power factor correction is procedure of diminution of harmonics. This thesis affirms a systematic state space approach to the modeling of boost type DC-DC converter for PFC circuit and reduction of output ripples and harmonics.

Chapter 3
DC-DC converters

3.1 Introduction:

A DC-DC converter, simply known as DC converters are circuits that converts high-frequency power using rapid switching, inductors and capacitors to smoothen noise in DC voltage circuits. It can be considered the DC equivalent of an AC transformer with continuously variable turn's ratio. It is primarily used to step-up or step-down voltage from dc voltage sources. DC-DC converters are used in traction motor control in automobiles, in voltage regulators and DC current source inverters. Before the advent of power semiconductors, DC voltage supply conversion for low power application was done by using a vibrator along-side a transformer and a rectifier. This implies that the DC voltage was converted to AC voltage and again rectified and filtered to convert to DC voltage again. For high power applications, a generator of desired voltage was driven by an electric motor to obtain the required DC voltage. Such means of stepping up or down DC voltage incurred huge expenses and the processes were highly cumbersome to begin with. With the invention of power electronic integrated circuits and solid-state switch-mode circuits, these processes became cheaper and more efficient.

3.2 Applications of DC-DC converters

DC-DC converters have a variety of applications ranging from small electronic circuits to high power supply systems. DC-DC converters has automotive applications. Boost converters are used in hybrid electric vehicles (HEV), adaptive control applications such as in spacecraft, airbuses and jets and in robotics. They are also used in different Battery power systems like cellular devices, laptop computers. In desktop computers, the power supply from the main bus is converted to lower voltages to supply power to USB, RAM and the motherboard. DC converters are used in motor traction control, in regenerative braking of cars, in different consumer electronics like iron, refrigerators, ovens, in different entertainment systems such as audio amplifiers, TV, gaming consoles. They are also used in different industrial applications such as in telecommunication racks and other electronic power drives etc.

3.3 DC-DC converter topologies

DC-DC converters can initially be classified into two divisions according to the mode of using transistors in the converter circuits:

1. Voltage Regulators
2. Switched Linear -mode Voltage regulators

Linear voltage regulators are named thus because of the mode of operation of the transistor used is in linear region. Fig 3.1 shows a basic linear voltage regulator. The output voltage is across the load, $V_0=I_LR_L$. By adjusting the base current in the transistor, the output voltage can be spanned across 0V to near V_s (source voltage). The transistor used in the circuit acts as the variable resistance. In spite of the simplicity of building such a circuit, the inefficiency that the power loss across the transistor counts for can be a big issue in curbing huge losses in high power applications. It can be observed that almost 70-75% of the total power supplied by the source is absorbed by the transistor. Hence this type of converters can be used only low power applications.

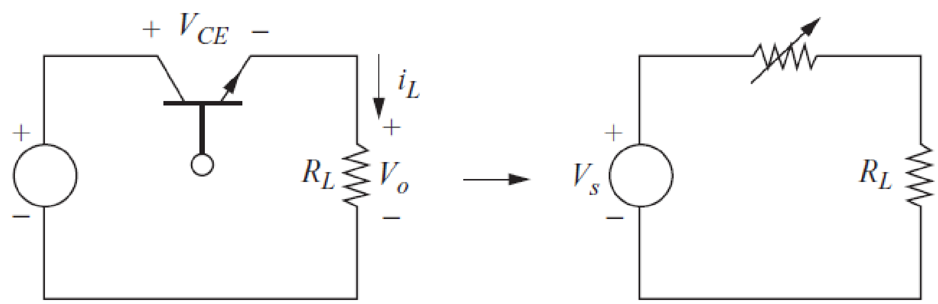


Fig 3.1: Basic Linear Voltage Regulator Circuit

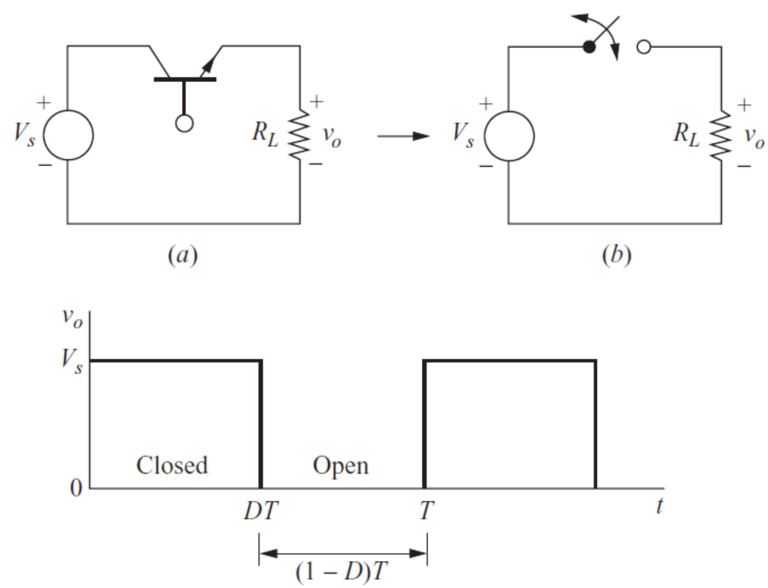


Fig 3.2: Basic Switched-mode Converter

On the other hand, the switched mode voltage regulators operate the transistors as an electronic switch and has proven to be a more efficient and practical alternative to linear voltage regulators. In such converters, the transistor is completely on and completely off. This occurs because the transistor is operated in saturation or cut-off (in case of BJT) or triode and cut off regions (in MOSFETS). Since the transience through the linear region of the transistor is so small and due to the lack of resistive components within the input and output, the dissipation of heat in the circuit is minute and almost negligible and the efficiency is much higher.

A basic switching converter is shown in Fig 3.1, V_o is the output voltage and V_S is the source voltage, T is the time period. D is the duty cycle which indicates for what percentage of the time period T the switch is closed. Let us assume the switch is ideal. If the switch is opened and closed periodically in continuum, the average output voltage will be

$$V_0 = \frac{1}{T}\int_0^T v0(t)dt \quad = \quad \frac{1}{T}\int_0^T vsdt \quad = V_s D$$

The DC component or the average output voltage can be controlled by adjusting the duty cycle as per requirement.

$$\text{Duty cycle, D} = \frac{\text{ton}}{\text{ton}+toff}$$

$$= \frac{t_{on}}{T}$$

$$= t_{on}f$$

Here f is the switching frequency. In real switches, power will still be absorbed as the voltage across it will not be zero, as the switch must still pass through the linear region during every transitional state. Yet the losses are so small, they can be neglected.

There are several Switched- mode power converter topologies that come in isolated and non-isolated varieties. The four most common and useful topologies that are usually used in most cases are:

1. Buck
2. Single-ended primary inductor converter (SEPIC)
3. Boost
4. Buck-Boost

3.3.1 Buck DC-DC converter:

Buck convertors are conventionally used to step down voltages, i.e. where the DC voltages need to be less than the supplied voltages. It simultaneously steps up current so it is also used in systems where high current is needed. In this converter, as in all switched mode converters, the transistor is switched on and off in high frequencies and to maintain a continuous output, the circuit uses the inductor during 'of' periods of the transistor to provide the load with power. It stores the energy during the 'on' period to do as such.

Buck converters can be incredibly efficient with efficiency more than 90% at times which makes it the most popular choice in step down voltage usages. Buck convertors are usually used as POL converter in computers to step down voltages from the main voltages to the USB, CPU and DRAMS. They are also used in Battery chargers, solar chargers, audio amplifiers, motor controllers etc.

Operating principles

Assuming all the components are ideal, S is the transistor operating as a switch, V_s is the supply voltage, I_S is the supply current. V_L is the voltage across the Inductor. The current flowing through the capacitor is I_C. V_b is the output voltage.
We assume D, which is the diode is forward-biased through the entire time period. We also assume that he circuits operates in steady state and the current through the inductor is continuous. We assume that the capacitor is very large and the output voltage is V_0 is constant.

The switching period is T and the switch is closed for time DT and subsequently it opens for time (1-D) T.

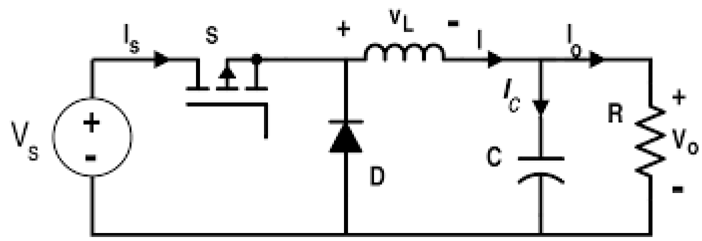


Fig 3.3: Buck Converter Circuit

Analysis for the switch: ON

When the transistor is on, the load is being supplied with current and the diode is reverse-biased as a large positive voltage builds on the diode D. AS the current starts to develop, the inductor builds an opposing voltage in response to the changing current. Due to the voltage drop across the inductor the net output voltage always remains less than the input voltage. Therefore, $V_0 = V_i - V_L$

During this time, the inductor also stores energy in the form of magnetic field. The energy stored across the inductor can be represented as, $E = \frac{1}{2} L I^2$ The increase in current during on state can be given by,

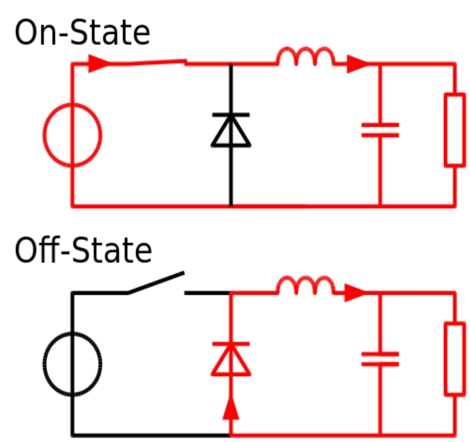


Fig 3.4: Switch on and off states of a buck converter

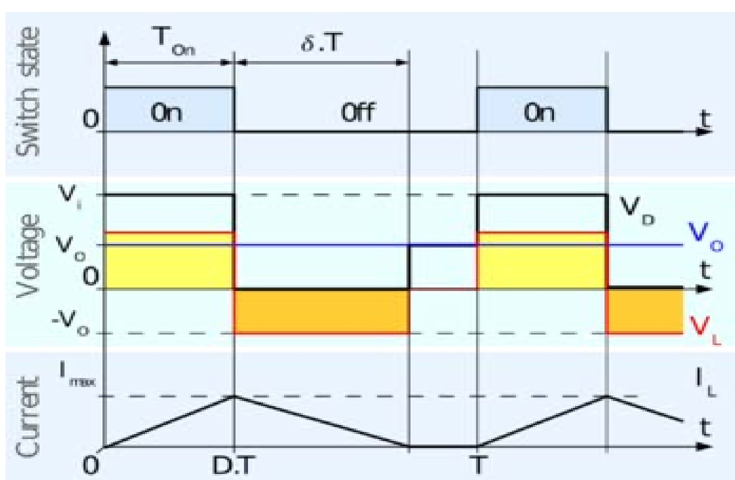


Fig 3.5: Input and Output Voltage and Current waveforms for on and off states

$$\Delta I_{L_{on}} = \int_0^{t_{on}} \frac{V_L}{L} dt = \frac{(V_i - V_0)}{L} t_{on}, t_{on} = DT$$

Analysis during switch: OFF

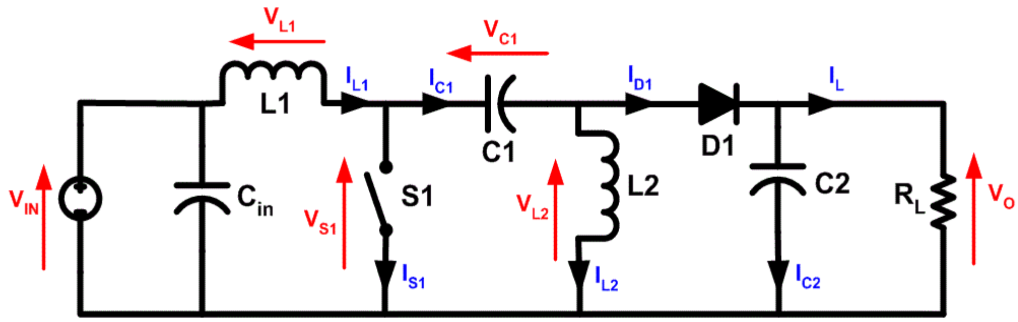
When the switch is opened, the voltage source is isolated by the transistor and current will decrease at a steady rate. The inductor changes polarity and creates a voltage drop and acts as the current source as the stored energy during on state is dissipated adding to the current flowing during on state, culminates to a current much greater than the average current and keeps it flowing until the transistor switches on again.

The decrease in current during off state is given by,

$$\Delta I_{L_{off}} = \int_{t_{on}}^{T=t_{on}+t_{off}} \frac{V_L}{L} dt = -\frac{V_0}{L} t_{off}, \qquad t_{off} = (1-D)T$$

3.3.2 Single ended primary-inductor DC-DC converter (SEPIC)

SEPIC converters is another basic DC-DC converter which can both step up or step down the supply voltage or keep its initial potential, according to the requirements of the user. It is a switched-mode DC converter so the output voltage is adjusted by varying the duty cycle of the transistor switch. It is essentially a boost converter subsequent to a buck boost converter with traits very similar to a usual buck-boost converter but the polarity of the output voltage is the same as that of the supply voltage, i.e. the output is non-inverted, which is essentially not the case for buck boost converters. The specialty of this converter is that the voltage drops to zero immediately as the switch is turned off.



Fig

3.6: SEPIC converter circuit diagram

Operating principles:

The characteristics of the converter circuit can be defined best by reflecting on the input output voltage relationships. In deriving the relationship, we must make some initial assumptions.

- The circuit operates in steady state with periodic voltage and current waveforms.
- The inductors and capacitors are very large and current and voltages across them respectively are constant.
- Switch is closed for time DT and open for (1-D) T.
- The components are ideal.

In continuous conduction mode, during steady state, the average voltage across the capacitor C1 is equal to the input voltage according to the circuit. Hence $V_{c1}=V_{in}$ and according to the circuit this also implies,

$$vL_1 = vL2$$

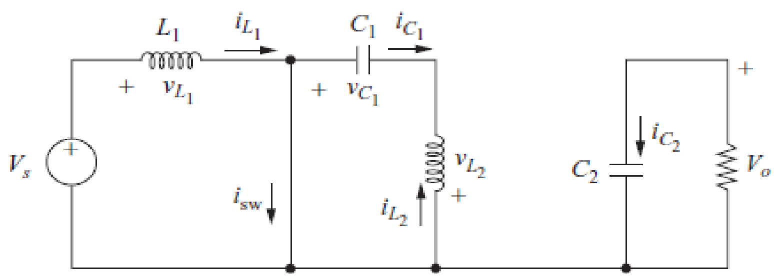
The current through the capacitor C1 is zero as it blocks the DC component. Thus, the only source of load current is the current from inductor L_2.

Thus, the average load current is equal to the current through L2, which indicates that the load current is independent of the supply voltage.

Applying Kirchhoff's law around Vs L_1, C_1 and L_2 gives

$$-V_s + V_{L1} + V_{c1} - V_{l2} = 0$$

The average of these voltages gives



$$V_{C1} = V_s$$

Fig: 3.7 (a): SEPIC converter with switch closed

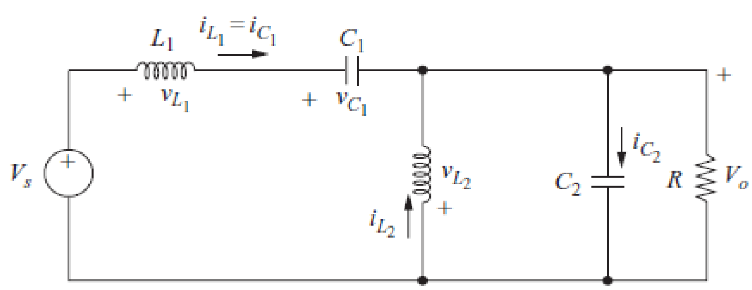


Fig: 3.7(b): SEPIC converter with switch open

The diode D1 is reverse-biased when the switch is closed. Hence the voltage across L_1 for time DT will be equal to V_s.

D1 is forward-biased for the interval (1-D)T (when switch is open). Now applying Kirchhoff's law around the outermost path will give,

$$-V_s + V_L + V_{c_1} + V_0 = 0$$

Assuming V_{C1} remains constant to its value of Vs

$$V_0 = -v_{L_1}$$

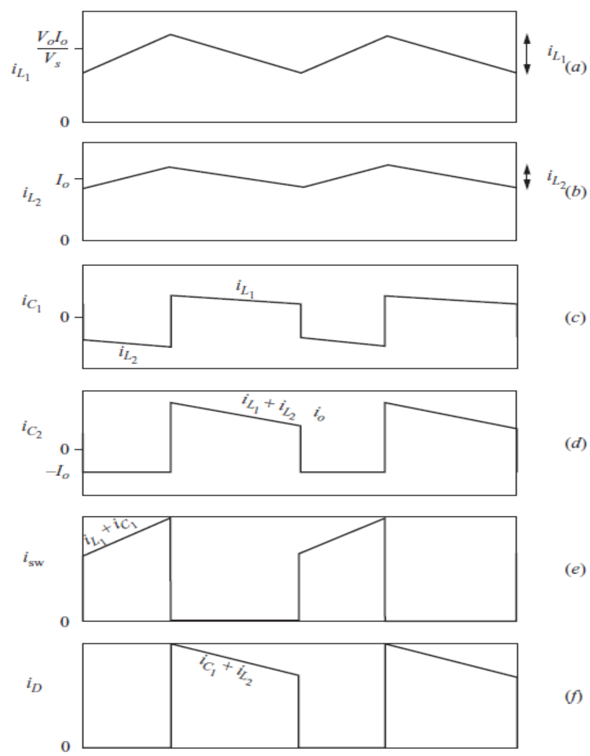


Fig 3.8: Voltage and Current waveforms of SEPIC converters

Average output voltage and Duty cycle:

In periodic operations, the average voltage across an inductor is always zero.

Hence,

$$(V_{L_{1},\ switch\ closed})\ (DT) + (V_{L_{1},\ switch\ open})(1 - D)T = 0$$

$$V_s(DT) - V_0(1 - D)T = 0$$

Hence, average output voltage can be defined by

$$V_0 = V_s(\frac{D}{1 - D})$$

And duty cycle,

$$D = \frac{V_0}{(V_o + V_{s)}}$$

3.3.3 Buck-Boost DC-DC converter:

Buck-Boost converter is a DC-DC converter with circuit topology similar to that of a buck converter and boost converter. It has the capability to produce an output voltage with magnitude equal, greater or less than the input supply voltage. The difference between a SEPIC DC-DC converter with a buck-boost converter is that it gives an output inverse of the polarity of the supply voltage. The output can range from much greater than the supply voltage down to almost zero. The voltage and current relationships can give an insight into the characteristics of the circuit and give a clear intuition on its working principles.

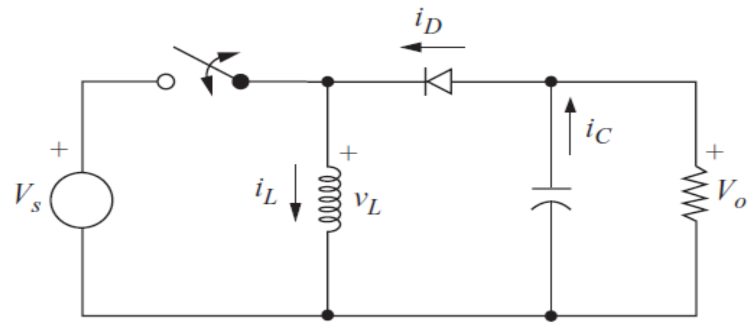


Fig: 3.9: Buck-Boost converter circuit

Operating principles:

Like most DC-DC converters the mainstay of the operating principle of buck boost converter is the reluctance of the inductor to the fast change in current. The instant the switch is closed, the current flows through the inductor as the diode D blocks the current from flowing to the right-hand side of the circuit. Since the inductor immediately follows the supply voltage in the circuit, the inductor accumulates energy at this stage and the capacitor is the only source of current in the load. When the switch is opened the inductor transfers its energy to the capacitor and the load resistor.

In the analysis of such switched-mode power converters, it is essential that some assumptions be made before delving into the circuit operations. The assumptions are as follows:

1. Circuit operates at steady state.
2. The inductor current remains continuous (Circuit is in continuous conduction mode).
3. The capacitor is large enough to assume a constant output voltage.

4. If the duty cycle is D, the transistor switch remains on for time DT and off for time (1-D) T.
5. All the components are ideal.

Analysis for the switch on state:

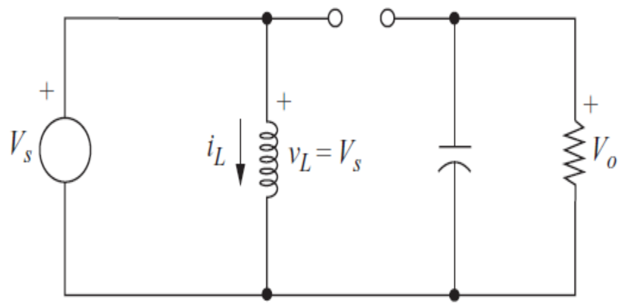


Fig 3.10 (a): Buck boost converter switch on state

As the switch is closed, the voltage across the capacitor can be expressed by,

$$v_L = V_s = L\frac{di_L}{dt}v_L$$

Since the switch is on for time DT, the expression for the current through the inductor can be given by

$$\Delta i_{L,closed} = V_s\frac{DT}{L}$$

Analysis for the switch off state:

As the switch is opened, the supply voltage is isolated from the inductor. The rate of change of current in the inductor becomes constant. The voltage drop across the diode D for the supply voltage is diminished due to the isolation of the supply voltage and the polarization across the diode is inverted. Hence the diode is now on forward bias and current from the inductor and passes into the load and capacitor. At this state the voltage across the inductor is defined by,

$$v_L = V_0 = L\frac{di_L}{dt}$$

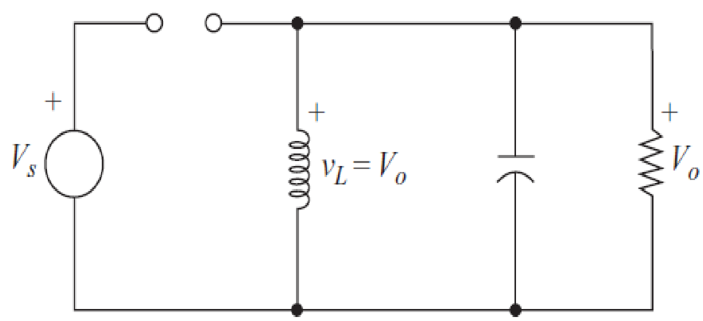


Fig 3.10(b): Buck Boost Converter Circuit switched off

The rate of change in current at this stage is constant and given by,

$$\frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1-D)T} = \frac{V_0}{L}$$

(1-D) T is the time interval for the switch off state and the equation can be further simplified to,

$$\Delta i_{l,open} = \frac{V_0(1-D)T}{L}$$

Output Voltage and Duty Cycle:

Since the operation is assumed to be in steady state, the net change in inductor current will be zero over one period.

$$\Delta i_{L,closed} + \Delta i_{L,open} = 0$$

$$\frac{V_S DT}{L} + \frac{V_0(1-D)T}{L} = 0$$

From this we can derive the equation for the output voltage which is the voltage across the load

$$V_0 = -V_S \frac{D}{1-D}$$

The output voltage can be adjusted by varying the Duty Cycle according to the voltage requirement. The relationship between the input/output voltages and the duty cycle is given by

$$D = \frac{|V_0|}{(V_S + |V_0|)}$$

3.3.4 Boost DC-DC converter

The Boost converter is a DC-DC switched-mode, non-isolating converter that provides with a larger output voltage than the supplied input voltage. The boost topology is popular among its DC-DC converter alternatives because of its steady and even hauling of current in its Continuous conduction mode and which is why boost converters are used mostly in Power Factor Correction (PFC) circuits. Boost converters has eliminated the need for battery stacking to achieve higher voltages and provided an easier, cheaper and space saving alternative to attain such. We shall discuss different facets of the boost converter a little more rigorously than the other converters since it is the primary concern of this research.

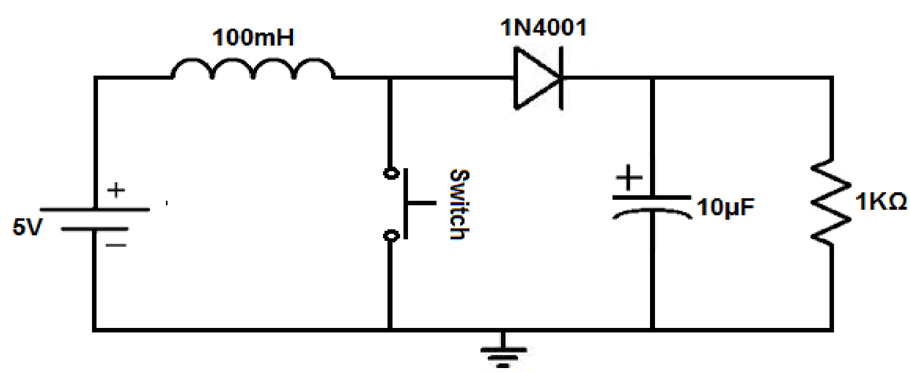


Fig 3.11: Boost Converter

Operating Principle:

Like the buck and buck-boost converters, the cornerstone of the boost topology is the inductor's reluctance to admit the rapid change in current. The response against the current is the energy that builds up and contained in the inductor in the on stage and subsequently released during the off state.

For comprehension of the voltage and current relationships of the boost converter, it is essential that some assumptions be made. For this analysis, the following assumptions are made:

- The circuit exists in steady state condition
- Components are ideal hence parasites are neglected.
- The circuit occurs to be in continuous conduction mode. Current through inductor is continuous.
- Capacitor is very large, the voltage at the load is constant
- Switching period is T and Duty Cycle is D. The switch is open for time (1-D) T and closed for time interval DT.

Analysis for the switch closed:

As soon as the switch is closed, current from the supply voltage moves clock-wise and the diode is reverse-biased. The polarity on the left side of the inductor is positive. Applying Kirchhoff's voltage law around then inductor, source and switch we get,

$$v_L = V_s = L\,\frac{di_L}{dt}$$

di_L/dt is the rate of change of the inductor current and a constant, so it increases almost linearly until the switch is opened. The above equation can be rearranged to the following,

$$\frac{\Delta i_L}{\Delta T} = \frac{\Delta i_L}{DT} = \frac{V_S}{L}$$

So, the expression for the inductor current when switch closed is

$$\Delta i_{L,\ closed} = \frac{V_S DT}{L}$$

Analysis for the switch open:

Once the switch is open, the inductor keeps supplying the electric current from the energy it bided during the switch closed period. The polarity on the inductor is inverted and the positive voltage drop across the diode makes it forward biased and provides a path for the current from the inductor.

Now, the voltage across the inductor can be defined by

$$v_L = V_S - V_0 = L\frac{di_L}{dt}$$

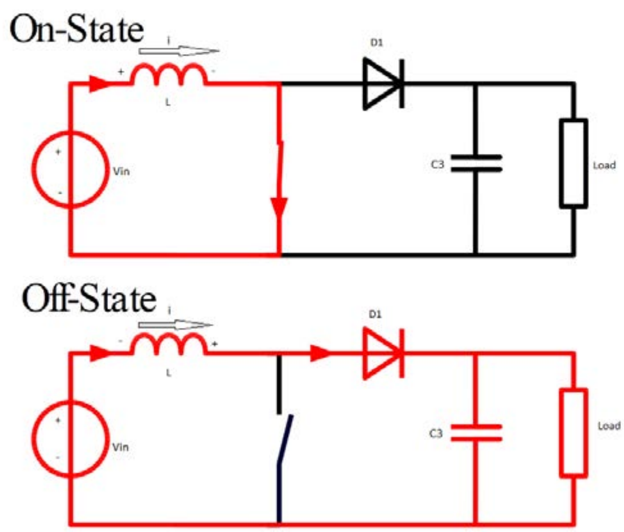


Fig 3.12: Boost converter at on and off states

From the above equation, we can see that the inductor current is constant $di_L/dt = (V_S - V_0)/L$. SO the change in current is linear. From this we can derive the equation of current for the interval (1-D) T which is the time interval for switch open state.

$$\Delta i_{L,\ open} = (V_s - V_0)\ (1-D)\ T/L$$

We already know that at steady state the current through the inductor over a time period T is zero. From that assumption, we can derive:

$$\Delta i_{L,\ closed} + \Delta i_{L,\ open} = 0$$

$$V_s \frac{DT}{L} + (V_s - V_0)\ \frac{(1-D)T}{L} = 0$$

From this equation, we can derive the expression for the output voltage:

$$V_0 = \frac{V_S}{(1-D)}$$

Which is also the relation of the Duty Cycle to the input output voltages of the circuit. From this equation, it is evident that increase in the duty ratio will result in a larger output than the supply voltage and the output voltage cannot be lower than the supply voltage.

The average power supplied by the input is equal to the average power absorbed by the load. Which implies:

$$V_0 I_0 = V_S I_L = \frac{V_0^2}{R}$$

$$V_S I_L = \frac{V_0^2}{R}$$

$$= \frac{\left[\frac{V_S}{(1-D)}\right]^2}{R}$$

From the above expression, the expression of I_L is obtained as such:

$$I_L = \frac{V_S}{(1-D)2\,R} = \frac{V_0 I_0}{V_S}$$

The maximum and minimum inductor currents can be derived by using the average value of inductor currents ,

$$I_{max} = I_L + \frac{\Delta i_L}{2}$$

$$= \frac{V_S}{(1\text{-}D)^2 R} + \frac{V_S DT}{2L}$$

$$I_{min} = I_L - \frac{\Delta i_L}{2} = \frac{V_S}{(1\text{-}D)^2 R} - \frac{V_S DT}{2L}$$

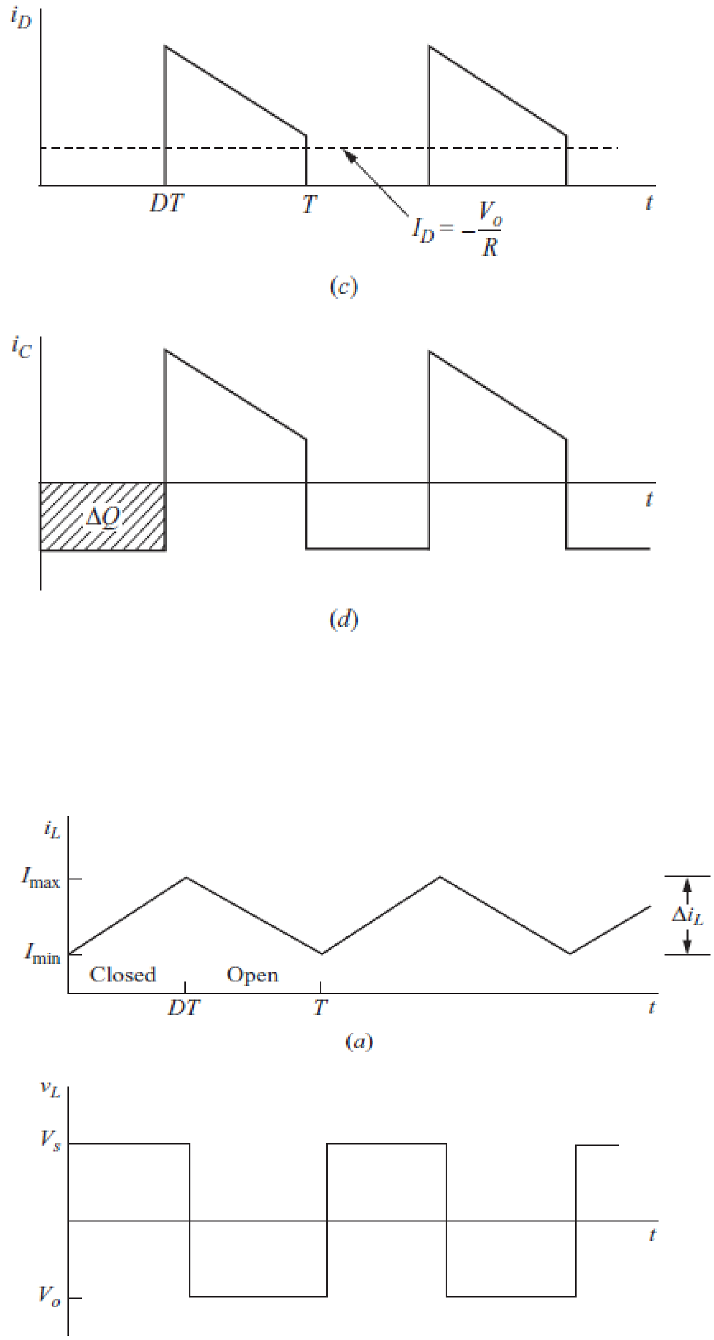


Fig 3.13: Boost converter Current and Voltage waveforms

The Expression for inductor current in discontinuous mode can be found by solving the above equation for $i_{min} = 0$.

$$\frac{V_S}{(1\text{-}D)^2R} - \frac{V_SDT}{2L} = 0$$

$$\frac{V_S}{(1\text{-}D)^2R} = \frac{V_SDT}{2L} = \frac{V_SD}{2Lf}$$

F is the frequency of the transistor switch. Now the minimum inductance required for continuous current in boost converter is $L_{min}= \frac{D(1\text{-}D)^2R}{2f}$

In conclusion, we can say that we have discussed here about different types of DC-DC boost converters and we have choosed DC-DC boost type converter because of covinient switching position and it need less inout size filtera required due to indutance situated at input side.

3.4 State Space Representation and Small Signal Analysis

For developing a closed loop control method for switching converters, small signal analysis is essential to model the required system. With the help of small signal model (SSM) we can derive the necessary transfer functions required of the DC-DC converter to determine the appropriate responses of the converter and desired controller in the closed loop system. Small signal analysis helps in identifying the deviations around the steady state operating point which is required in ripple reduction. The general state space representation is given below:

$\dot{x}$ =Ax + Bu

y=Cx + Du

A= characteristics property of a matrix

B= input matrix gain related

Y= control variable

D= feed forward matrix

$\dot{x}$ = prediction for what will be the next value

Some assumptions are to be made for the small signal analysis of boost converter:

1. Current through the inductor is considered constant
2. All components are ideal
3. The switching period is T, switch is closed for time DT and open for time (1-D)T. Here D is the duty cycle.
4. Capacitor is large hence output voltage is constant.

For steady state model:

$\dot{x} = 0$

D=D

$V_g = V_g$

$i_s = I_S$

Input vector, $u_1 = [V_s]$, $u_2 = [i_v]$

State vector, $x = \begin{bmatrix} i_L \\ v_c \end{bmatrix}$

Parameters: L, C, R

For DT interval (switch ON state)

L:

$$L\frac{di_L}{dt} = v_s$$

$$\frac{di_L}{dt} = \underbrace{v_s\left(\frac{1}{L}\right)}_{\boxed{\text{INPUT}}} + \underbrace{0 \times i_L\left(\frac{1}{L}\right) + 0 \times v_c \times \left(\frac{1}{L}\right)}_{\boxed{\text{STATE}}}$$

C:

$$c\frac{dv_c}{dt} = i_v - \frac{V_c}{R}$$

$$\frac{dv_c}{dt} = -v_c\left(\frac{1}{RC}\right) + \frac{1}{C}(i_v) + \frac{1}{C} \times 0 \times i_L$$

$$= -\underbrace{v_c\left(\frac{1}{RC}\right) + \left(\frac{1}{C}\right) \times 0 \times (i_L)}_{\boxed{\text{STATE}}} + \underbrace{\frac{1}{c}(i_v)}_{\boxed{\text{INPUT}}}$$

$$\frac{di_L}{dt} = \dot{x}_1,$$

$$\frac{dv_c}{dt} = \dot{x}\ ,$$

$$x_1 = i_L,$$

$$x_2 = V_c,$$

$$u_1 = V_g$$

$$u_2 = i_V$$

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix} \begin{bmatrix} v_g \\ i_v \end{bmatrix}$$

$$\boxed{\dot{x_1} = A_1 \ .\ x_1 + B_1 \ .\ u_1}$$

For (1-d)T interval (switch OFF state)

$$\text{L: } \frac{L di_L}{dt} = V_g - V_c$$

$$\frac{di_L}{dt} = -V_c\left(\frac{1}{L}\right) + 0 \times i_L + V_s\left(\frac{1}{L}\right)$$

$$\text{C: } C\frac{dv_c}{dt} = i_L - \frac{V_c}{R} + i_V + 0 \times V_g$$

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & \frac{1}{RC} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix}$$

$$\boxed{\dot{x} = A_2 \,.\, x + B_2 \,.\, u}$$

Here,

$$\frac{di_L}{dt} = \dot{x}_1,$$

$$\frac{dv_c}{dt} = \dot{x}_2\,,$$

$$x_1 = i_L, x_2 = V_c,$$

$$u_1 = V_g$$

$$u_2 = i_V$$

For deriving the steady state model, we must assume that,

$\dot{x} = A\,.x + B.u = 0$

Circuit averaging

$\dot{x_1} = A_1 x + B_1 u$

$\dot{x_2} = A_2 x + B_2 u$

Using the state space averaging technique, we can find the complete dynamic state space representation of the boost converter circuit from the above equations. The final representation is given below:

$$\dot{x} = [\,A_1 d + A_2\,(1-d)]\,[x] \;\; + \;[B_1 d + B_2\,(1-d)]\,[u]$$

The order on the equation is 2 (L, C)

Therefore, there will be 2 differential equations.

Input Vector, U = [v_g]

State Vector, x = $\begin{bmatrix} i_L \\ V_c \end{bmatrix}$

Parameters: R_1, L, C, R_2

$$L: L\frac{di_L}{dt} = V_L = -V_{R_1} - V_c + V_g$$

$$= V_g - i_L R_1 - V_c$$

$$\frac{di_L}{dt} = -\underbrace{\frac{R_1}{L}(i_L) - \frac{1}{L}\,V_c}_{\text{State Variable Component}} + \underbrace{\frac{1}{L}\,V_g}_{\text{Input Variable Component}}$$

$$C = C\frac{dv_C}{dt} = i_L - \frac{V_C}{R_2} + 0 \times V_g$$

$$\frac{dV_C}{dt} = \frac{1}{C}\underbrace{i_L \;\; -}_{\text{State}} \;\; \underbrace{\frac{1}{C}\left(\frac{1}{R_2}\right)(V_c)}_{\text{Input}}$$

$$\begin{bmatrix} \dot{i}_L \\ \dot{V}_c \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L} & \frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_2 C} \end{bmatrix} \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [V_g]$$

$$\boxed{\dot{x} \;=\; A \;.\; x \;+\; B \;.\; u}$$

For steady state we assume,

$$\dot{x} = A\,.\,x + B.u = 0$$

Equilibrium condition, d=D

$$v_g = V_g, \qquad i_g = I_g$$

Large signal= small signal + steady state

Therefore, $\quad i_L = I_L + i_L$

$$\hat{A} = A_1 d + A_2(1-d)$$

$$= \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} d + \begin{bmatrix} 0 & \frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} (1-d)$$

$$= \begin{bmatrix} 0 & \frac{1-d}{L} \\ \frac{1-d}{C} & -\frac{1}{RC} \end{bmatrix}$$

$$\hat{B} = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix} \mathrm{d} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix} \text{(1-d)}$$

$$= \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix}$$

Basic state space averaged model:

$$\dot{x}_1 = \frac{L}{1-d}\dot{x} + x_2$$

$$\dot{x}_2 = \frac{C}{1-d}\dot{x}_2 + \frac{x_2}{R(1-d)}$$

Small signal model:

For switch ON

$$\frac{d\hat{x}_1}{dt} = -\frac{1-D}{L}\hat{x}_2 + \frac{\hat{d}x_{2_0}}{L} + \frac{\hat{U}_1}{L}$$

$$= L\frac{d\hat{x}_1}{dt} = -(1-D)\hat{x}_2 + \hat{d}x_{2_0} + \hat{u}$$

Similarly for switch OFF

$$\frac{d\hat{x}_2}{dt} = (1-D)\hat{x}_1 - x_{1_0}\hat{d} - \frac{\hat{x}_2}{R} + \hat{u}_2$$

Small Signal Averaged State Space Equation:

$$\dot{\hat{x}} = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{L} & -\frac{1}{RC} \end{bmatrix}\hat{x} + \begin{bmatrix} \frac{x_{2_0}}{L} \\ -\frac{x_{1_0}}{C} \end{bmatrix}\hat{d} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} \hat{u}_1 \\ \hat{u}_2 \end{bmatrix}$$

Here,

$$i_L = I_L + \hat{\imath}_L$$

$$v_g = V_g + \hat{v}_g$$

$$u_1 = \hat{v}_s, \quad u_2 = \hat{\imath}_v$$

$$\hat{x}_1 = \hat{\imath}_L\,, \qquad \hat{x}_2 = \hat{v}_c$$

$$x_{2_0} = V_c \;\; and \;\; x_{1_0} = \;\; I_L \;\; \text{(Steady state part)}$$

By the dint of these expressions, we can arrive at the transfer functions necessary to obtain the bode plot and root locus to design the closed loop controller.

Chapter 4

Open Loop Analysis

4.1 Introduction:

For most part of the power electronic systems, the power (i.e. input and output) instantaneously change with respect to the time, input voltage, resistance and so on. In addition, they are also not accurately identical with each other. Therefore, for providing a good relation between input and output is a very difficult task, but it is not impossible. For that reason, we analyze and simulate open loop system for DC to DC Boost converter to get proper boost up output voltage by varying input voltage and load resistance.

Firstly, how we try to control the switched mode power convertor is an important issue to look at. We have to look at the switched mode convertor as an open loop system, we need to control it develop controllers such that we get outputs with a certain performance conciliation. As a result, that is the aim and towards that aim we will develop and develop the subject.

4.2 Objective:

The objective is to design a boost converter that converts 6 V input to 12 V output. The switching frequency is 20 kHz. Generally, a faster switching frequency leads to small size of components, but the switching losses in the circuit increase.

The specifications of the boost converter are listed as follows:

Input voltage, V_{in} = 6V

Nominal output voltage, V_{out} = 12 V

Input current, I= 0.012 A

Switching frequency, f = 200 kHz

Inductance, L = 120uH

Capacitance, C = 47uF

Duty ratio, D = 0.5

Load resistance, R_L = 10m Ω

R_{esr} = 1m Ω

4.3 Open Loop Model for Single Input DC to DC converter

In this report, Input voltage (6 V) is connected as input source with common inductor through unidirectional switch. We know that switches can be realized by IGBT (Insulated-Gate Bipolar Transistor) or other similar devices due to different conduction cases of diodes and switches, the converter can be operated in buck, boost and buck-boost modes for both positive and negative input power sources deliver power to the output. The configuration of this circuit is designed in such a manner so it will act as a boost converter. In open loop model gate voltage is given on switch IRF540 having constant Duty cycle 0.5. We have used V_{pulse} for controlling switching operation with different parameters for getting load voltage for different values of V_{in} and R_L.

4.4 Analysis of Open Loop Model:

- Changing Load Resistance (RL)
- Changing Input Voltage (Vin)

For the 1st case when it is simulated for different R_L values by setting up a fixed input voltage (Vin=6V) we get different output voltage (Vout). And for the 2nd case again output voltage (Vout) is changing when we do the simulation by setting the other value fixed, R_L=1kΩ & change the input voltage (Vin). For both case duty cycle is fixed.

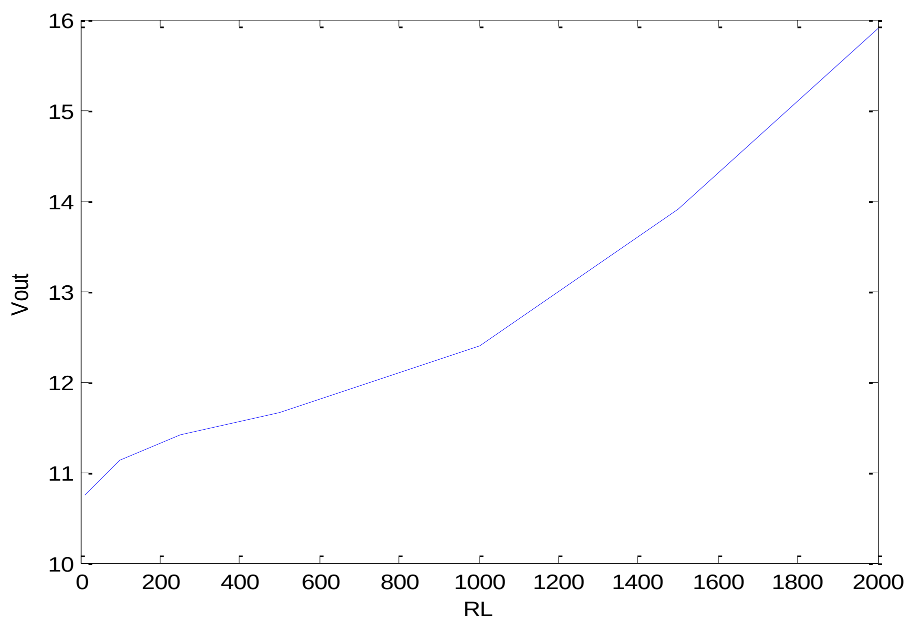


Fig. 4.1: V_{out} vs. R_L

Fig. 4.1 is showing that output voltage is changing while RL is changing. It shows when RL is high Vout is high & it decreases when we use low load resistance (RL).

When R_L is low the fluctuation of output voltage is high. On the other hand when we use high R_L the output voltage acts like almost DC voltage.

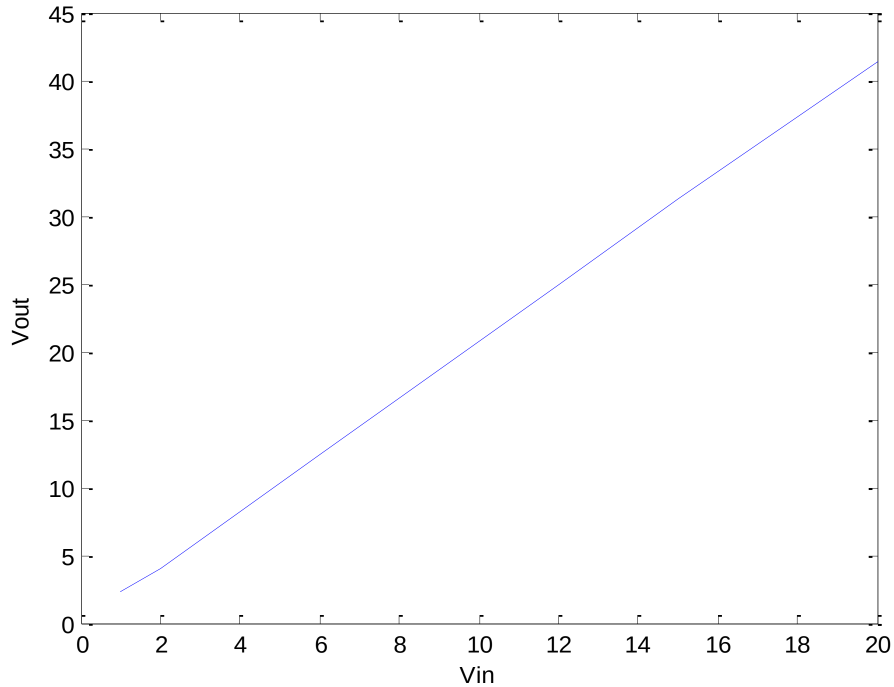
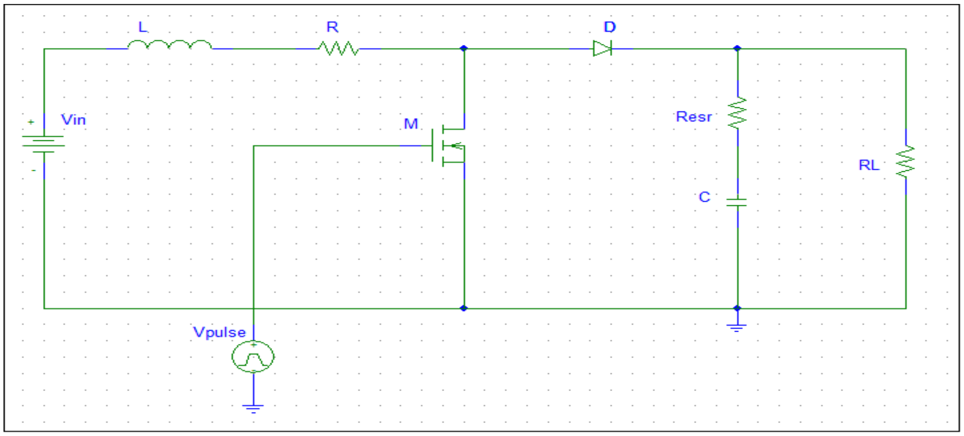


Fig. 4.2: V_{out} vs. V_{in}

Fig. 4.2 is also showing that output of voltage (V_{out}) changes linearly by the change of input voltage (V_{in}). The output voltage gets around double of the input voltage for duty cycle 0.5

4.5 Simulation for open loop analysis:

Circuit Diagram in PSpice:



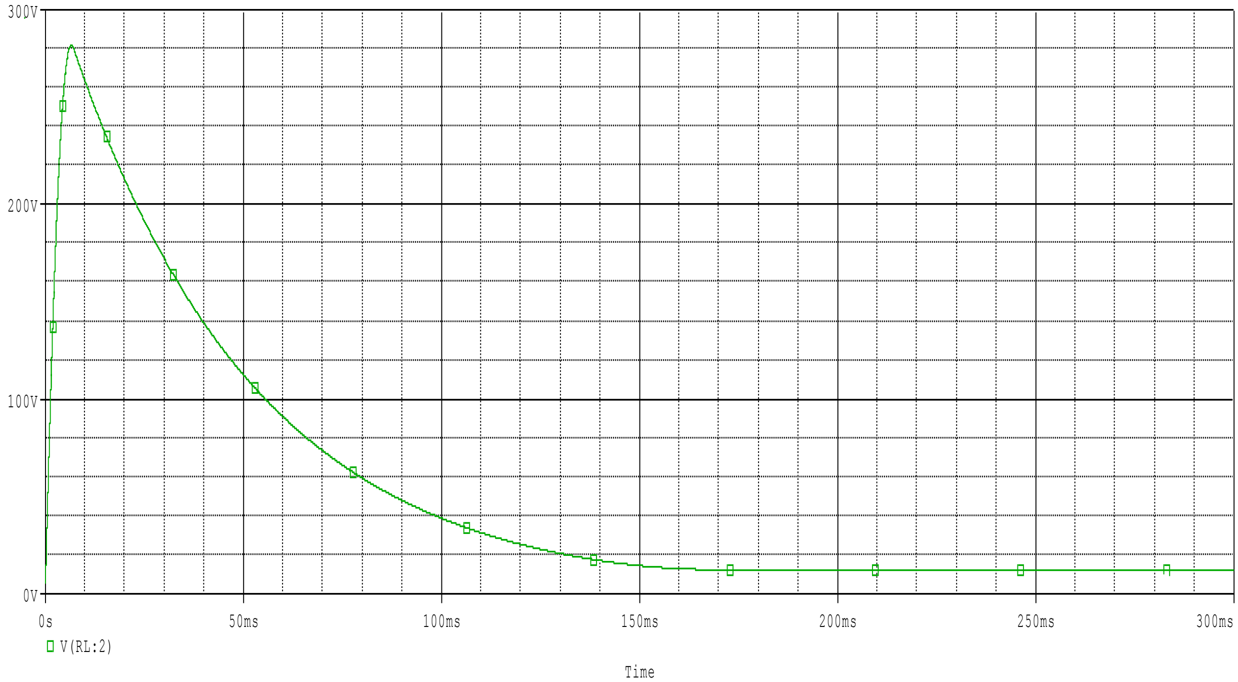


Fig. 4.3: Output Voltage vs Time

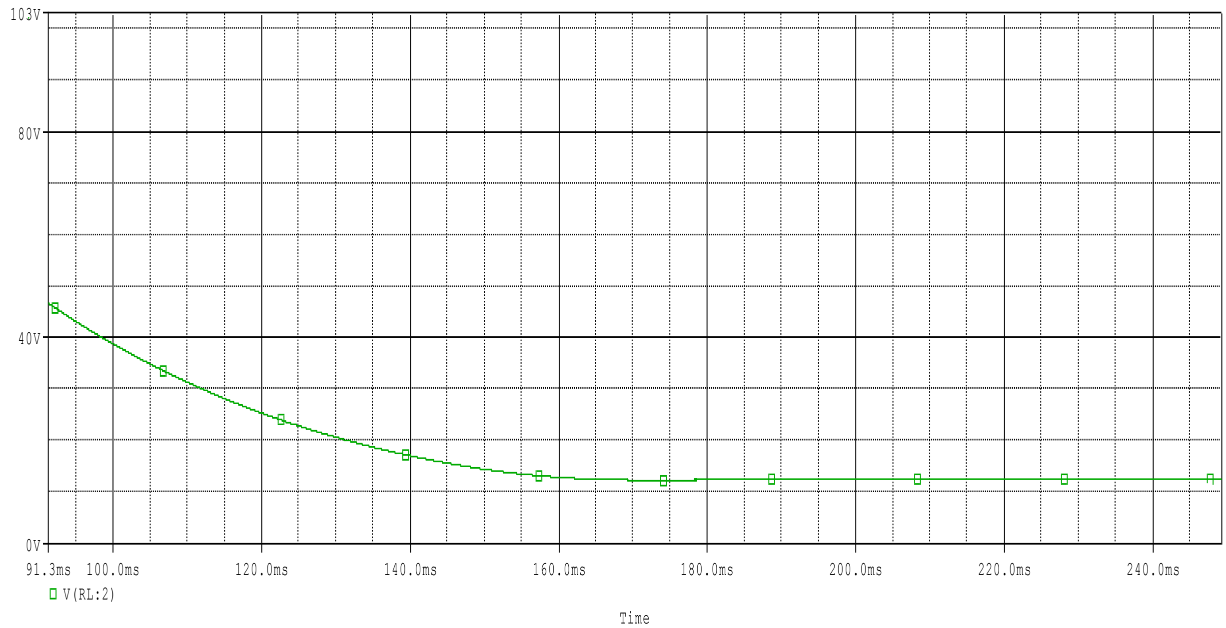


Fig. 4.4: Zoomed View of Fig 4.3

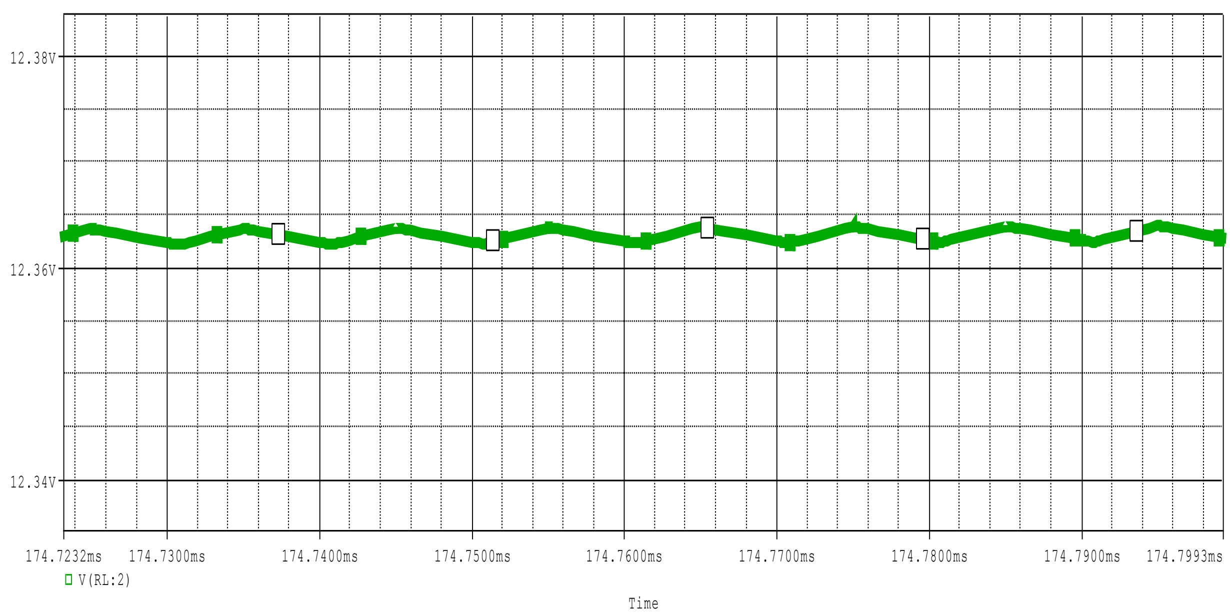


Fig. 4.5: Zoomed view of output voltage when R_L=1kΩ

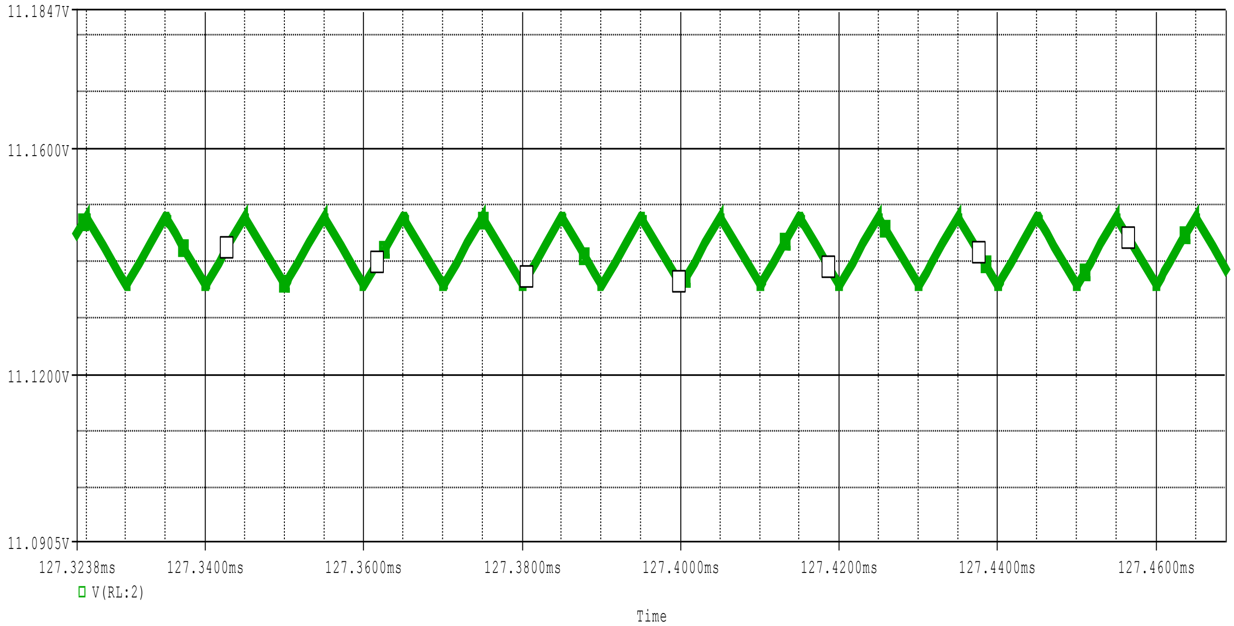


Fig. 4.6: Zoomed view of output voltage when R_L=100Ω

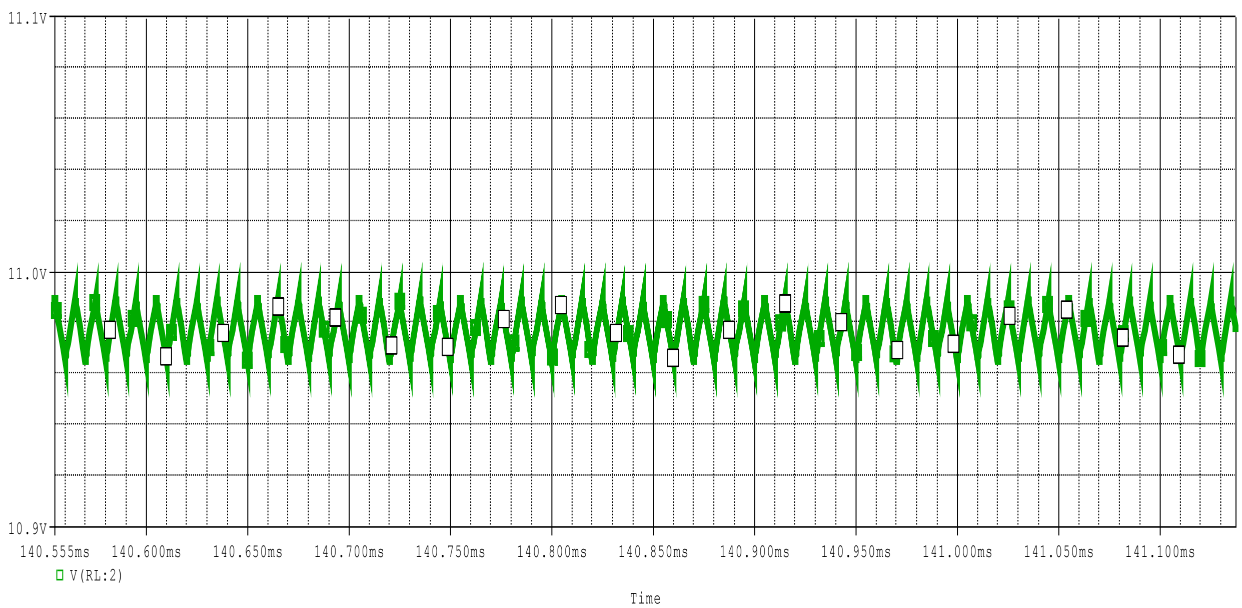


Fig. 4.7: Zoomed view of output voltage when R_L=50Ω

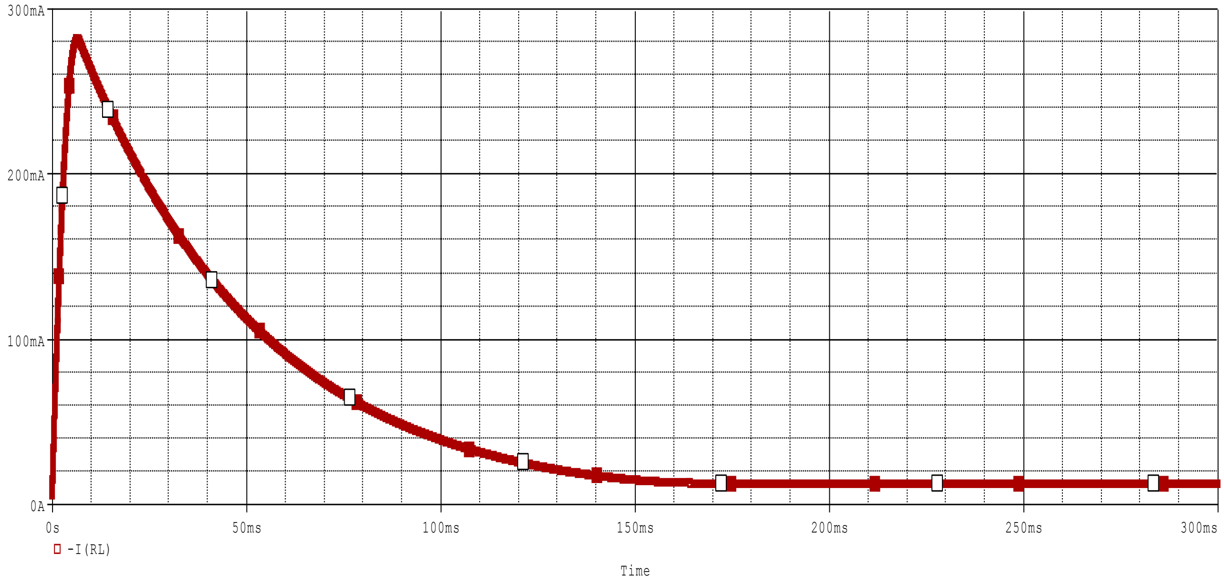


Figure 4.8: Current vs Time

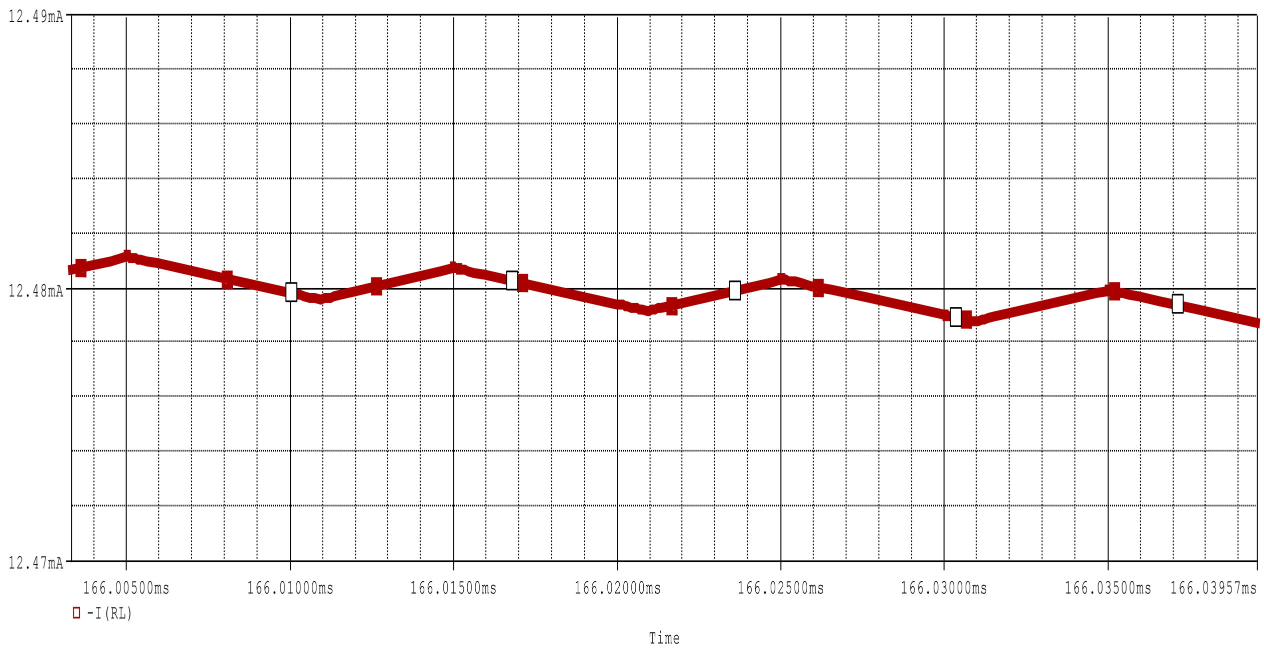
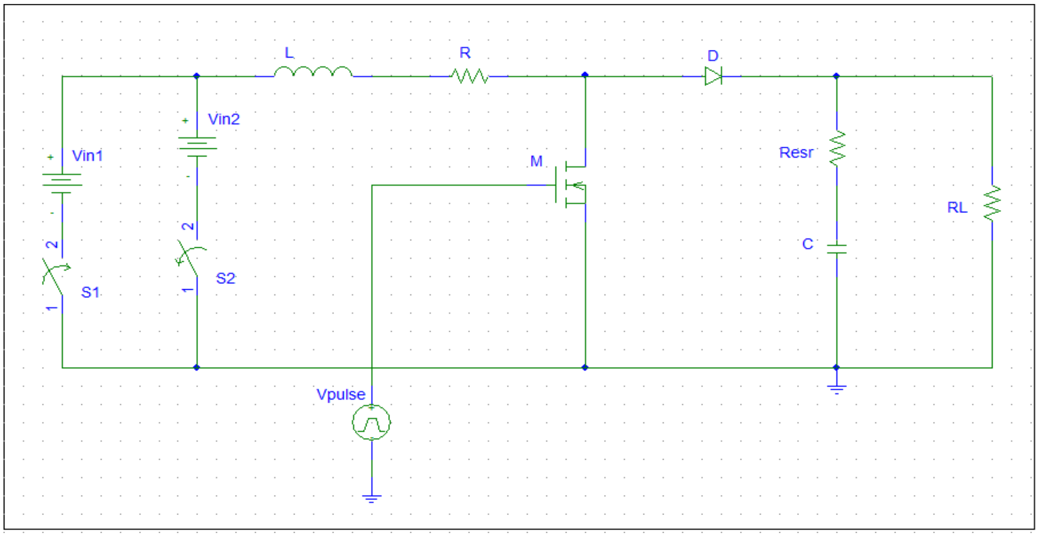


Fig. 4.9: Zoomed View of Fig. 4.8

Boost converter open loop analysis (changing input voltage)



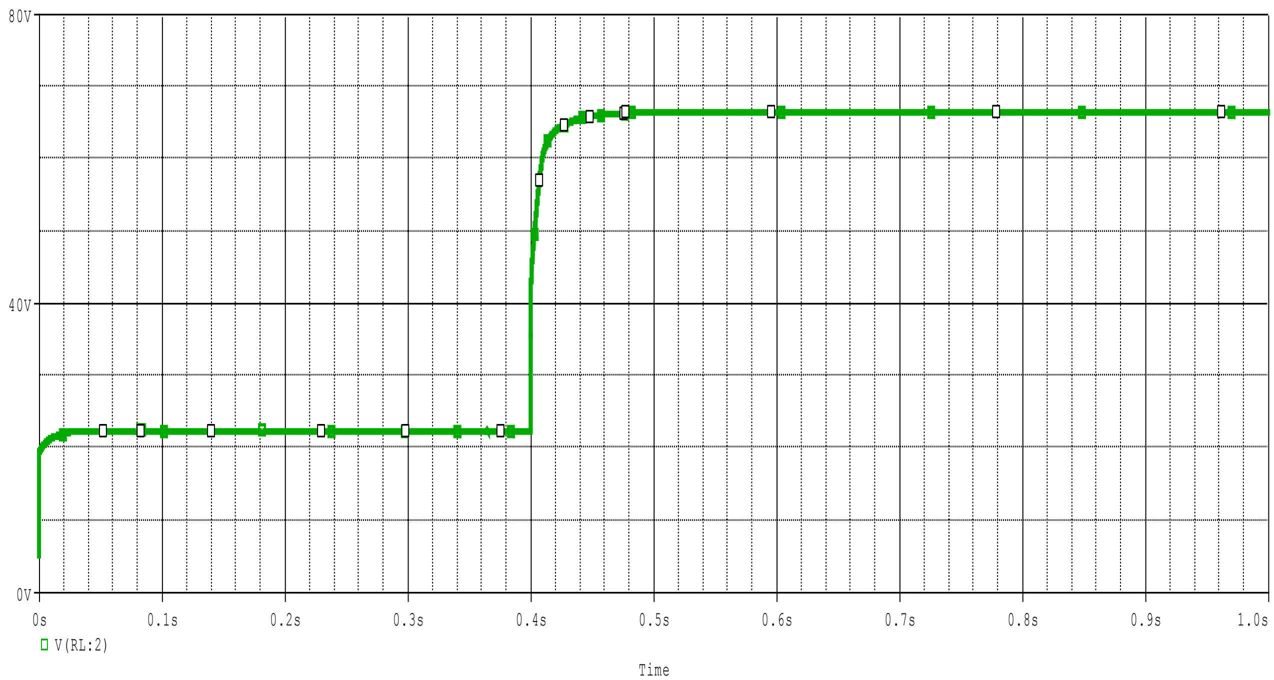


Fig. 4.10: Voltage across R_l

Simulation verification of the performance of proposed converter using input source, switch, MOSFET have been made using PSpice platform. According to the simulation we can observe that V_{out} is changing due to change in V_{in} and R_L. But our converter should give stable and efficient value all the time whatever we give in input and if it is doable to vary duty cycle, we can solve this problem. In this report, we come to the point that open loop system is somehow difficult to maintain constant output voltage and current and that is why we need a systematic control approaches which will be anticipated as controller because controller is better to use in this converter which will vary our duty cycle to maintain steady output, even when the system voltages and currents are more distorted.

Chapter 5
Controller Design

5.1 Introduction:

From the previous chapters we know by analyzing the process of circuit averaging wherein we get the average large signal model, then we get steady state model and the small signal model which we are going to use for the control purposes. We will have Vs as input and output Vo which we are going to control. Duty ratio or duty cycle will be our controlled input and there will be another output y which will be the sensed out and it will carry information about output voltage, we will discuss about it in the following part of our paper. We know the DC-DC converter is represented by the following equations-

$$\dot{x} = Ax + Bu$$

$$y = Cx + Du$$

We can control output voltage or input current of boost converter. For that we have to get the transfer function of the output voltage to the control input which we will consider the d(duty cycle). We get our transfer function by using MATLAB simulation-

Transfer Function of boost converter = $\frac{1063829787.2341}{s^2+21.28s+4.433e007}$

5.2 Gain Margin. Phase Margin and Crossover Frequency:

The gain margin is the amount of gain increase or decrease required to make the loop gain unity at the frequency Wg where the phase angle is –180° (modulo 360°). In other ways, the gain margin is 1/g if g is the gain at the –180° phase frequency. Likewise, the phase margin is the difference between the phase of the response and –180° when the loop gain is 1.0. The frequency Wp at which the magnitude is 1.0 is called the unity-gain frequency or gain crossover frequency. It is generally found that gain margins of three or more combined with phase margins between 30 and 60 degrees result in reasonable trade-offs between bandwidth and stability. As we know that gain margin is the gain when the phase causes -180º but in our boost converter phase never crosses -180º that means the gain margin is infinite (Fig. 5.1). It will be clear if we see root locus of the system(Fig. 5.2) we assume we have our converter at gain K and we are operating at unity feedback it has two poles and no matter how much we increase the gain- the system will never goes unstable. If we increase gain that means we need to move the gain margin curve upward so by doing this we see that phase margin never crosses -180º that means increasing gain will not change the gain margin or will unstable the system.

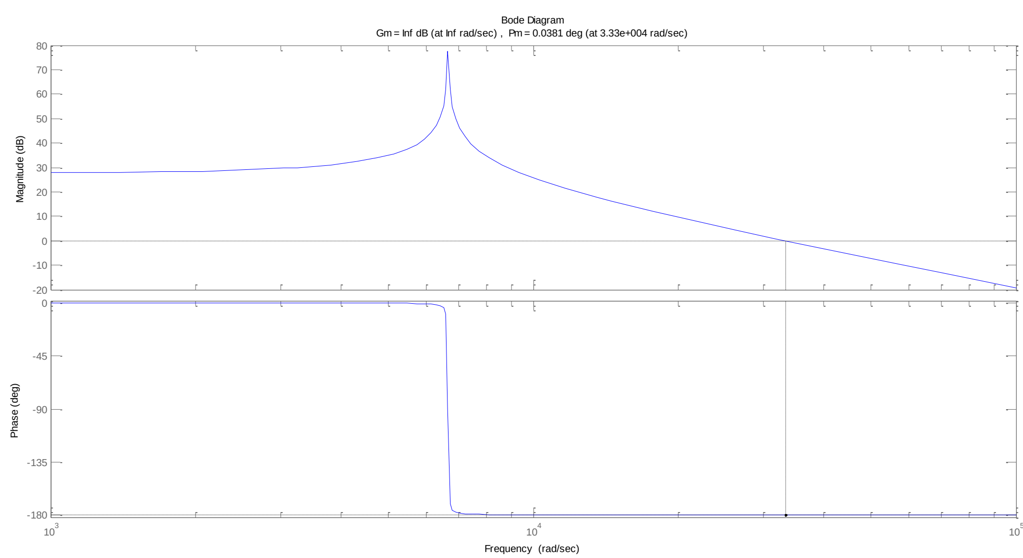


Fig. 5.1: Gain Margin, Phase Margin and Crossover Frequency

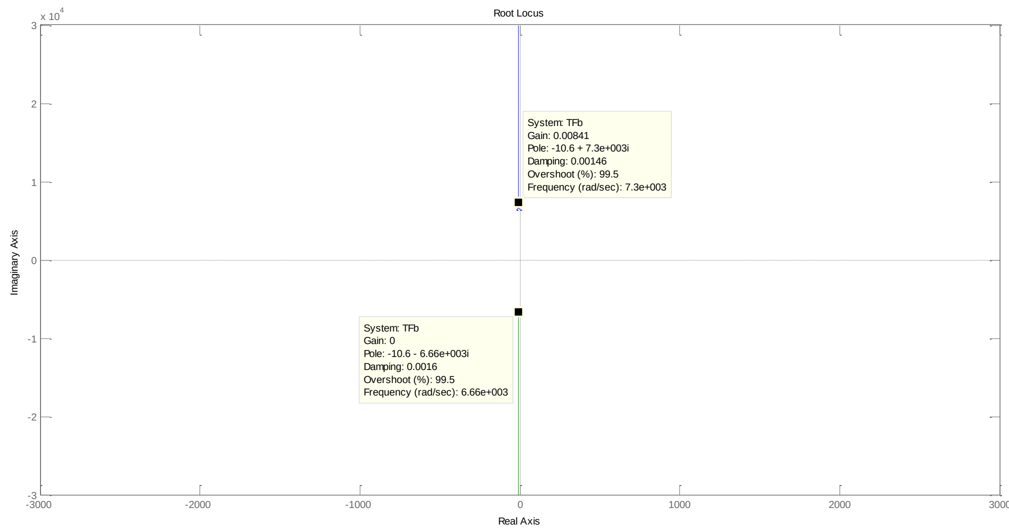


Fig. 5.2: Root Locus

5.3 Single-loop control:

The output voltage is regulated by closing a feedback loop between the output voltage and duty-ratio signal.

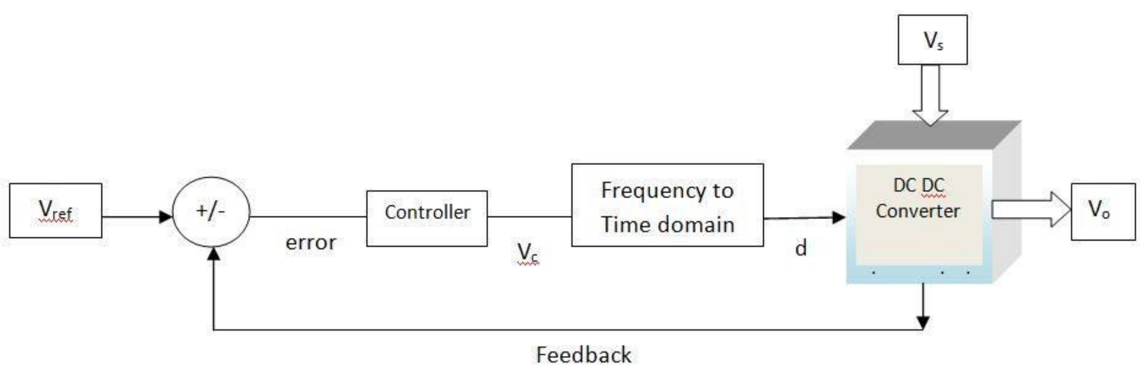


Fig. 5.3: Close loop system

From the figure above we can see that the output voltage is compared with a constant reference signal V_{ref} to the error, which is then passed through the control transfer function G(s) to generate a control signal V and lastly the PWM modulator converts the control signal into the transistor drive waveform. The negative feedback summation and the control transfer function are usually implemented using a single op-amp even as the PWM modulator is formed by a comparator and ramp generator. Fanatical integrated circuits are available for the control of DC-DC converters, they typically comprise a control amplifier, modulator circuitry, a latch for the comparator output to prevent 'switch bounce', and also housekeeping functions such as current limit, shutdown and soft-start. Simple analogue circuit-based control systems such as this are the most appropriate for many DC-DC converter applications due to their low cost and high speed. The controller will have a output voltage V_c and it will go to some circuitry and we want to make error zero. Our error will be zero when the gain K will be $= \frac{V_c}{e}$; e= error. If we want to make error zero either we have to make V_c zero or should be make K infinite. Making Vc zero means making it ground in that case there will be no negative feedback. So, we have to choose the option of making K infinite. So, whatever the value of V_c we have the high value of K will make error as much small as possible. However, infinite or high value of K have some problems such as noise which is beyond control. Noise may be in our circuit, noise may come from neighboring circuit and so on and so forth. Noise is an issue and particularly if the controller gain K as a very high value then noise which is generated in every component in the electronic circuit will also get amplified by this infinite gain and it will swamp out all useful signal. Additionally, another problem is limited input or limits in input. There is a power supply which is given to the signal conditioning circuits of the switch mode converter DC-DC converter is generally plus minus 12 V or plus minus 15 V, 0 to 5 V, 0 to 3.3 V. These put a limit on the input voltage value and as a result, any value cannot be given any value to from the minus infinity to plus infinity an error. If it hangs beyond of particular value it will saturate the input; it will go and struck to either plus or minus voltage limit and once it will get saturated there will be no longer a close loop system. Thus, the system will be open loop and our main objective of closing the loop will not be met, for that reason, these two are very important issues that needs to be addressed for designing a controller.

The controller gain which is inserted in between the error and the plant input needs to be shaped with respect to frequency and there are three important gain shaping components, one is the integrator. The integrator which falls at the rate of 20 dB per decade mean the gain decreases a 20 dB for every decade change in ω frequency and we basically works with the plane gain. The plane gain does not change with frequency. Furthermore, there is derivative component but pure derivative does not exist.

We are trying to design the controller which is consisting of one proportional component, it is a co-proportional gain component, usually called K_p. There is another component- the integrator component and this has a gain $\frac{K_i}{s}$ and in this case s suggest the Laplace pole at s is equal to 0 in the S plane. Moreover, there is derivative component but pure derivative is not possible to represent. So, we have considered the gain, which will be denominated$\frac{K_d \times s}{s+a}$. Currently, this are the three component that we are going to use to design our controller.

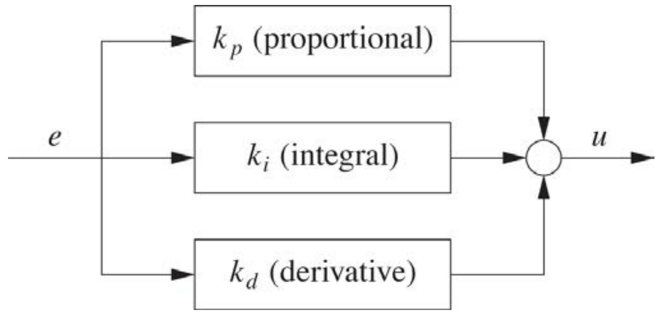


Fig. 5.4: A fundamental model of PID Controller

Now the following components vary with a respect to ω in a certain style. If we plot a graph in which there will be ω along with the x axis and dB gain along the y axis; dB gain = $20\log_{10}\frac{Input}{Output}$. So in this case we will have different dB gain for our different three components.

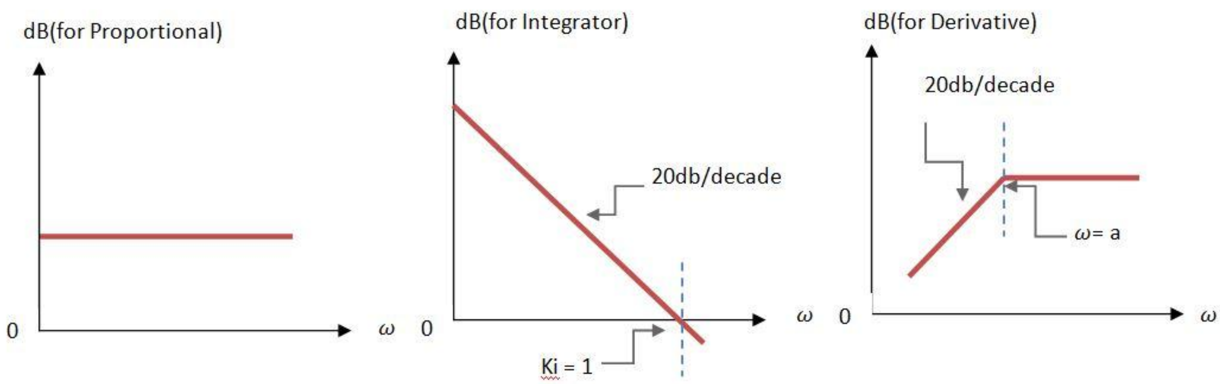


Fig. 5.5: dB gain curves for

From the figure above we can say that there will be no change in gain or dB gain in case of proportional component. For Integrator component there is downward slope and it will decay by -20 dB per decade, the moment it crosses the 0 dB line the gain will be 1 or we can say unity gain will be achieved. Additionally, the derivative component will have an upward slope and it will increase by +20dB per decade but at the moment when ω= a then it turns into a flat. These are the concerns we are concerned about for designing a controller. So from the single loop control analysis we see that the gain is dynamic and it cannot be infinite. We have mentioned before that there are two issues- one is the issue of noise, noise which is present in all electronic circuits, which will also get amplify and amplified and it will swamp the plant input and the second issue is that of limited supply voltage at input or can say duty cycle. At this moment we can sum up that because of these two limitations; we have to face that dynamic gain and the dynamic gain cannot be an constant along with it should vary with frequency.

Most physical systems have natural gain versus frequency and they act like a low pass filter. The gains automatically start reducing and becoming attenuating after a certain values of frequency. The low pass filter characteristics is like it will have lower frequency gains and the lower frequency has a higher gains pass through the plants or converters or systems. As a result, the higher frequency component get attenuated. If it is third order systems, the system will have -60 dB per decade slope. If it is first order system; the system will have -20 dB per decade slope. The complications because of plant frequency will be solved by designing a controller by using PID components.

5.4 Frequency Response of Proportional, Integrator and Derivative Part by MATLAB Simulation:

To make the concept clear we did MATLAB simulation for the major important component of our controller circuit.

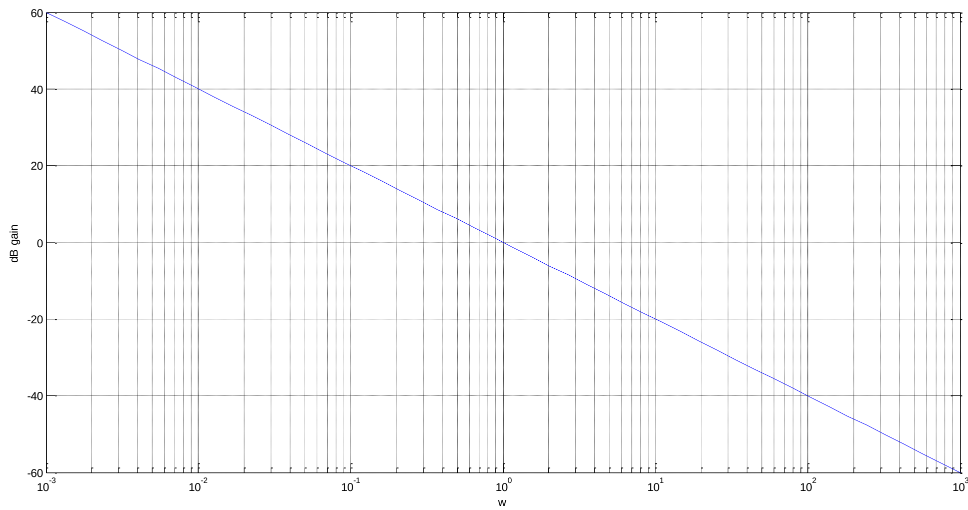


Fig. 5.6: Frequency response of integrator component [assuming, Ki=1]

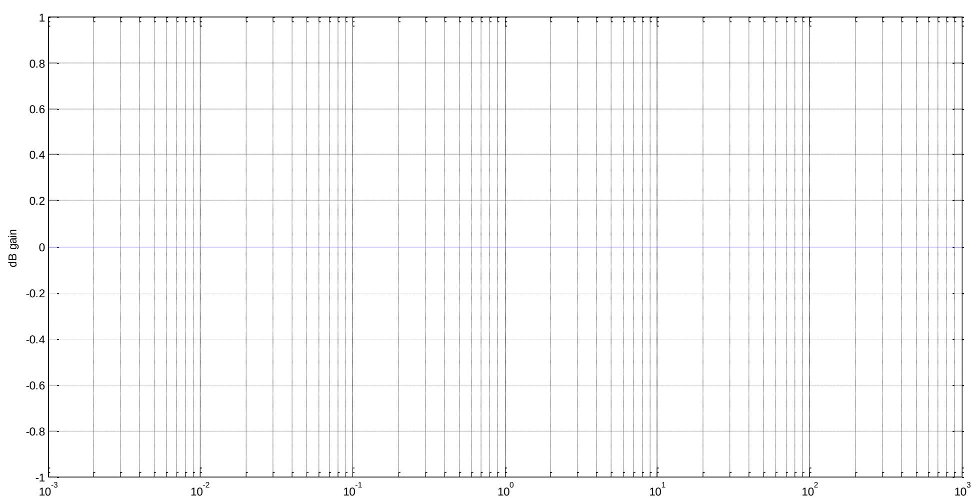


Fig. 5.7: Frequency response of proportional component . [assuming, Kp=100]

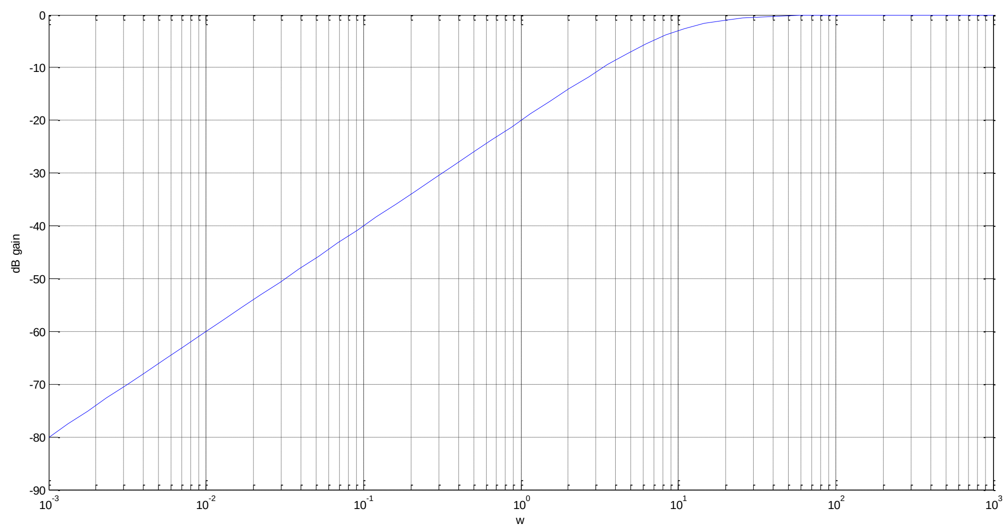


Fig. 5.8: Frequency response of proportional component . [assuming, Kd=1]

5.5 Closed Loop Feedback using Integral component:

We are going to design the controller step by step. In the first step we make our closed loop system by only integrator part so that we can see what portion or what component of our controller should be changed. After using only Ki gain or integration block we find the following graph by doing MATLAB simulation.

We assume the gain or value of K_i=1 and use our transfer function to observe the step response of the system. We surly can see from Fig. 5.9 that it has some problems and the response we get is not in fact satisfactory. It is under damped oscillatory and we are going to improve it by adding something ahead.

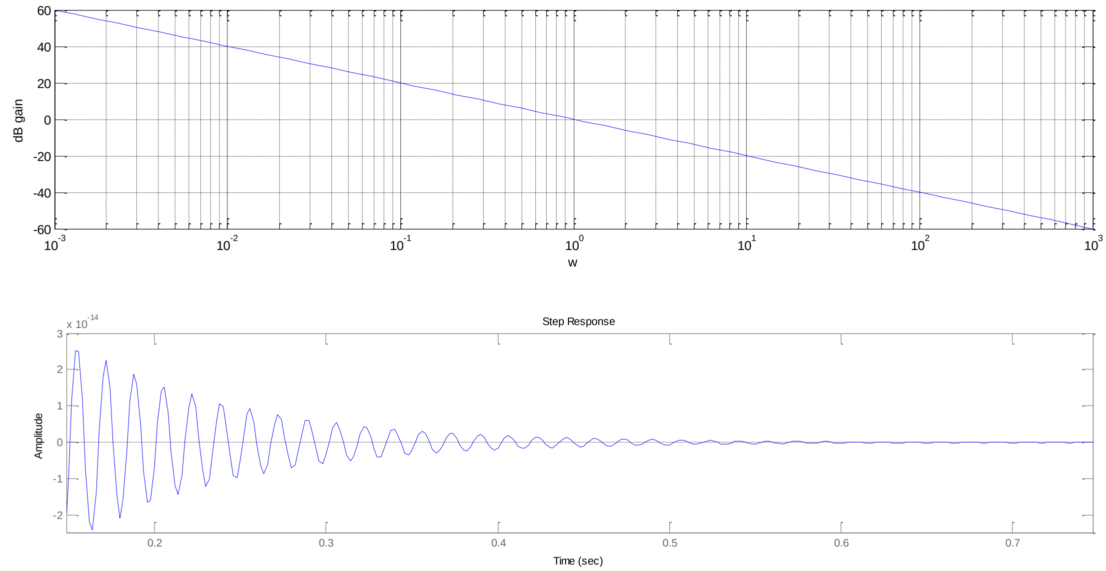


Fig. 5.9: Step Response of the system using Integral Component Only.

Now again we are going to consider transfer function of integrator part and our DC-DC boost converter part to get the closed loop transfer function for getting better result.

Let, G_c= Controller Transfer function= $\frac{K_i}{s}$

G_{bc}= Boost converter transfer function

$G_{SI} = \frac{G_c \times G_{bc}}{1+ G_c G_{bc}}$, here G_{SI} will be the closed system transfer function.

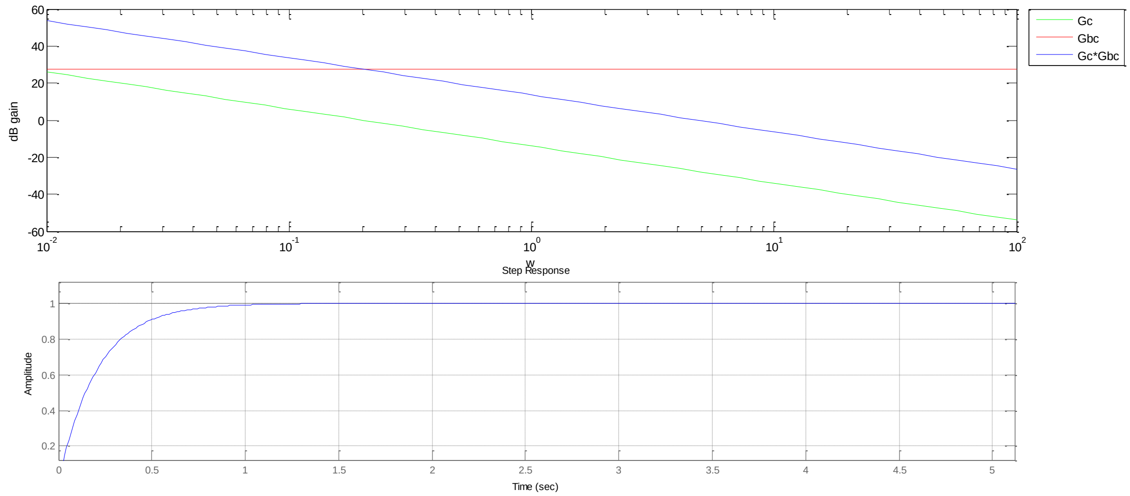


Fig. 5.10: Response of G_c, G_{bc} and G_{SI}

From the Fig. 5.10 we can see that our system response does not change. Furthermore, when we add Gc and Gbc, we see that GSI is pulled up means it increases. At the K_i= 0.2 the system reaches at the steady state point at time 1 second. We observe the time response of the system, so finding proper value of K_i can bring stability to the system. However, we need to reduce the error in the transient and for that reason we are going to introduce the new component and that is the proportional component. So our new transfer function will be $G_c = \frac{K_i}{s} + K_p$. If the integrator portion starts to cross the unity gain point then there will be dropped off and along the K_i gain line by -20dB/decade. But we can change the scenario by adding the proportional part at the point where the gain seems to be dropped off. From the MATLAB simulation we change the values of gain of proportional part.

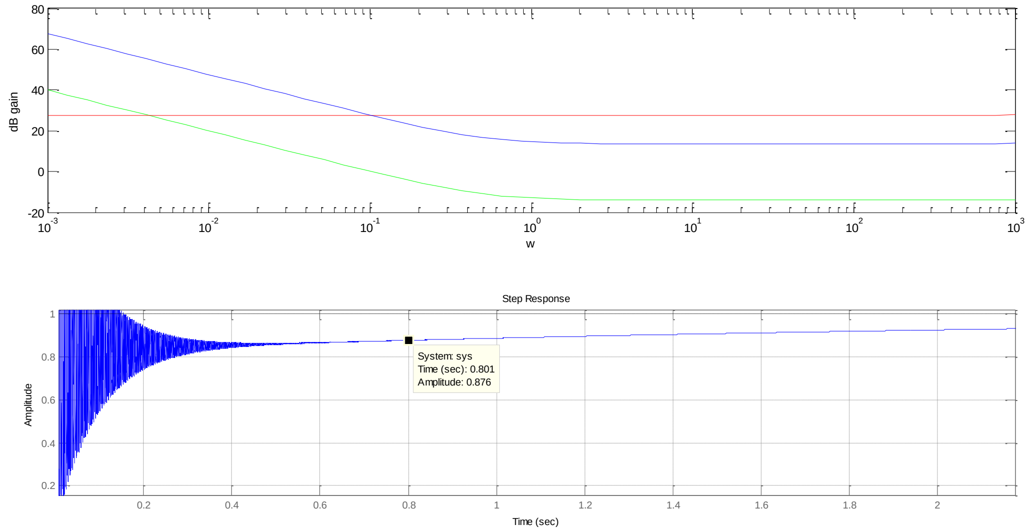


Fig. 5.11: Response of G_c, G_{bc} and G_{SI} [when K_p= 0.1]

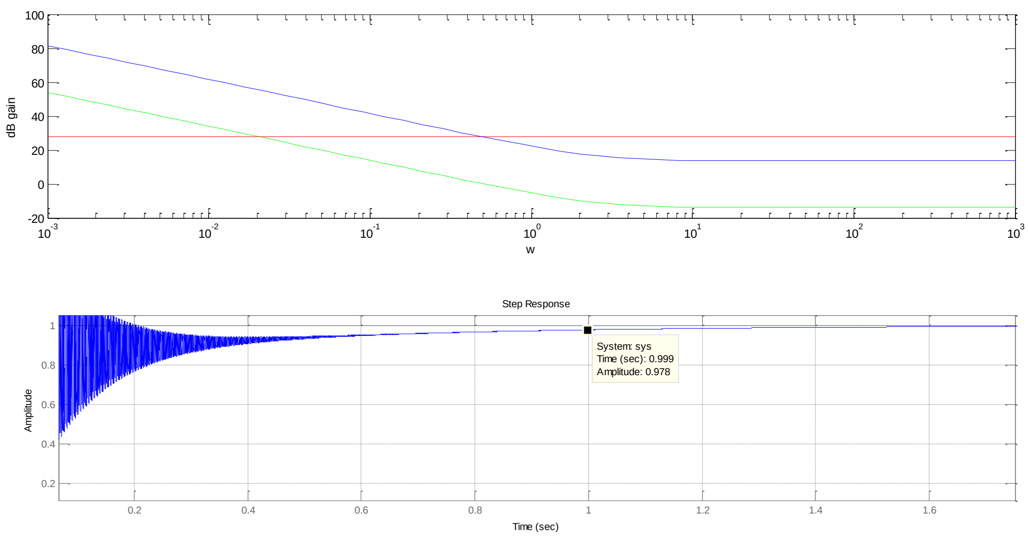


Fig. 5.12: Response of G_c, G_{bc} and G_{SI} [when K_p= 0.5]

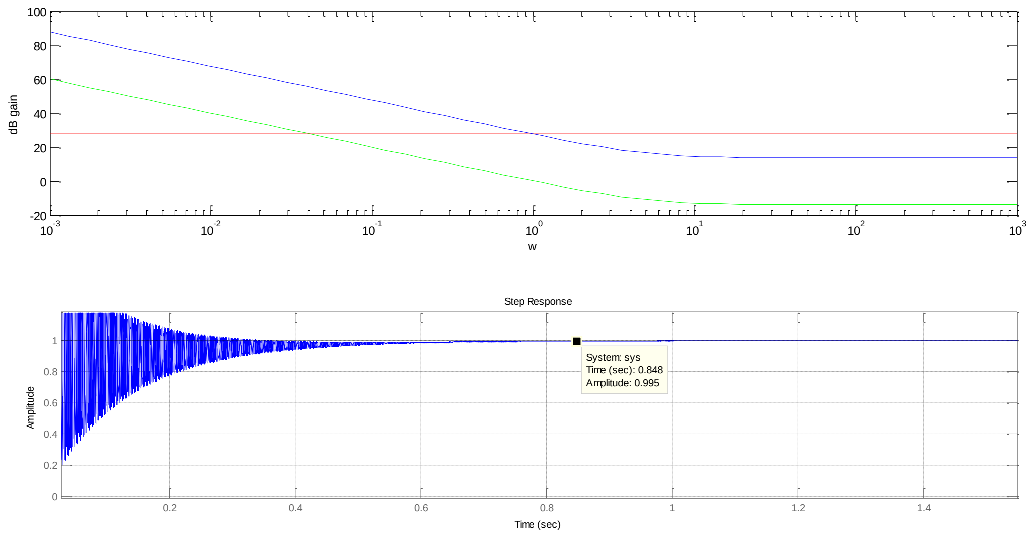


Fig. 5.13: Response of G_c, G_{bc} and G_{SI} [when Kp= 1]

From the above simulation results say that system will have noise when the frequency is low, but by the increasing 0f K_p value the time to enter into steady state will decrease which is actually better for our system. As a result in our controller we will make sure that the value of K_p will be 1 but not so high cause excess high K_p will make the system vulnerable.

Among all three components we have already discuss about the integrator component, then proportional component and now we will see the change or importance of the third component the derivative component which has a 20 dB per decade rise. After particular point and frequency pole get in the picture and then behaves in a way the gain get compressed. Consequently, this is the derivative component and this is achieved by adding this $\frac{K_d S}{s+a}$.

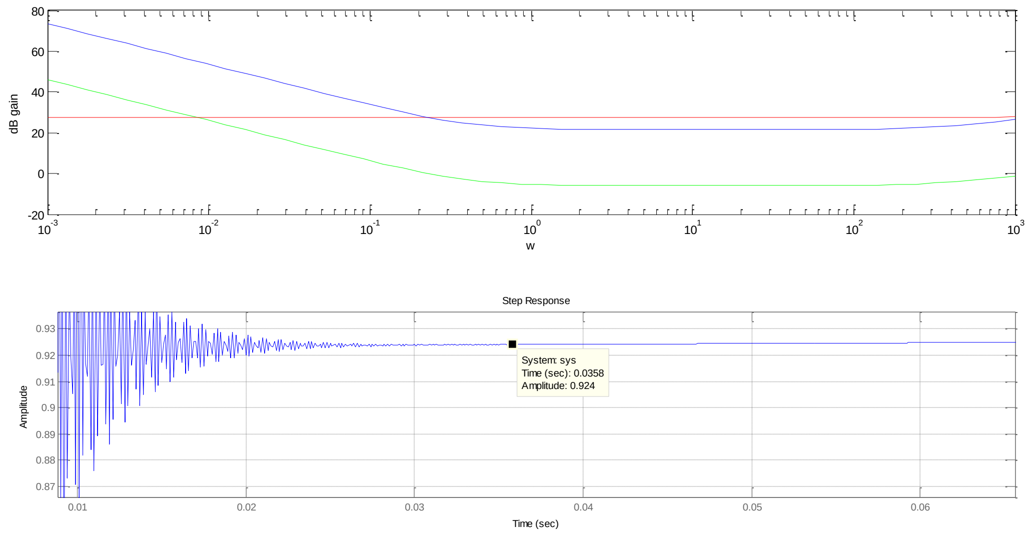


Fig 5.14: Response of G_c, G_{bc} and G_{SI} [when K_d= 0.6]

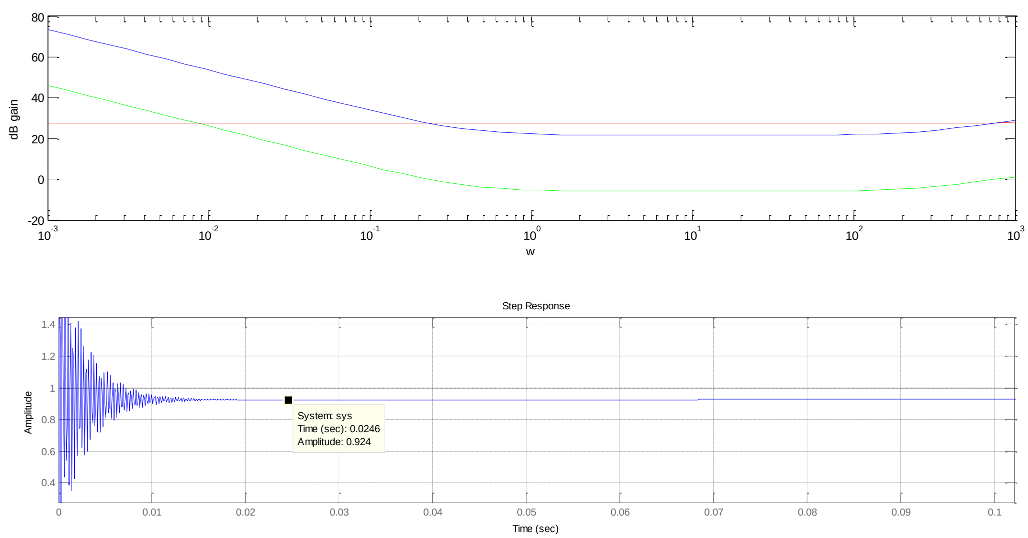


Fig. 5.15: Response of G_c, G_{bc} and G_{SI} [when K_d= 1]

From the simulation we can get that adding derivative part will reduce the noise and the time to enter into the steady state will decrease more quickly than before. When the system starts to move from high to low frequency the derivative portion gives it to the proportional part of the system. However, at particular point of proportional part, gain starts to fall so then it handed over to the integrator part to maintain the gain. So, the derivative part quickly pulls it up because the gain in gain is much higher than the proportional part. The gain compared to the proportional part is so much more in the case of the derivative. Therefore, the action would be very fast but we should be kept in sense that all these high frequency segments are noise sensitive which may cause amplified gain due to the gain, so we have to choose the values of K_d and K_p carefully.

5.6 Windup Problem:

Integral windup, also known as integrator windup refers to the situation in a PID feedback controller where a large change in set point occurs and the integral terms accumulates a significant error during the rise (windup), thus overshooting and continuing to increase as this accumulated error is unwound (offset by errors in the other direction). The specific problem is the excess overshooting **[3]**. From the Figure below we can be clear about Windup problem.

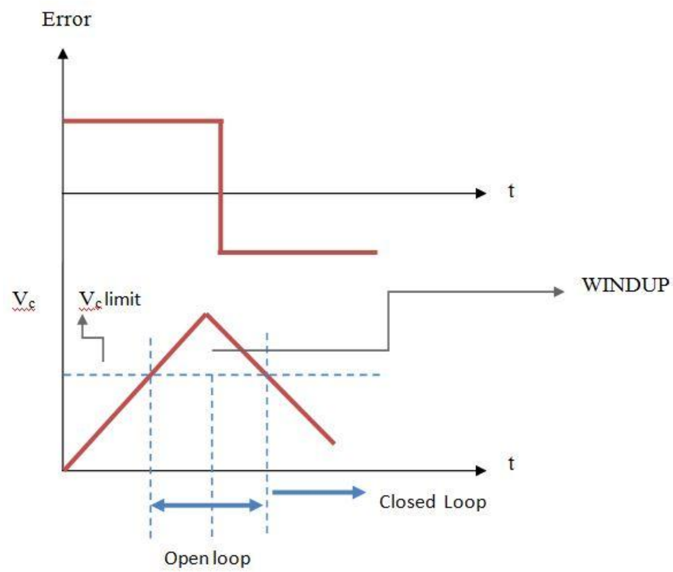


Fig 5.16: Integral Windup

As we cannot give infinite input so that when V_c is more than V_{climit} after a certain point it will be clamped and the error change with respect to time when at particular point V_c increases and the error becomes negative. While the error switches to negative the Vc started to decrease and when it starts to enter to below the V_{climt} that is the place the close loop operation start to operate. Open loop stays for a significant amount of time and it causes delay in giving feedback as the closed loop system starts later. This is the windup problem which happens due to integral portion of the controller. How can that be solved, will be presenting on the following chapter.

Chapter 6

Implementation of PID Controller

6.1 Introduction:

We can simply our controllers' gain blocks by using op amps. Making the circuit less complicated we need to choose proper value. This chapter is going to show how it will happen.

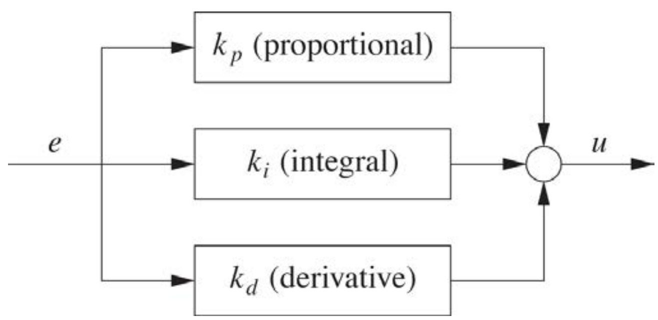


Fig 6.1: Blocks of K_i, K_p, K_d

6.2 Implementation of PID blocks by op amps:

As in our thesis we need to control V of the converter so we can replace the blocks with op amp. Firstly, we can change the comparator portion with a differential op amp. The positive portion will be connected to V_o and negative portion will be connected to V_{oref}. The output will be-

$$\text{Error, e} = V_{oref} - V_o$$

Then, we need to replace integrator portion with op amp (additional gain and inversion). For making the circuit less complicated we can choose proper value of R_i and C_i so that we can reduce the number of op amp. Again the output of integrator will be -

$$V_{oi} = \frac{1}{R_i \times C_i} \int e \, dt$$

And then, we need to replace K_p or proportional portion with a single op amp (inverting amplifier). So, input of the op amp will be Error and output will be-

$$V_{op} = -\left[\frac{R_f}{R_p}\right] \times e$$

For summing up we can use one more op amp- summing op amp and we choose to connect summing resistances which have same values of resistances and have to connect them with integrator output and proportional output.

$$V_c = -\left[V_o \times \frac{R_i}{R_{si}} + V_{op} \times \frac{R}{R_{op}}\right]$$

We put minus sign because of inversion. After implementing op amps in PID block the control voltage V_c goes to PWM block and then converted into time and then goes as input to the DC- DC converter. PI controller is not complete if we do not add Anti-Windup. The value of V_c goes beyond a particular threshold. In that case we do not want integrator to integrate. We want to stop the capacitance from accruing any further charge consequently we just need to clamp it. We do clamp by using two zener diodes back to back- one in positive and one in negative direction respectively and those will used as Anti-Windup clamp.

Our plant or DC-DC converter has low pass filter characteristics; controller try to pull up by integration and proportional part want to preserve the pull up part. Differential portion tries to pull up the gain at much higher frequency. The differential portion of the controller does not make significant change rather than it makes the system slower. Therefore we do not need to use differential part.

$$V_c = V_{oi} + V_{op}$$

$$= \frac{1}{R_i \times C_i} \int e\, dt + [-\left[\frac{R_f}{R_p}\right] \times e]$$

$$\frac{1}{R_i \times C_i} \int e\, dt = \frac{K_i}{s}$$

So, our transfer function will be-

$$\frac{V_{c(s)}}{E_{(s)}} = \frac{K_i}{s} + \frac{R_f}{R_p}$$

But we can eliminate the op amps by using simpler op amp like the following figure.

In that case the transfer function will be-

$$\frac{V_{c(s)}}{E_{(s)}} = \frac{R_1}{R_2} + \left[-\left(\frac{R_1}{R_2}\right) \times \frac{1}{s}\right]$$

$$\frac{V_{c(s)}}{E_{(s)}} = \frac{R_1 + \frac{1}{sC_1}}{R_2} = \left(\frac{R_1}{R_2}\right) + \left(\frac{\frac{1}{sC_1}}{R_2}\right)$$

Where, $\frac{R_1}{R_2} = K_p$ and $\frac{R_2 C_1}{s} = \frac{K_i}{s}$

We can give inversion on PWM portion or on comparator portion. When we inter change V_{oref} and V_o attach with feedback. Then we get inversion error, e = $V_{oref} - V_o$ and this inversion is followed by inversion in PID controller and reach at V_c without inversion. We track the inversion for observing line tuning. However, we can combine two op amps; one is differential amplifier and another one is inverting amplifier with impedance gain. We will convert resistance and capacitor with impedance. If we look at R and R_1 and C_1, if we look at resistances are connected with V_{oref} and convert them into impedances, then they become difference amplifier and additionally they can also do integration. But we replace the mentioned, it will affect K_i and it will affect the K_p also. Hence, it is preferred to use two op amps.

All the signal we get here have two parts-

$$V_{oref} = V_{oref} + 0$$

$$d = D + \hat{d}$$

$$v_c = V_c + \widehat{v_c}$$

We need to add a summer between PID and PWM $\widehat{v_c}$ will come from PID and we will get,

$$error = V_{oref} + 0 - (V_o + \widehat{v_o}) = V_{oref} - V_o + (0 - \widehat{v_o})$$

In the steady state $V_{oref} - V_o$ will be zero. As we are using PID controller, we would focus on deviation. Stady State portion can be given directly through a special circuitry connection which will provide V_{oref} and put it into the summer or it will connect the input directly. If the controller only take care of small signal part, the response will be much faster. But our controller can take care of both steady state and small signal part, if we want to. We can use PWM block which will control our duty cycle and put its value on MOFET's gate to attain noise free step response.

From the previous part of this chapter we can observe that we can make our controller or IC of controller by using op amp. But it will be very effective if we simulate the circuit first and see how actually values change and we can examine that is it really possible to get the value or the closer value as we have wanted?

6.3 SIMULINK Simulation of PID Controller:

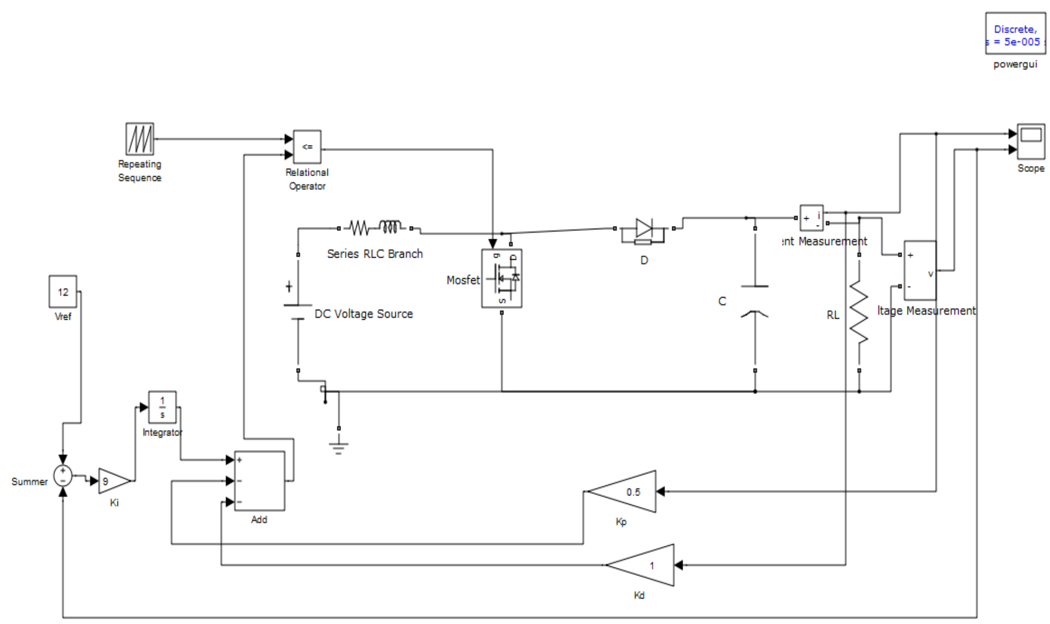


Fig. 6.2: Demo Model of Boost Converter with PID Controller

The specifications of the boost converter are listed as follows:

Input voltage, V_{in} = 6V

Nominal output voltage, V_{out} = 12 V

Reference Voltage, V_{ref}= 12V

Input current, I= 0.012 A

Inductance, L = 120uH

Capacitance, C = 47uF

Duty ratio, D = 0.5

Load resistance, R_L = 10K Ω

R_{esr} = 1m Ω

6.3.1 Parameter and Values for PID Controller:

K_p= 0.5

K_d= 1

K_i=9

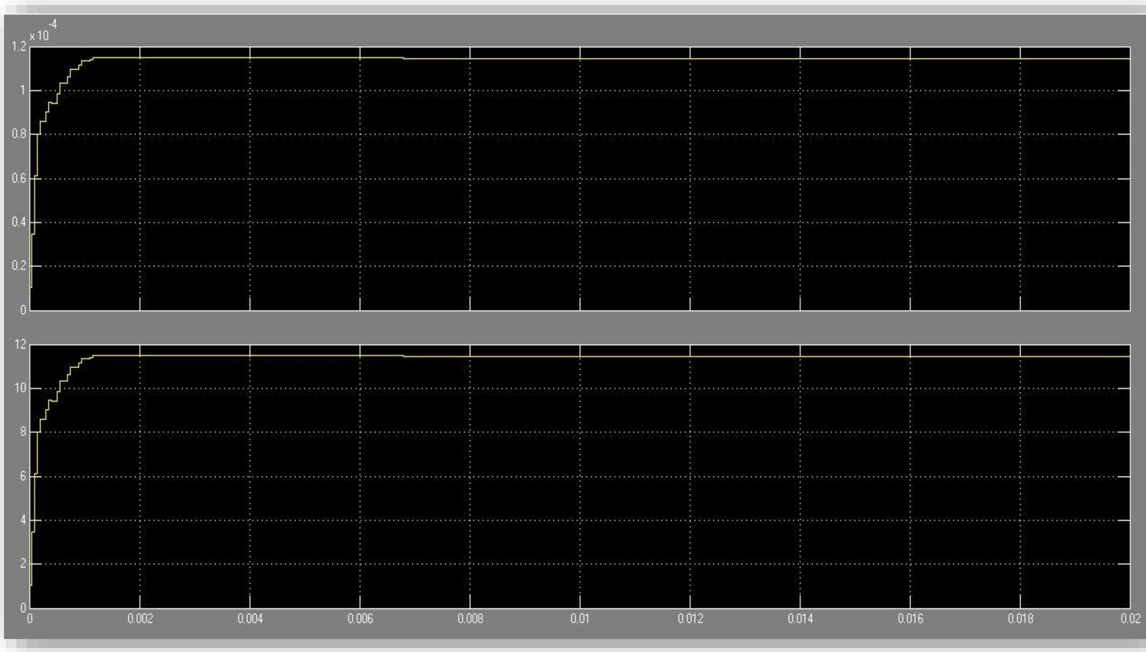


Fig. 6.3: SIMULINK simulation

From the above Fig. 6.2 we can say that we set reference voltage 12 V as we all know we give input of 6V and want the double voltage as output. .From Fig. 6.3 we see that we get almost exact desired value from SIMULINK simulation.

6.4 Practical Work:

We implement the hardware model to observe the relationship between change in input current and output voltage with the change of duty cycle. We take values of different components and face some problems while setting the model due to power rating of the components.

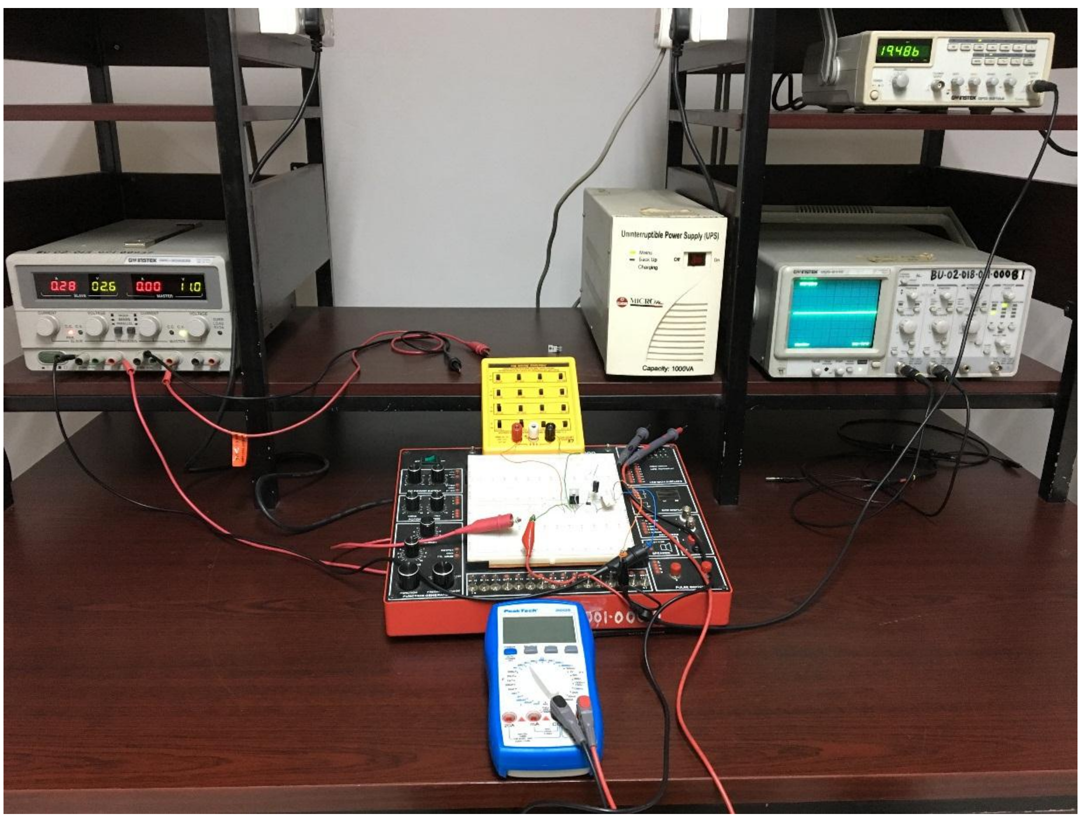


Fig. 6.4: Overall Circuit Setup

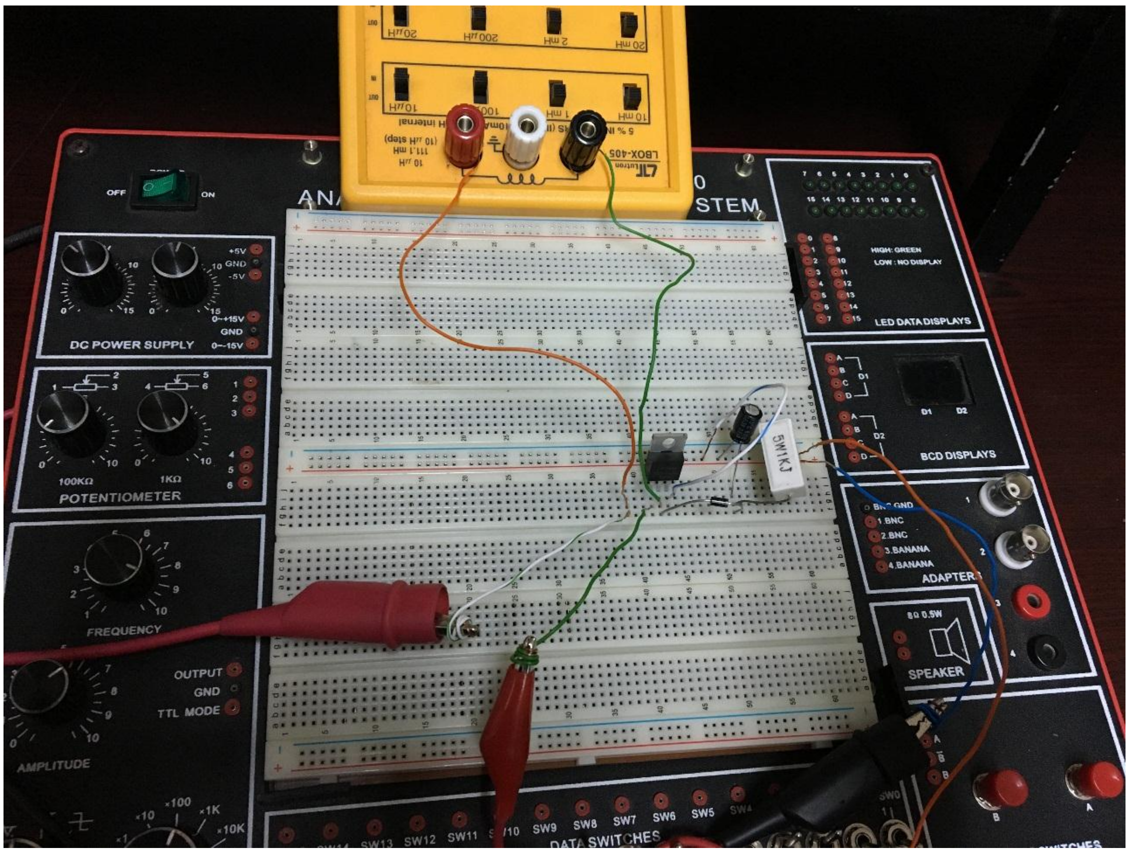


Fig. 6.5: Close view of the circuit setup

We use Vs= 6 V as input voltage, Resistance = 1 kΩ, Inductor = 120µH and frequency = 20 kHz.

V_{in} V	D (Duty cycle)	V_{out} (Theoretical) V	V_{out} (Experimental) V	I_L (Theoretical) A		I_L (Experimental) A
				I_{max}	I_{min}	
6	0.1	6.67	-	0.1324	-0.1176	-
	0.2	7.5	16.5	0.2593	-0.2406	0.06
	0.3	8.57	-	0.3872	-0.3628	-
	0.4	10	29.2	0.5167	-0.4833	0.20
	0.5	12	-	0.6490	-0.6010	-
	0.6	15	36.7	0.7875	-0.7125	0.43
	0.7	20	-	0.9417	-0.8083	-
	0.8	30	46.2	1.15	-0.8500	0.66
	0.9	60	-	1.725	-0.5250	-

Table 1: Theoretical and Experimental results of V_{out} and I_L

In conclusion, in this chapter we have showed that we can make our controller with op amps for making it less complicated and we have presented the simulation of our controller in SIMULINK for being sure of the values of gain as we required. Later, we have mentioned our practical work on DC-DC boost converter to make sure that it will give us expected values as theoretical calculations.

Chapter 7

7.1 Conclusion:

From the above discussion we can state that we have showed the problems of harmonics in rectifier circuits and for solving that we introduce boost converter and we use it because of convenient switching position and less input size. We have stated controller to get noise and distortion less output. We have showed op amps circuits in theories for making less complicated gain blocks. We have done simulations in PSPICE, MATLAB and SIMULINK for showing the values and experiment results.

7.2 Future Research:

We have done our thesis on DC-DC boost converter and design controller and show its simulation. We have done this taking the load side but it can be done as feed forward or we can say from the input side. Additionally, we have taken single input, it can be done by taking multiple input and so on. We can add micro controller application if we would have studied more on this topic.

References

[1] Hart, D. W. (2011). Power Electronics

[2] Hart, D. W. (2011). Power Electronics

[3] Bucella, T. (1997). Servo control of a DC-brush motor. Application Note AN532, Microchip Technology Inc.

Appendix:

MATLAB CODES FOR CONVERTER SIMULATION:

```
%---Model for DC-DC boost converter
disp(['the values of the plant parameters']);
Vg= 12; %V
D= 0.6; %duty ratio
L=120e-6; %H
C=50e-6; %F
R=1e-3; %ohm
%STAEDY STATE MODEL OF BOOST CONVERTER
As=[0 -(1-D)/L ; (1-D)/C -1/R*C];
Bs=[1/L 0 ; 0 1/C];
Cs=[0 1 ; 1 0];
Ds=[0 0 0 ; 0 0 0];
Vo= -Cs(1,:)*((As)\Bs(:,1))*Vg;
Ig= -Cs(2,:)*((As)*Bs(:,1))*Vg;
%SMALL SIGNAL MODEL OF THE BOOST CONVERTER
a= [0 -(1-D)/L ; (1-D)/C -1/R/C];
b= [1/L  0 Vo/L ; 0 -1/C -Ig/C];
c=[0 1];
d=[0 0 0];
TFb= zpk(tf(ss(a,b(:,3),c,[0])))
bode(TFb);
margin(TFb);
[gm,pm,wp,wg]=margin(TFb);
```

MATLAB CODE FOR CONTROLLER:

```
ki=9;
kp=0.5;
kd=1;
a=800;
nc=[(kp+kd) (ki+kp*a) (ki*a)];
dc=[1 a 0];
w=logspace(-3,3);
gc=freqs(nc,dc,w);
subplot(2,1,1),semilogx(w,20*log10(abs(gc)));hold;pause;
%PLANT
np= [1063829787.2341];
dp= [1 21.28 4.433E007]
gp=freqs(np,dp,w);
subplot(2,1,1),semilogx(w,20*log10(abs(gp)),'r');pause;
%PLANT+CONTROLLER
gpc=freqs(conv(nc,np),conv(dc,dp),w);
subplot(2,1,1),semilogx(w,20*log10(abs(gpc)), 'b');hold;pause;
%STEP RESPONSE OF CLOSED LOOP SYSTEM
[ns,ds]=feedback(conv(nc,dc),conv(np,dp),[1],[1]);
subplot(2,1,2),step(ns,ds,50);
```

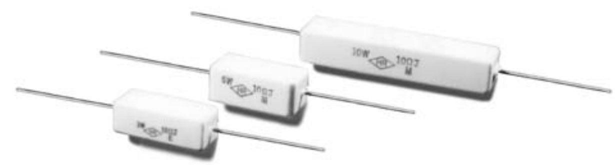
Cement Power Resistors (RoHS Compliant) PW-RC Series

FEATURES

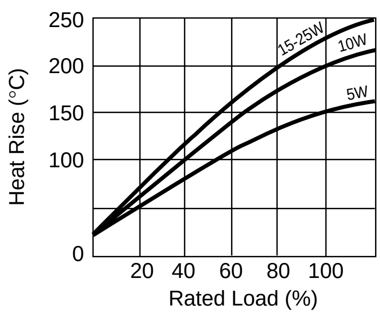
- Temperature Range: -55°C ~ +155°C
- 5% tolerance
- Exceptionally small, sturdy, and reliable
- Sealed with a special cement
- Excellent moisture resistance
- High temperature stability
- Ceramic flame retardant package
- Recommended wash method is alcohol

LEAD-FREE

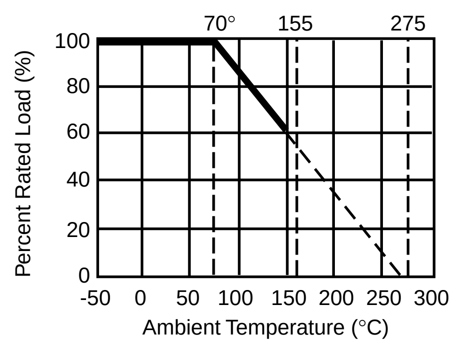
Environmental Commitment



HEAT RISE CHART



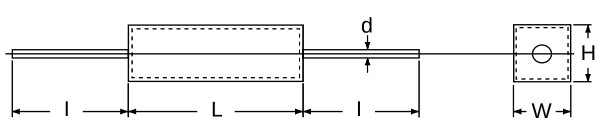
DERATING CURVE



PART NUMBERING SYSTEM

C	R		5	-	1	0	K	-	R	C
Series			Watts		Value				Suffix (RoHS Compliant)	

POWER RATING, RANGE OF VALUES, AND DIMENSIONS



Watts (W)	Range of Values		Dimensions (mm)				
	Wire Wound	Metal Oxide	L ±1	W ±1	H ±1	l ±5	d ±0.05
5	0.1 ~ 47	48 ~ 25K	22	10	9	35	0.75
10	0.1 ~ 910	911 ~ 25K	49	10	9	35	0.75
15	1 ~ 1K	- - N/A - -	49	12.5	11.5	35	0.75
25	2 ~ 1.0K	- - N/A - -	64	14.5	13.5	35	0.75

STANDARD STOCKED VALUES (Ω)

0.1	0.33	0.56	1.0	1.8	3.3	4.7	6.8	11	18	27	43	62	100	160	250	390	560	910	1.5K	2.4K	4.7K
0.15	0.39	0.62	1.1	2.0	3.6	5.0	7.5	12	20	30	47	68	110	180	270	430	620	1.0K	1.6K	2.7K	5.0K
0.2	0.43	0.68	1.2	2.2	3.9	5.1	8.2	13	22	33	50	75	120	200	300	470	680	1.1K	1.8K	3.0K	10K
0.22	0.47	0.75	1.3	2.4	4.0	5.6	9.1	15	24	36	51	82	130	220	330	500	750	1.2K	2.0K	3.3K	20K
0.27	0.5	0.82	1.5	2.7	4.3	6.2	10	16	25	39	56	91	150	240	360	510	820	1.3K	2.2K	3.9K	25K
0.3	0.51	0.91	1.6	3.0																	

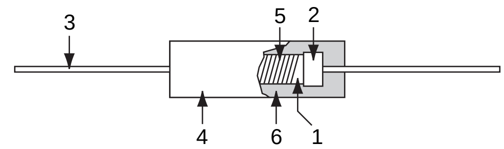
*Other values available by special request

XICON

Cement Power Resistors (RoHS Compliant) PW-RC Series

CONSTRUCTION

No.	Subpart Name	Material	Material Generic Name
1	Body	Rod Type Ceramics	Al_2O_3, SiO_2
2	End Cap	Tin plated iron surface	Tin : 5%, Iron : 95%
3	Lead	Annealed copper wire (Electrosolder plated surface) Pb Free	Tin-Coated Copper wire
4	Ceramic Case	Ceramic	Al_2O_3, SiO_2
5	Resistance wire	Ni-Cr Alloy	Ni-Cr Alloy
6	Filling Materials	Quartz mixed sand	SiO_2



Cement: Wire wound

CHARACTERISTICS

<table>
<tr><th>Characteristics</th><th colspan="2">Limits</th><th colspan="3">Test Methods (JIS C 5201-1)</th></tr>
<tr><td>Temperature coefficient</td><td colspan="2">± 350 PPM / °C Max.
<20Ω ± 400 PPM / °C</td><td colspan="3">5.2 Natural resistance change per temp. degree centigrade.
$\frac{R_2-R_1}{R_1(t_2-t_1)} \times 10^6$ (PPM / °C)
R_1: Resistance value at room temperature (t_1)
R_2: Resistance value at room temp. plus 100 °C (t_2)</td></tr>
<tr><td>Dielectric withstanding voltage</td><td colspan="2">No evidence of flashover, mechanical damage, arcing or insulation break down</td><td colspan="3">5.7 Resistors shall be clamped in the trough of a 90° metallic V-block and shall be tested at AC potential respectively for 60 +10/ -0 secs.</td></tr>
<tr><td rowspan="6">Temperature cycling</td><td colspan="2" rowspan="6">Resistance change rate is ± (2% + 0.05Ω) Max. with no evidence of mechanical damage</td><td colspan="3">7.4 Resistance change after continuous 5 cycles for duty shown below:</td></tr>
<tr><td>Step</td><td>Temperature</td><td>Time</td></tr>
<tr><td>1</td><td>-55 °C ± 3 °C</td><td>30 mins</td></tr>
<tr><td>2</td><td>Room temp.</td><td>10 ~ 15 mins</td></tr>
<tr><td>3</td><td>+155 °C ± 2 °C</td><td>30 mins</td></tr>
<tr><td>4</td><td>Room temp.</td><td>10 ~ 15 mins</td></tr>
<tr><td>Short time overload</td><td colspan="2">Resistance change rate is ± (5% + 0.05Ω) Max. with no evidence of mechanical damage</td><td colspan="3">5.5 Permanent resistance change after the application of a potential of 2.5 times RCWV for 5 seconds</td></tr>
<tr><td rowspan="2">Load life in humidity</td><td>Resistance value</td><td>Δ R/R</td><td colspan="3" rowspan="2">7.9 Resistance change after 1,000 hours operating at RCWV with duty cycle of (1.5 hours "on", 0.5 hour "off") in a humidity test chamber controlled at 40 °C ± 2 °C and 90 to 95 % relative humidity</td></tr>
<tr><td>Wire-wound</td><td>± 5%</td></tr>
<tr><td rowspan="2">Load life</td><td>Resistance value</td><td>Δ R/R</td><td colspan="3" rowspan="2">7.10 Permanent resistance change after 1,000 hours operating at RCWV with duty cycle of (1.5 hours “on”, 0.5 hour “off”) at 70 °C ±2 °C</td></tr>
<tr><td>Wire-wound</td><td>± 5%</td></tr>
<tr><td>Terminal strength</td><td colspan="2">No evidence of mechanical damage</td><td colspan="3">6.1 Direct load :
Resistance to a 2.5 kgs direct load for 10 secs. in the direction of the longitudinal axis of the terminal leads
Twist test :
Terminal leads shall be bent through 90 ° at a point of about 6mm from the body of the resistor and shall be rotated through 360° about the original axis of the bent terminal in alternating direction for a total of 3 rotations</td></tr>
<tr><td>Resistance to soldering heat</td><td colspan="2">Resistance change rate is ± (1% + 0.05ø) Max. with no evidence of mechanical damage</td><td colspan="3">6.4 Permanent resistance change when leads immersed to 3.2 to 4.8 mm from the body in 350 °C ± 10 °C solder for 3 ± 0.5 secs.</td></tr>
<tr><td>Solderability</td><td colspan="2">95 % coverage Min.</td><td colspan="3">6.5 The area covered with a new , smooth clean , shiny and continuous surface free from concentrated pinholes.
Test temp. of solder : 245 °C ± 3 °C
Dwell time in solder : 2 ~ 3 seconds</td></tr>
</table>

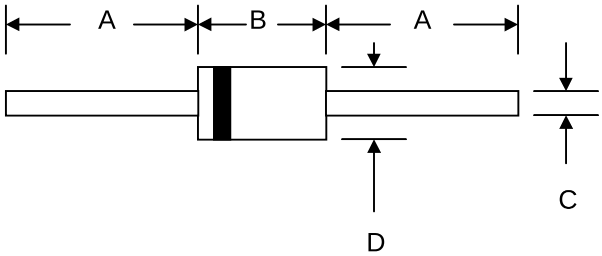
1N4001 – 1N4007

1.0A SILICON RECTIFIER

WTE
POWER SEMICONDUCTORS

Features

- Diffused Junction
- Low Forward Voltage Drop
- High Current Capability
- High Reliability
- High Surge Current Capability



DO-41		
Dim	**Min**	**Max**
A	25.4	—
B	4.06	5.21
C	0.71	0.864
D	2.00	2.72
All Dimensions in mm		

Mechanical Data

- Case: Molded Plastic
- Terminals: Plated Leads Solderable per MIL-STD-202, Method 208
- Polarity: Cathode Band
- Weight: 0.35 grams (approx.)
- Mounting Position: Any
- Marking: Type Number

Maximum Ratings and Electrical Characteristics @T_A=25°C unless otherwise specified

Single Phase, half wave, 60Hz, resistive or inductive load.
For capacitive load, derate current by 20%.

Characteristic	Symbol	1N 4001	1N 4002	1N 4003	1N 4004	1N 4005	1N 4006	1N 4007	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	800	1000	V
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	560	700	V
Average Rectified Output Current (Note 1) @T_A = 75°C	I_O	1.0							A
Non-Repetitive Peak Forward Surge Current 8.3ms Single half sine-wave superimposed on rated load (JEDEC Method)	I_{FSM}	30							A
Forward Voltage @I_F = 1.0A	V_{FM}	1.0							V
Peak Reverse Current @T_A = 25°C At Rated DC Blocking Voltage @T_A = 100°C	I_{RM}	5.0 50							µA
Typical Junction Capacitance (Note 2)	C_j	15							pF
Typical Thermal Resistance Junction to Ambient (Note 1)	$R_{\theta JA}$	50							K/W
Operating Temperature Range	T_j	-65 to +125							°C
Storage Temperature Range	T_{STG}	-65 to +150							°C

***Glass passivated forms are available upon request**

Note: 1. Leads maintained at ambient temperature at a distance of 9.5mm from the case
2. Measured at 1.0 MHz and Applied Reverse Voltage of 4.0V D.C.

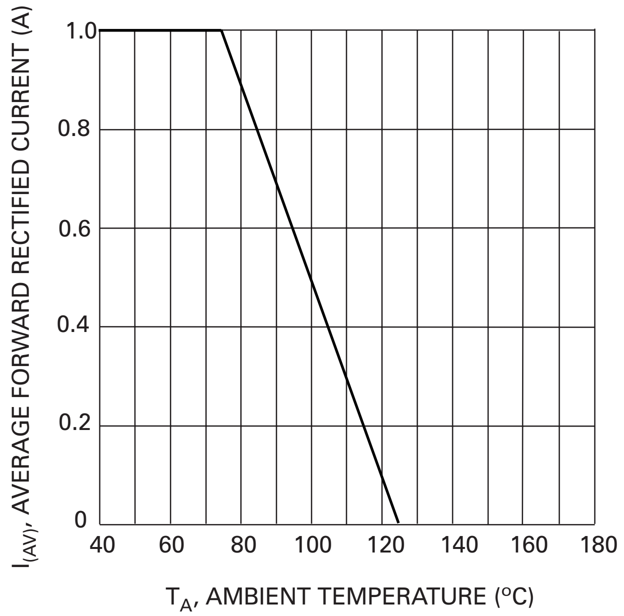


Fig. 1 Forward Current Derating Curve

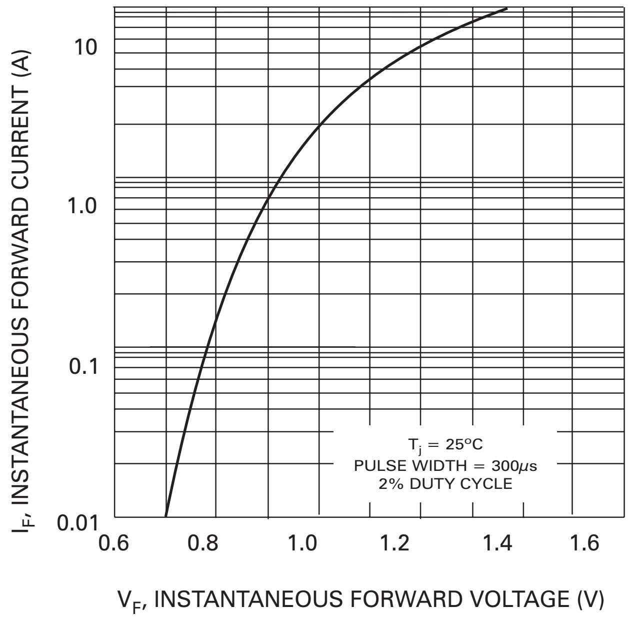


Fig. 2 Typical Forward Characteristics

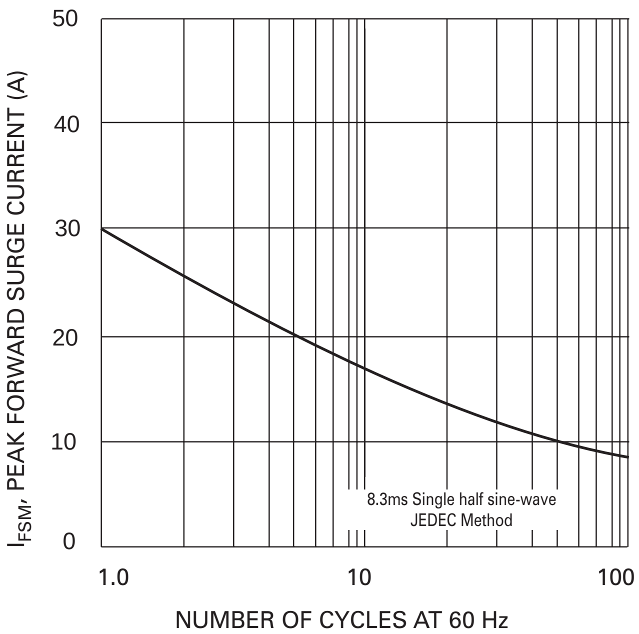


Fig. 3 Max Non-Repetitive Peak Fwd Surge Current

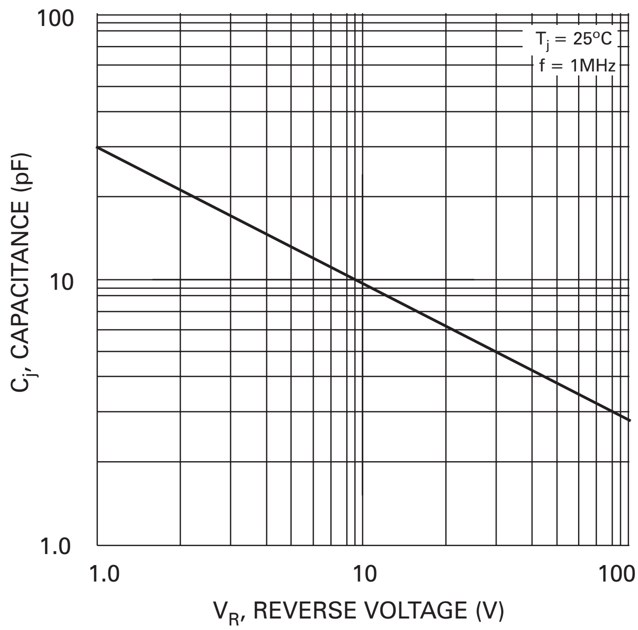


Fig. 4 Typical Junction Capacitance

ORDERING INFORMATION

Product No.◆	Package Type	Shipping Quantity
1N4001-T3	DO-41	5000/Tape & Reel
1N4001-TB	DO-41	5000/Tape & Box
1N4001	DO-41	1000 Units/Box
1N4002-T3	DO-41	5000/Tape & Reel
1N4002-TB	DO-41	5000/Tape & Box
1N4002	DO-41	1000 Units/Box
1N4003-T3	DO-41	5000/Tape & Reel
1N4003-TB	DO-41	5000/Tape & Box
1N4003	DO-41	1000 Units/Box
1N4004-T3	DO-41	5000/Tape & Reel
1N4004-TB	DO-41	5000/Tape & Box
1N4004	DO-41	1000 Units/Box
1N4005-T3	DO-41	5000/Tape & Reel
1N4005-TB	DO-41	5000/Tape & Box
1N4005	DO-41	1000 Units/Box
1N4006-T3	DO-41	5000/Tape & Reel
1N4006-TB	DO-41	5000/Tape & Box
1N4006	DO-41	1000 Units/Box
1N4007-T3	DO-41	5000/Tape & Reel
1N4007-TB	DO-41	5000/Tape & Box
1N4007	DO-41	1000 Units/Box

Products listed in **bold** are WTE **Preferred** devices.
◆T3 suffix refers to a 13" reel. TB suffix refers to Ammo Pack.
Shipping quantity given is for minimum packing quantity only. For minimum order quantity, please consult the Sales Department.

Won-Top Electronics Co., Ltd.
No. 44 Yu Kang North 3rd Road, Chine Chen Dist., Kaohsiung, Taiwan
Phone: 886-7-822-5408 or 886-7-822-5410
Fax: 886-7-822-5417
Email: sales@wontop.com
Internet: http://www.wontop.com

We power your everyday.

INDUCTANCE DECADE BOX

Model : LBOX-405 *ISO-9001, CE, IEC1010*

FEATURES

* Applications :

  General applications
  Troubleshooting, maintenance
  Education and Vocational training
  Production line testing
  Radio and TV services
  Working standards
  Research design & develop
  Physics laboratory work

* Pocket size, offering accurate, reliable performance.
* 10 uH to 111.1 mH, wide range and high resolution (10 uH per step), practical and versatile tools.
* With four decades of inductance.
* Slide switches that allow the user to simply add or subtract for desired value.
* Terminals with multi way binding posts, one to switch shield case.
* ABS plastic housing case, rugged components.

INDUCTANCE DECADE BOX
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* Pocket size, offering accurate, reliable performance.	* ABS plastic housing case, rugged components.

SPECIFICATIONS	
Range	10 uH to 111.1 mH (10 uH per step)
Accuracy	5% inductors used throughout. *@ 23 ± 5℃* *@ 1 KHz test frequency*
Max. Rating Current	10 mA DC or AC.
Internal Residual Inductance	Approx. 0.5 uH.
Power Supply	None.
Operating Temperature	0 ℃ to 50 ℃(32 ℉ to 122 ℉).
Operating Humidity	Less than 80% RH.
Weight	333 g/0.74 lb.
Dimension	14.7 cm x 11.7 cm x 5.5 cm. (5.79 x 4.61 x 2.16 inch).
Accessories	Operation Manual... 1 PC.

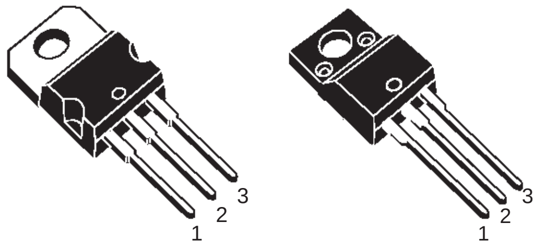
TESTING PROCEDURE
1) Start with all switches up (OUT) for min. inductance. 2) Switch down (IN) to add Inductance value. 3) The " Ground Terminal " is connected to the metal enclosure of all switches For some special application may connect the " Ground Terminal " to the external equipment to prevent other environment interference.

IRF540
IRF540FI

N - CHANNEL100V - 00.50Ω - 30A - TO-220/TO-220FI POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF540 IRF540FI	100 V 100 V	< 0.077 Ω < 0.077 Ω	30 A 16 A

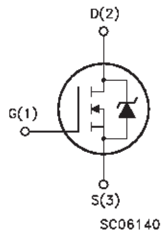
- TYPICAL $R_{DS(on)}$ = 0.050 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION



TO-220 TO-220FI

APPLICATIONS
- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- DC-DC & DC-AC CONVERTER
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMP DRIVERS Etc.)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		IRF530	IRF530FI	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	100		V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	100		V
V_{GS}	Gate-source Voltage	± 20		V
I_D	Drain Current (continuous) at T_c = 25 °C	30	17	A
I_D	Drain Current (continuous) at T_c = 100 °C	21	12	A
I_{DM}(•)	Drain Current (pulsed)	120	120	A
P_{tot}	Total Dissipation at T_c = 25 °C	150	45	W
	Derating Factor	1	0.3	W/°C
Viso	Insulation Withstand Voltage (DC)	-	2000	V
T_{stg}	Storage Temperature	-65 to 175		°C
T_j	Max. Operating Junction Temperature	175		°C

(•) Pulse width limited by safe operating area

(1) I_{SD} 3 30 A, di/dt 3 200 A/µs, V_{DD} 3 $V_{(BR)DSS}$, Tj 3 T_{JMAX}

THERMAL DATA

		TO-220	TO220-FI	
$R_{thj-case}$	Thermal Resistance Junction-case Max	1	3.33	$^oC/W$
$R_{thj-amb}$ $R_{thc-sink}$ T_l	Thermal Resistance Junction-ambient Max Thermal Resistance Case-sink Typ Maximum Lead Temperature For Soldering Purpose	62.5 0.5 300		$^oC/W$ $^oC/W$ ^oC

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max	30	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 ^oC, I_D = I_{AR}, V_{DD} = 25 V)	200	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 ^oC unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 μA V_{GS} = 0	100			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125 ^oC			1 10	μA μA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (∗)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 μA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 15 A		0.05	0.077	Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ V_{GS} = 10 V	30			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (∗)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ I_D = 15 A	10	20		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		2600 350 85	3600 500 120	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 50 V I_D = 15 A R_G = 4.7 Ω V_{GS} = 10 V		20 60	28 85	ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} =80 V I_D =30 A V_{GS} = 10 V		80 13 28	110	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 80 V I_D =30 A R_G = 4.7 Ω V_{GS} = 10 V		22 25 55	30 35 75	ns ns ns

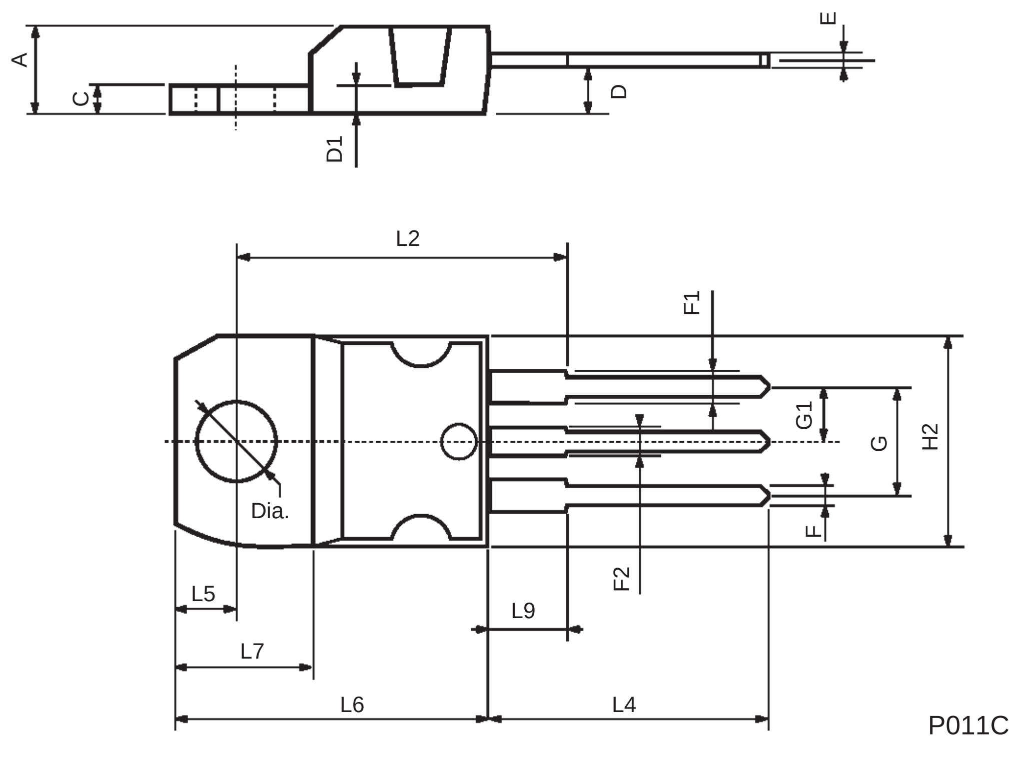
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				30 120	A A
V_{SD} (∗)	Forward On Voltage	I_{SD} = 50 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} =30 A di/dt = 100 A/μs V_{DD} = 30 V T_j = 150 °C		175 1.1 12.5		ns μC A

(∗) Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

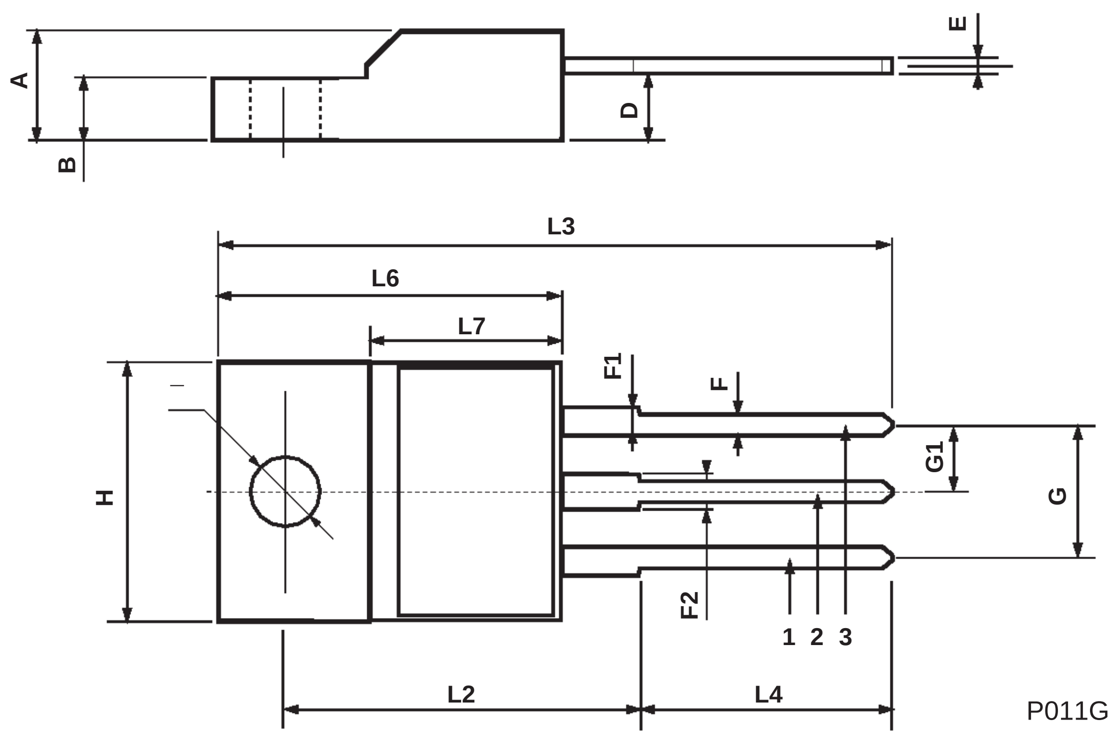
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



ISOWATT220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



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