Thesis (Summer 2015)

Report on

SIMULATION BASED STUDY OF NON-PLANAR MULTIGATE INDIUM GALLIUM ARSENIDE QUANTUM WELL FIELD EFFECT TRANSISTORS

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DECLARATION

We hereby declare that the thesis titled "SIMULATION BASED STUDY OF NON-PLANAR MULTIGATE INDIUM GALLIUM ARSENIDE QUANTUM WELL FIELD EFFECT TRANSISTORS" is submitted to the Department of Electrical and Electronic Engineering of BRAC University in partial fulfilment of the Bachelor of Science in Electrical and Electronic Engineering. This is our original work and was not submitted elsewhere for the award of any other degree or any other publication.

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ACKNOWLEDGEMENTS

We would like to thank our supervisor Dr. Mohammed Belal Hossain Bhuian and co-supervisor Atanu Kumar Saha for giving us the opportunity to work on this topic. Their constant support and guidelines throughout the whole span of the thesis was critical to our success. We would like to mention Dr. Supriyo Datta and his book Quantum Transport. It was very helpful in constructing our simulator. Lastly a very special tribute to the book Semiconductor Physics and Devices by Donald A. Neamen for giving us a thorough knowledge of the basic semiconductor devices.

TABLE OF CONTENTS

List of Figures……………………………………………………………………………v

List of Tables…………………………………………………………………………...vii

Abbreviations…………………………………………………………………………..viii

Nomenclature………………………………………………………………………….. .ix

Abstract………………………………………………………………………………….1

1. INTRODUCTION…………………………………………………………….............2

    1.1 The evolution of FET…………………………………...……….............2

    1.2 Junction Field Effect Transistor……………………………………….............3

    1.3 Metal Oxide Semiconductor Field Effect Transistor……………………….............5

    1.4 High Electron Mobility Transistor………………………………………………....8

    1.5 Quantum Well Field Effect Transistor………………………………………………10

    1.6 Non-planar multigate structure and FINFET technology……………………………11

    1.7 Motivation of QWFETs……………………………………………………………...12

2. SOLUTION OF SCHRÖDINGER EQUATION…………………………………………13

    2.1 Schrödinger equation…………………………………………………………....13

    2.2 Time independent Schrödinger equation……………………………………………..13

    2.3 Solving Schrödinger equation using the Finite difference method…………………..14

    2.4 Schrödinger equation for a 1-D lattice…………………………………………….....15

    2.5 Schrödinger equation for a 2-D lattice………………………………………….,,,.17

    2.6 Schrodinger equation for 1-D lattice with different materials………..……………..19

    2.7 Simulation of potential wells by solving Schrödinger equation……………………...21

3. SOLUTION OF POISSON'S EQUATION……………………………………………….22

    3.1 Poisson's equation……………………………………………………….............22

    3.2 Solving Poisson's equation for a 1-D lattice using Finite difference method………..23

    3.3 Solving Poisson's equation for a 2-D lattice…………………………..………….25

    3.4 Solving Poisson's equation for 1-D lattice with different materials………………....27

    3.5 Generation of energy band-diagrams by Schrödinger-Poisson coupled simulations...29

4. CAPACITANCE CALCULATION……………………………………………………31

5. SELF-CONSISTENT SIMULATION APPROACH……………………………………...32

5.1 Lattice construction……..32
5.2 Hamiltonian generation……32
5.3 Poisson solver……...32
5.4 Band-diagram generation…….....32
5.5 Schrödinger solver……32
5.6 Charge density……..32
5.7 Schrödinger-Poisson coupling……..33
5.8 Variation in gate-voltage……..33
5.9 Capacitance calculation……33
5.10 Flowchart of simulation……..34

6. BENCHMARKING…….35

7. 3-D MODEL OF SIMULATED DEVICES…….....36

8. SIMULATION RESULTS.......38

8.1 Equilibrium 3-D band-diagram……..38
8.2 Contour plots of band-diagram…….39
8.3 Band profiles for varying gate voltages...……...40
8.4 Charge density plot……...42
8.5 Charge density vs. gate voltage graph……..44
8.6 Capacitance vs. gate voltage curve……...45

9. CONCLUSION……......……46

REFERENCES……...47

LIST OF FIGURES

Fig.1.1: A pn-JFET at zero gate voltage…………………………………………………....3

Fig.1.2: A pn-JFET at negative gate voltage showing depletion regions……………………..4

Fig.1.3: An n-channel MESFET…………………………………………………………....4

Fig.1.4: An n-channel MESFET at negative gate voltage. …………………………….......5

Fig.1.5: A p-type MOSFET……………………………………………………………......6

Fig.1.6: A p-type MOSFET with gate voltage exceeding the threshold voltage and leading to channel formation……………………………………………………………………………..6

Fig.1.7: NMOS and PMOS symbols………………………………………………………..7

Fig. 1.8: A CMOS inverter…………………………………………………………….…7

Fig. 1.9: A heterojunction showing the formation of a quantum well……………………......8

Fig. 10: A GaAs HEMT……………………………………………………………………….9

Fig. 11: A double heterostructure showing the formation of quantum wells at the edges…...10

Fig. 12: A non-planar device with the gate wrapped around the 'fin' shaped channel……....11

Fig. 13: An infinite potential well with discrete energy levels having different shaped electron wave functions…………………………………………………………………………..…21

Fig.2.2: An electron wavefunction inside a 2-D potential well………………………………21

Fig. 3.1: The band profile generated after the first iteration……………………….............29

Fig.3.2: The charge density for the band diagram shown in Fig. 3.1………………………...29

Fig.3.3: The band profile after coupling…………………………………………………...30

Fig.3.4: The charge density for the band diagram shown in Fig 3.3…………………………30

Fig. 6.1: A 3-D model of InGaAs QWFET with InP spacer layer…………………………...35

Fig.6.2: The C-V curves of the simulated device and the original device…………………...35

Fig. 14: A 3-D model of InGaAS QWFET with InAlAs spacer layer……………………….37

Fig. 15: A 3-D model of InGaAs QWFET with Si-δ doping layer inside the InAlAs spacer layer………………………………………………………………………………………..37

Fig. 8.1: The 3-D equilibrium band diagram of InGaAs QWFET with InAlAs spacer layer..38

Fig. 8.2: The 3-D equilibrium band diagram of InGaAs QWFET with InAlAs spacer layer containing a thin Si-δ doping layer..38

Fig.8.3: Contour plot of QWFET with plain InAlAs spacer layer…………………………..39

Fig.8.4: Contour plot of QWFET with Si-δ doping layer inside InAlAs spacer layer……..39

Fig.8.5: Band profile of undoped QWFET along x-axis for V_G= 0V, 0.3V, 0.6 V and 0.9V…………………………………………………………………………………………40

Fig.8.6: Band profile of undoped QWFET along z-axis for V_G = 0V, 0.3V, 0.6 V and 0.9V…………………………………………………………………………………………40

Fig.8.7: Band profile along x-axis for V_G = 0V, 0.3V, 0.6 V and 0.9V……………………..41

Fig.8.8: Band profile along z-axis for V_G = 0V, 0.3V, 0.6 V and 0.9V……………………...41

Fig. 8.9: Charge density plot of undoped QWFET…………………………………………..42

Fig.8.10a: Charge density plot of doped QWFET at V_G=0.9V……………………………...43

Fig.8.10b: Charge density plot of doped QWFET at V_G=1.1V……………………………...43

Fig.8.11: Charge density vs. gate voltage graph of undoped QWFET………………………44

Fig.8.12: Charge density vs. gate voltage graph of doped QWFET…………………………44

Fig.8.13: C-V curves of four different QWFETs. The Si-δ doped QWFET has the greatest capacitance……………………………………………………………………………...45

LIST OF TABLES

Table.1 Lattice parameters…………………………………………………………………...33

ABBREVIATIONS

FET	Field Effect Transistor
JFET	Junction Field Effect Transistor
MESFET	Metal Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
HEMT	High Electron Mobility Transistor
QWFET	Quantum Well Field Effect Transistor
C-V	Capacitance -voltage

NOMENCLATURE

GaAs	Gallium Arsenide
HfO_2	Hafnium (IV) Oxide
InGaAs	Indium Gallium Arsenide
InAlAs	Indium Aluminium Arsenide
InP	Indium Phosphide
Si	Silicon

ABSTRACT

QWFETs with non-planar, multigate structures are known to provide higher electrostatistics than their conventional planar counterparts. Due to this desirable feature of the non-planar, multigate architecture, the electronics community is leaning towards transistors having gates wrapped around the channel for higher scalability and performance.

In this work, 2-D Schrodinger-Poisson coupled simulations of non-planar, multigate InGaAs QWFETs were carried out using an in-house simulator to study the performance of the devices based on the C-V characteristics. The simulator was carefully benchmarked to evaluate its accuracy before carrying out the simulations. Two InGaAs QWFETs with InAlAs spacer layers were simulated. The first device had a plain InAlAs spacer layer and the second device contained a Si δ-doped layer between InAlAs spacer layer. The simulation results showed that the device with the plain InAlAs spacer layer had a threshold voltage of 0.3V and C-V characteristics similar to that of a device with an InP spacer layer which was used for benchmarking. The second device which contained a thin Si δ-doped layer within the InAlAs spacer layer was simulated next. From the simulation results, it was seen that the device had a threshold voltage of 0.2V and an effective improvement in C-V characteristics was also observed compared to the device with plain InAlAs layer.

1. INTRODUCTION

1.1 The evolution of FET

The field effect transistor, more commonly known as FET is a semiconductor device with the basic principle of controlling the conductivity of the device, hence the flow of charge or current in the channel by changing the voltage applied. The concept of the field effect transistor (FET) has been around since as early as the 1920s, earlier than that of the BJT (bipolar junction transistor) however the first FETs were produced much later than the BJTs only after the emergence of suitable semiconductor materials and technology. A FET has three terminals namely the gate, source and drain. As stated earlier, the functioning of the FET involves regulating the flow of charge from the source to drain by regulating the voltage applied to the gate. Over the years, FETs have undergone numerous evolutions, each change leading to a shrink in the transistor size and increase in the number of transistors in an integrated circuit, staying true to Moore's law. The first FET produced was the JFET (Junction field effect transistor) in the 1950s, initiating a saga of semiconductor devices, with the basic concept of controlling the channel conductance by changing the gate voltage. The JFET was replaced by the metal oxide semiconductor field effect transistor (MOSFET), which is the most well-known FET to date and is responsible for revolutionizing the world of electronics. The CMOS technology which employs an NMOS and a PMOS has been the heart of all logic applications till date. With the progress of technology, the channel length of MOSFETs was reduced to improve performance, leading to an overall scale down of the devices which also resulted in the increase in doping of the channel. However a major shortcoming of the MOSFET is the adverse effect of heavy doping in the channel namely the reduction in carrier mobility [1]. To overcome this adversity, transistors with undoped channels were designed. The HEMT or high electron mobility transistor is one such transistor that has been developed to avoid the problem of heavy doping in the channel by employing a quantum well in an undoped channel for charge accumulation [12]. As the development continues, the boundaries of the FETs with planar architecture especially in terms of scalability have been pushed to the limit. Now the electronics world, has turned its attention to non-planar FETs to provide higher scalability, lower power consumption and faster operations, with the FINFET technology being the most exciting prospect.

1.2 Junction Field Effect Transistor

The JFET is the earliest field effect transistor to be produced. There are two categories of JFET, the pn junction field effect transistor (pn JFET) and the metal semiconductor field effect transistor or MESFET [12]. The difference between the two is that in a pn JFET, as the name suggests a pn junction is employed and in a MESFET a Schottky barrier rectifying junction is used. JFETs are usually turned off by applying the correct voltage, hence they are depletion mode devices.

- **pn-JFET**

Like all FETs, the pn-JFET has three terminals, the gate, source and drain. A differential voltage is applied to the source and drain such that current flows from the drain to the source. The region between the source and drain is called the channel. The channel can be n-type or p-type. There are two gate terminals joined to the channel via regions having opposite doping to the channel, such that pn junctions are formed between the channel and the gates. Considering an n-channel pn-JFET, with p-doped gate terminals as shown in Fig.1.1, depletion layers will form in the gate-channel junctions. When a negative voltage is applied to the gate terminals the depletion layers will widen and decrease electron flow in the channel. As voltage becomes more negative the depletion layers will become wider and channel conductivity will decrease (Fig.1.2). This is the principle of controlling the channel conductivity.

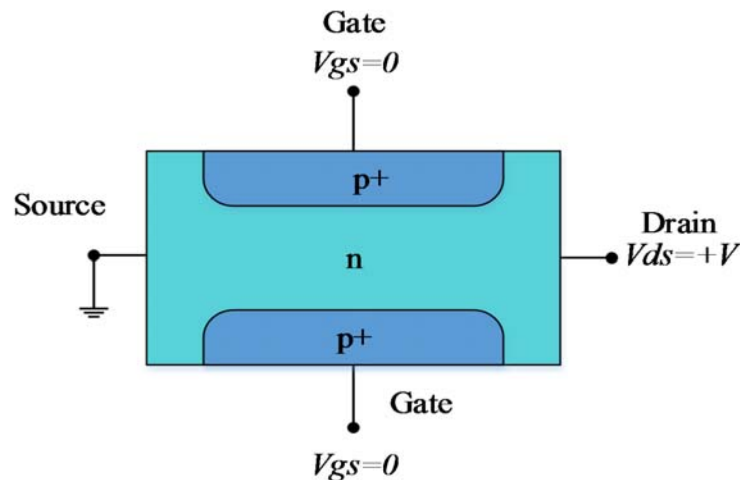


Fig.1.1: A pn-JFET at zero gate voltage.

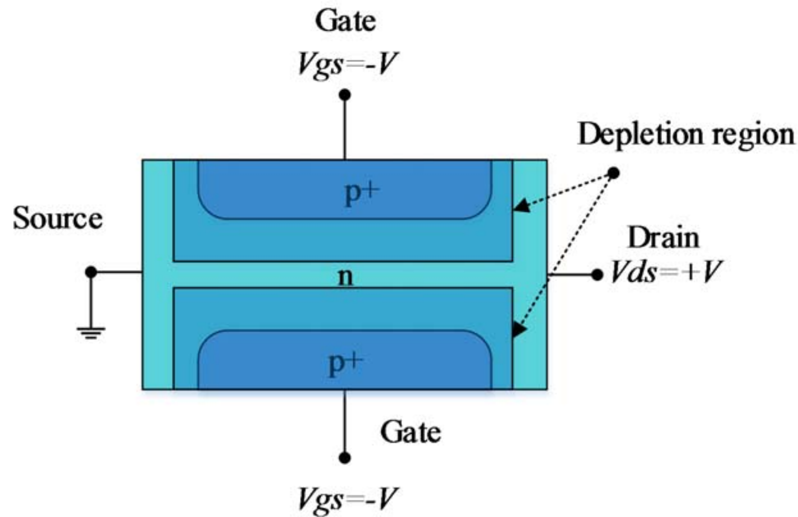


Fig.1.2: A pn-JFET at negative gate voltage showing depletion regions.

- **MESFET**

A MESFET has a gate terminal with a Schottky contact above the channel on top of a substrate. With the application of a reverse biased gate-to-source voltage, a depletion layer is created in the channel under the gate and as the voltage is increased it will eventually reach the substrate and cease further flow of current. An n-channel MESFET is shown in Fig.1.3, as the reverse-bias voltage is increased, the depletion region will widen and cover the width of the channel (Fig.1.4).

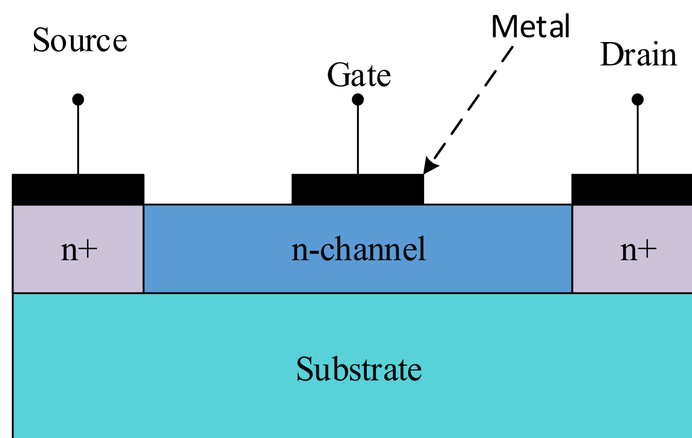


Fig. 1.3: An n-channel MESFET.

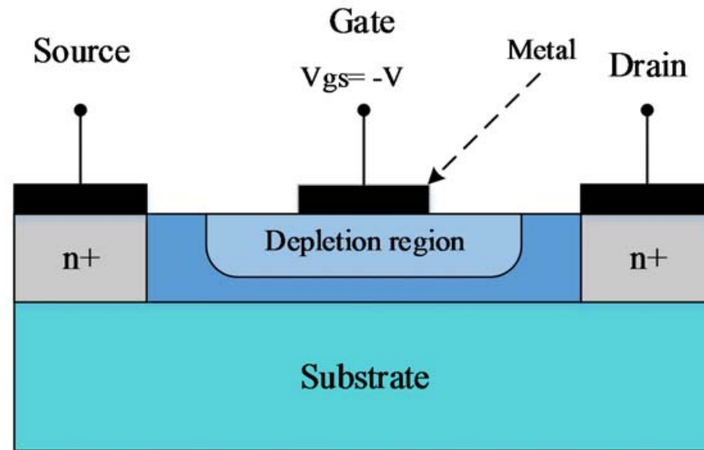


Fig. 1.4: An n-channel MESFET at negative gate voltage.

1.3 Metal Oxide Semiconductor Field Effect Transistor

The MOSFET is almost similar to a MESFET except the fact that it has an insulator between the metal and semiconductor, hence the name metal oxide semiconductor (MOS) FET. In a MOSFET, the substrate either n-type or p-type, is connected to the gate via the oxide usually through the center of the device. The source and drain terminals are connected to regions oppositely doped to the substrate, at either end of the device. When a voltage is applied to the gate, depending on the doping of the substrate, charge accumulation or the creation of a depletion layer will occur in the substrate below the oxide. Considering a p-type MOSFET (substrate is p-doped) depicted in Fig.1.5, applying a positive voltage at the gate will lead to a build-up of positive charge on the gate surface. This will induce an electric field inside the substrate such that the holes near the oxide-semiconductor interface will be repelled and create a depletion region. Since the substrate is p-type, the depletion layer will have negatively charged acceptor ions. As the voltage is increased, the electric field gets stronger and a larger depletion layer forms. As the gate voltage exceeds the threshold voltage, the minority carrier electrons in the p-type are attracted towards the interface creating an inversion layer of electrons which connect the n-type source and drain (Fig.1.6)

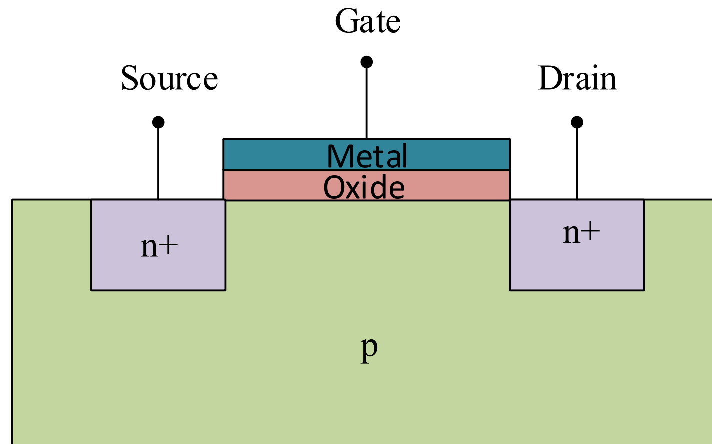


Fig. 1.5: A p-type MOSFET.

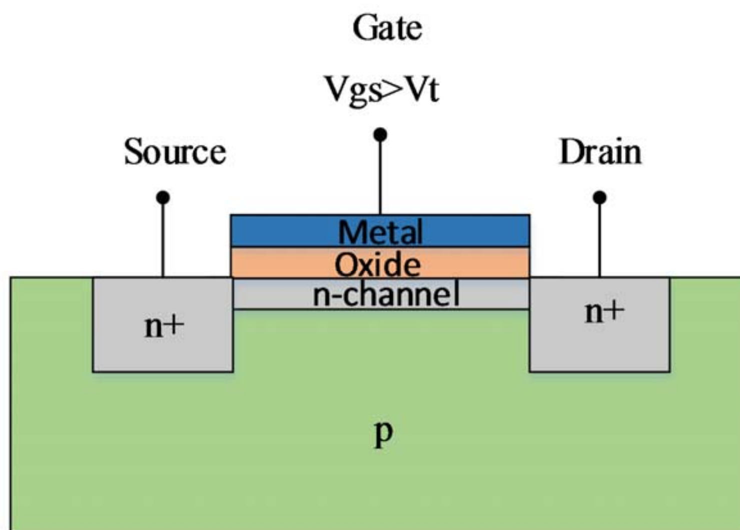


Fig. 1.6: A p-type MOSFET with gate voltage exceeding the threshold voltage and leading to channel formation.

NMOS & PMOS

An n-channel MOSFET is commonly called NMOS, whereas PMOS is a MOSFET with a p-channel. Fig.1.7 shows the symbol of the NMOS and PMOS. Simulation and studies have been done using Silvaco^{TM} to find the effect of oxide thickness on the C-V characteristics of NMOS devices [17].

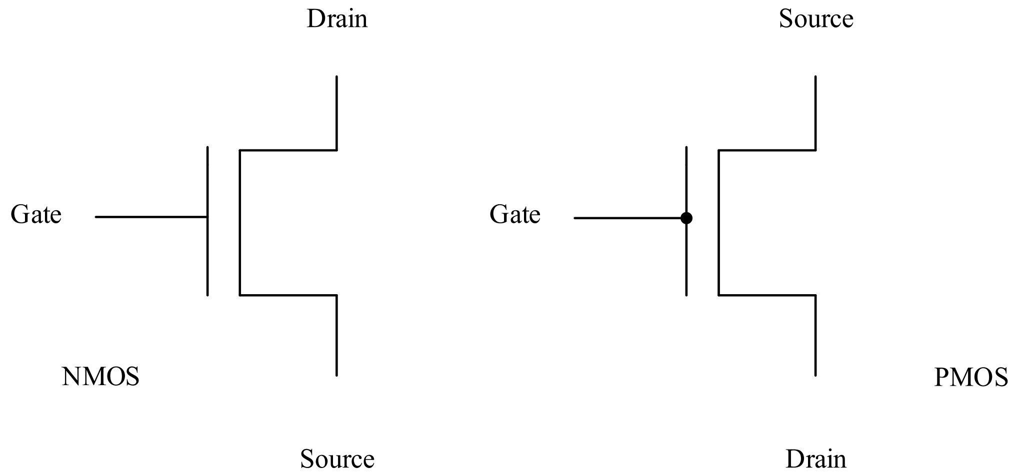


Fig. 1.7: NMOS and PMOS symbols.

CMOS

Circuits that use the CMOS or Complementary Metal Oxide Semiconductor technology utilizes both the NMOS and PMOS transistors. The biggest advantage of the CMOS technology is its low power consumption. Moreover, it is relatively inexpensive (since fewer transistors are used).

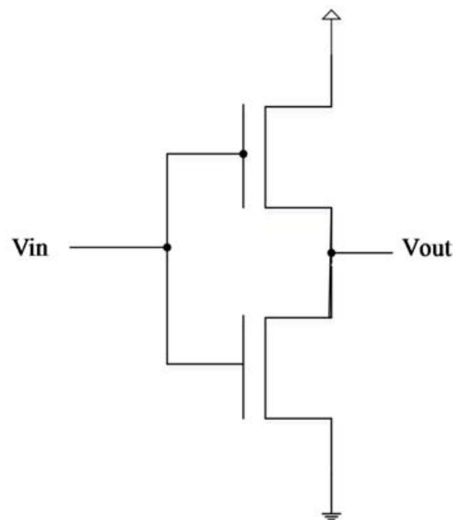


Fig. 1.8: A CMOS inverter.

1.4 High Electron Mobility Transistor

The HEMT employs a quantum well for the purpose of charge accumulation; such a well is formed in the junction of two semiconductor materials with different band gaps or a heterojunction as illustrated below in Fig.1.9 [7][10]. The idea is to avoid doping inside the channel to enhance carrier mobility by reducing scattering. In a GaAs HEMT (Fig.1.10), a heavily doped (n+) AlGaAs layer is joined to the intrinsic GaAs channel. Due to band gap difference between the two materials, a well is formed in the GaAs channel. Electrons from the heavily doped AlGaAs layer will cross the junction and accumulate in the well in the GaAs channel. The gate voltage controls the electron concentration inside the well, as the gate voltage is increased the electron concentration will increase. Thus, electrons can travel from the source to the drain via the channel with greater mobility as scattering is reduced.

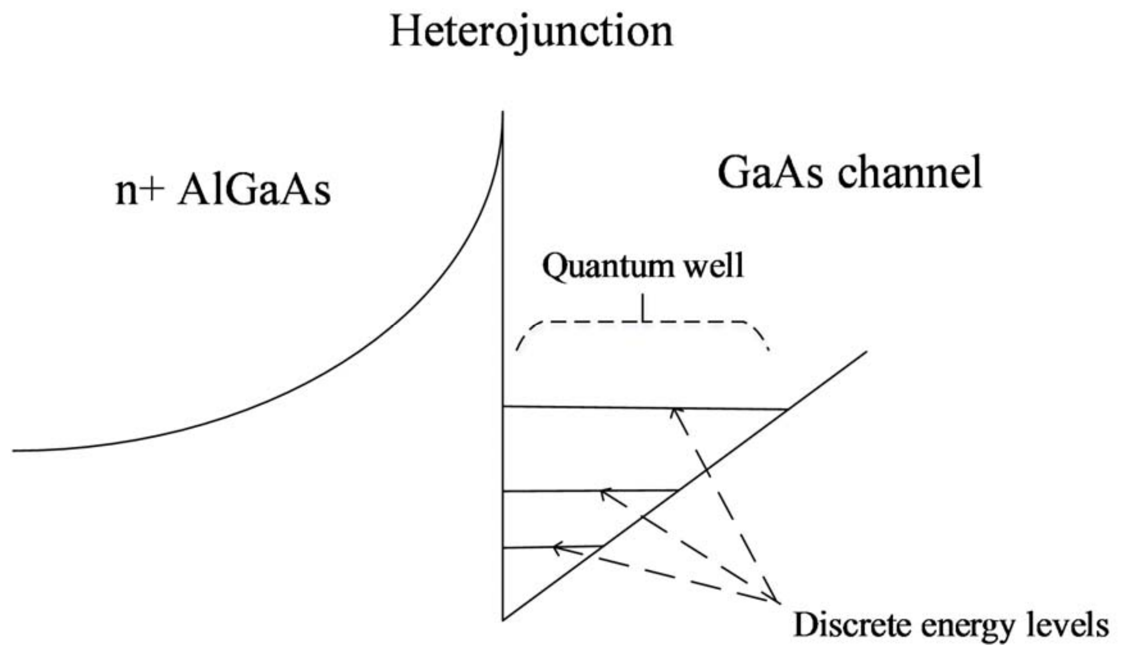


Fig. 1.9: A heterojunction showing the formation of a quantum well.

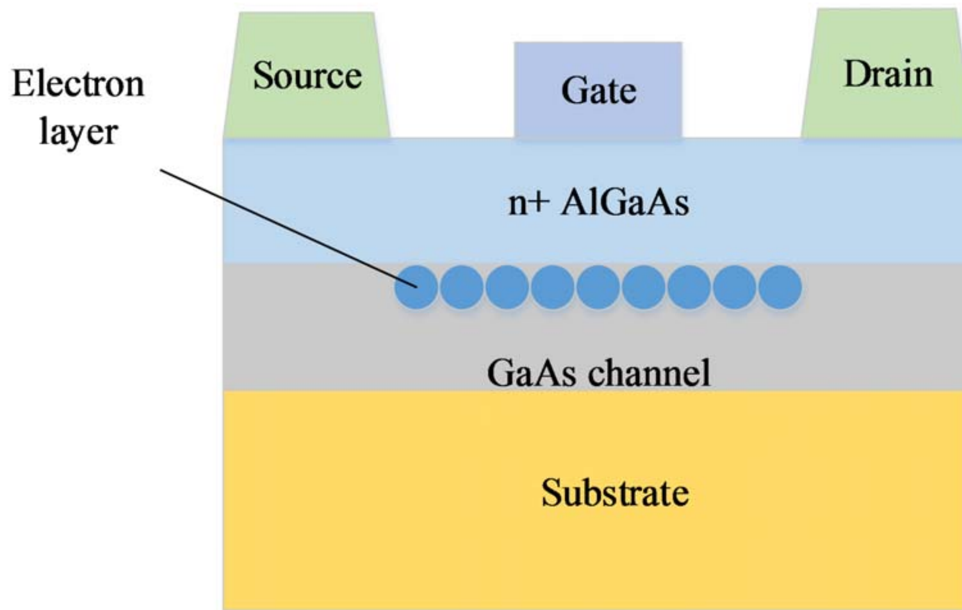


Fig. 1.10: A GaAs HEMT.

1.5 Quantum Well Field Effect Transistor

HEMTs that have the undoped channel positioned between two high band gap materials essentially contain two heterojunctions leading to the formation of quantum wells at the edges of the channel [7][9][10]. This is also known as a double heterostructure. The idea behind having the channel between two high band gap materials is to use high band gap materials as potential barriers and at the same time increase electron concentration in the channel. As electrons will move from the doped regions into the channel from both ends via the quantum wells, the channel will have higher charge accumulation. Moreover, with the addition of another potential barrier, the electrons are essentially trapped in the channel region. In Fig.1.11 a GaAs QWFET with n+ AlGaAs top and bottom barriers are shown.

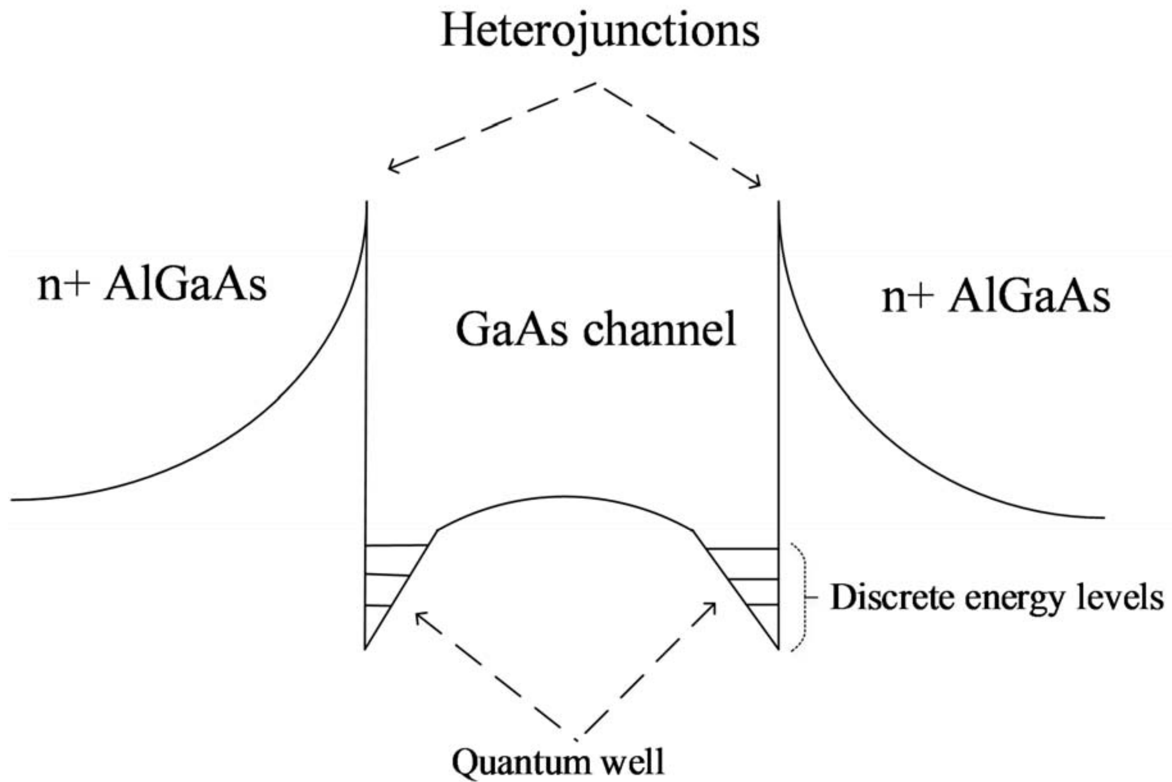


Fig. 1.11: A double heterostructure showing the formation of quantum wells at the edges.

1.6 Non-planar multigate structure and FINFET

There are two broad classifications in device architecture namely planar and non-planar. In planar architecture, the device is fabricated such that the semiconductor materials are stacked on top of each other or placed in layers. The non-planar architecture is different than the planar in the sense that not all materials are placed above one another, some are wrapped around others. The FINFET has a distinct 'fin' shaped channel on top of the substrate which is wrapped by the gate (Fig.1.12). As the gate is placed around the channel in more than one side, the term multigate is used [11]. Such a non-planar multigate architecture allows better gate control and hence, higher electrostatistics as opposed to planar architectures with the gate only on top. FINFETs have the potential to take CMOS scaling below the 22nm mark [14]. Moreover according to International Technology Roadmap for Semiconductors [13], [17] FINFETs are tipped to replace conventional MOSFETs in a bid to take scaling to a 10nm size.

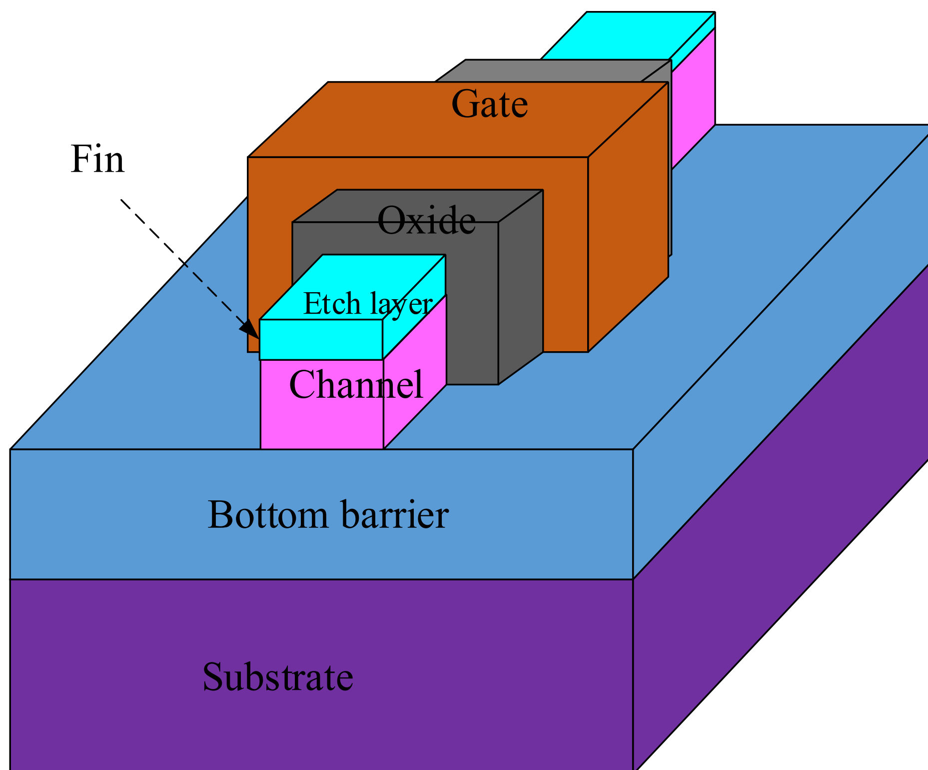


Fig. 1.12: A non-planar device with the gate wrapped around the 'fin' shaped channel.

1.7 Motivation of QWFETs

The usage of quantum wells in FETs have led to drastic improvement in terms of performance and service over the years. Moreover, non-planar structures have a lot to offer in terms of scalability and gate control. The possibility of high speed, low power applications using non-planar QWFETs make it more in demand. Modifications regarding the type of materials used, the thickness of the oxide and the amount of doping are still being carried out and they hold very interesting prospects for the future. The scope of improving the QWFETs to suit the needs of the electronics community is a vast and a worthy challenge. Most of the studied or modified QWFETs have shown better electrostatics and better performance in various aspects and this paper proves how small changes in the layers and materials can lead to a better performing device.

In the past, simulation based study of semiconductor devices using 1-D Schrodinger-Poisson coupled simulations have been conducted. However, 2-D Schrodinger-Poisson coupled simulations have not been done extensively .This paper is based on two QWFET structures and highlights the differences between them. The first was an InGaAs QWFET with InAlAs spacer layer. The second device was an InGaAs QWFET with a Si-δ doping layer inside the InAlAs spacer layer. Compared to the QWFET with only the InAlAs spacer layer, the one with δ doping layer inside the InAlAs spacer layer showed improved electrostatics and performance which will be further explained in the coming chapters.

2. SOLUTION OF SCHRÖDINGER EQUATION

2.1 Schrödinger equation

Schrödinger equation is a partial differential equation that can be solved to find the electron wave function of a material. The Schrödinger's equation has two forms namely the time independent and the time dependent. Since the system under consideration is an equilibrium system, the time independent form of the Schrödinger equation has been used.

2.2 Time independent Schrödinger equation

General form,

$$E\psi = \hat{H}\psi$$

Where,

$\hat{H}$ = Hamiltonian operator

ψ =Electron wave function

E =Total energy of the system

For a single non-relativistic particle the Schrödinger equation has the form,

$$E\psi(r) = [-\frac{\hbar}{2m^*}\nabla^2 + V(r)]\psi(r)$$

Where,

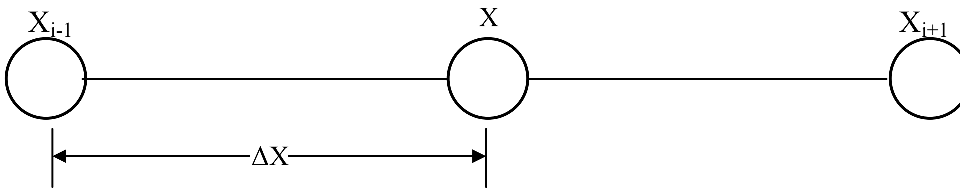
m^* = Effective mass of an electron of the system

∇^2 =Laplacian operator

$V(r)$ =Potential profile

2.3 Solving Schrödinger equation using the Finite difference method

Schrödinger equation can be solved numerically using the finite difference method. According to the finite difference method, differential equations can be approximated by difference equations.



For a finite Δx, the following approximations of first order derivatives are:

Forward difference approximation:

$$f'(x) \approx \frac{f(x+\Delta x) - f(x)}{\Delta x}$$

Backward difference approximation:

$$f'(x) \approx \frac{f(x) - f(x+\Delta x)}{\Delta x}$$

Central difference approximation:

$$f'(x) \approx \frac{f(x_{i+1}) - f(x_{i-1})}{2\Delta x}$$

As the central difference approximation yields the most accurate result, the central difference approximation has been used.

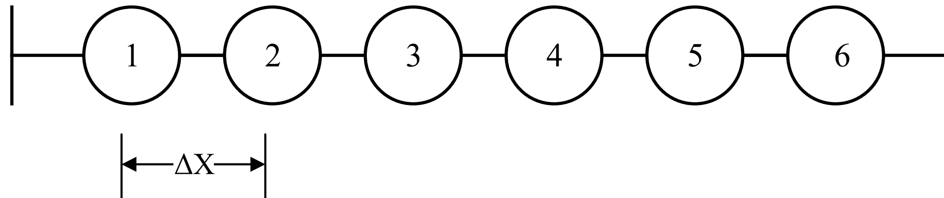
2.4 Schrödinger equation for a 1-D lattice

The second order derivative using the central difference approximation can be represented as,

$$f''(x) \approx \frac{f(x_{i+1}) - 2f(x) + f(x_{i-1})}{(\Delta x)^2}$$

Using the central difference approximation the Hamiltonian operator can be converted into a matrix form.

Assuming a discrete 1-D lattice having six points,



The Schrodinger equation for the above case can be represented as,

$$\mathrm{E}\begin{Bmatrix} \psi_1 \\ \psi_2 \\ \psi_3 \\ \psi_4 \\ \psi_5 \\ \psi_6 \end{Bmatrix} = \hat{H}\begin{Bmatrix} \psi_1 \\ \psi_2 \\ \psi_3 \\ \psi_4 \\ \psi_5 \\ \psi_6 \end{Bmatrix}$$

Assuming,

$$\mathrm{t} = \frac{\hbar}{2\mathrm{m}^{*}\Delta \mathrm{x}^{2}}$$

Where,

x=lattice parameter

For the discrete 1D lattice having six points the Hamiltonian matrix can be written as,

$$\hat{H}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\end{Bmatrix}=t\begin{bmatrix}-2&1&0&0&0&0\\1&-2&1&0&0&0\\0&1&-2&1&0&0\\0&0&1&-2&1&0\\0&0&0&1&-2&1\\0&0&0&0&1&-2\end{bmatrix}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\end{Bmatrix}+\begin{bmatrix}U_1&0&0&0&0&0\\0&U_2&0&0&0&0\\0&0&U_3&0&0&0\\0&0&0&U_4&0&0\\0&0&0&0&U_5&0\\0&0&0&0&0&U_6\end{bmatrix}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\end{Bmatrix}$$

$$\text{Or, }\hat{H}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\end{Bmatrix}=\begin{bmatrix}-2\mathrm{t}&\mathrm{t}&0&0&0&0\\\mathrm{t}&-2\mathrm{t}&\mathrm{t}&0&0&0\\0&\mathrm{t}&-2\mathrm{t}&\mathrm{t}&0&0\\0&0&\mathrm{t}&-2\mathrm{t}&\mathrm{t}&0\\0&0&0&\mathrm{t}&-2\mathrm{t}&\mathrm{t}\\0&0&0&0&\mathrm{t}&-2\mathrm{t}\end{bmatrix}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\end{Bmatrix}+\begin{bmatrix}\mathrm{U}_1&0&0&0&0&0\\0&\mathrm{U}_2&0&0&0&0\\0&0&\mathrm{U}_3&0&0&0\\0&0&0&\mathrm{U}_4&0&0\\0&0&0&0&\mathrm{U}_5&0\\0&0&0&0&0&\mathrm{U}_6\end{bmatrix}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\end{Bmatrix}$$

$$\text{Therefore, }\hat{H}=\begin{bmatrix}-2t&t&0&0&0&0\\t&-2t&t&0&0&0\\0&t&-2t&t&0&0\\0&0&t&-2t&t&0\\0&0&0&t&-2t&t\\0&0&0&0&t&-2t\end{bmatrix}+\begin{bmatrix}U_1&0&0&0&0&0\\0&U_2&0&0&0&0\\0&0&U_3&0&0&0\\0&0&0&U_4&0&0\\0&0&0&0&U_5&0\\0&0&0&0&0&U_6\end{bmatrix}$$

Overall equation,

$$\hat{H}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\end{Bmatrix}=\begin{bmatrix}-2t&t&0&0&0&0\\t&-2t&t&0&0&0\\0&t&-2t&t&0&0\\0&0&t&-2t&t&0\\0&0&0&t&-2t&t\\0&0&0&0&t&-2t\end{bmatrix}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\end{Bmatrix}+\begin{bmatrix}U_1&0&0&0&0&0\\0&U_2&0&0&0&0\\0&0&U_3&0&0&0\\0&0&0&U_4&0&0\\0&0&0&0&U_5&0\\0&0&0&0&0&U_6\end{bmatrix}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\end{Bmatrix}$$

This form of the Schrodinger equation can be treated as an Eigen value problem and can be solved for the Eigen vectors and the Eigen values.

2.5 Schrödinger equation for a 2-D lattice

General time-independent 2-D Schrodinger equation has the form,

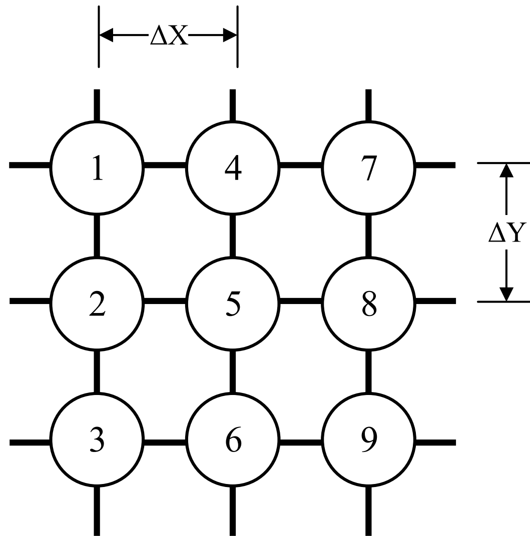
$$E\psi(x,y) = [-\frac{\hbar}{2m^*}\nabla^2 + U(x,y)]\psi(x,y)]$$

The equation above can be solved numerically using the finite difference method considering the central difference approximation. The second order derivative for 2-D can be represented as,

$$\psi''(x,y) = \frac{\psi(\mathrm{i},\mathrm{j}-1) + \psi(\mathrm{i}-1,\mathrm{j}) - 4\psi(\mathrm{i},\mathrm{j}) + \psi(\mathrm{i}+1,\mathrm{j}) + \psi(\mathrm{i},\mathrm{j}+1)}{\Delta x^2}$$

Using the equation above, the Hamiltonian operator can be converted to matrix form.

Assuming the 2-D lattice given below,



Considering Δx=Δy as the lattice parameter, the Schrodinger equation for the above case can be represented as,

$$E\begin{Bmatrix}\Psi_1\\ \Psi_2\\ \Psi_3\\ \Psi_4\\ \Psi_5\\ \Psi_6\\ \Psi_7\\ \Psi_8\\ \Psi_9\end{Bmatrix} = \hat{H}\begin{Bmatrix}\Psi_1\\ \Psi_2\\ \Psi_3\\ \Psi_4\\ \Psi_5\\ \Psi_6\\ \Psi_7\\ \Psi_8\\ \Psi_9\end{Bmatrix}$$

As considered previously $t = \frac{\hbar}{2m^* \Delta x^2}$, the Hamiltonian matrix then becomes,

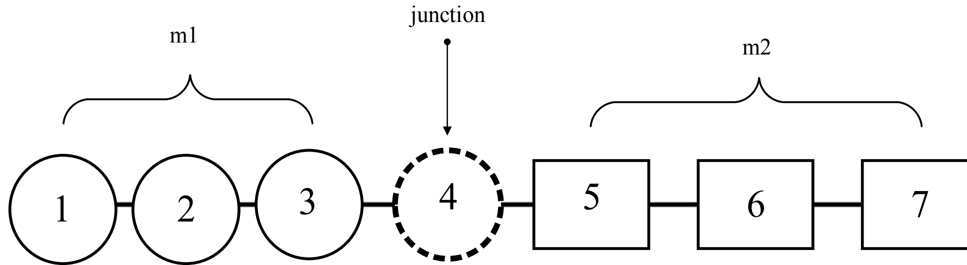
$$\hat{H} = \left[t\begin{pmatrix} -4 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0\\ 1 & -4 & 1 & 0 & 1 & 0 & 0 & 0 & 0\\ 0 & 1 & -4 & 0 & 0 & 1 & 0 & 0 & 0\\ 1 & 0 & 0 & -4 & 1 & 0 & 1 & 0 & 0\\ 0 & 1 & 0 & 1 & -4 & 1 & 0 & 1 & 0\\ 0 & 0 & 1 & 0 & 1 & -4 & 0 & 0 & 1\\ 0 & 0 & 0 & 1 & 0 & 0 & -4 & 1 & 0\\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & -4 & 1\\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & -4 \end{pmatrix} + \begin{pmatrix} U_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0\\ 0 & U_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & U_3 & 0 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & U_4 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & U_5 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & U_6 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & U_7 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & U_8 & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & U_9 \end{pmatrix} \right]$$

Where the potential profile, $U(x,y) = \begin{pmatrix} U_1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0\\ 0 & U_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & U_3 & 0 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & U_4 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & U_5 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & U_6 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & U_7 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & U_8 & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & U_9 \end{pmatrix}$

Using the aforementioned matrices, the Schrodinger equation can be solved to give a series of Eigen values and Eigen vectors for 2-D lattice of same material and lattice constant

2.6 Schrodinger equation for 1-D lattice with different materials

Assuming a 1-D discrete lattice of two different materials with seven points as shown below, with the lattice parameter Δx.



The Schrodinger equation for the above case can be represented as,

$$E\begin{Bmatrix}\psi_1\\ \psi_2\\ \psi_3\\ \psi_4\\ \psi_5\\ \psi_6\\ \psi_7\end{Bmatrix} = \hat{H}\begin{Bmatrix}\psi_1\\ \psi_2\\ \psi_3\\ \psi_4\\ \psi_5\\ \psi_6\\ \psi_7\end{Bmatrix}$$

Assuming,

$$t_1 = \frac{\hbar^2}{2m_1 * \Delta x^2}$$

$$t_2 = \frac{\hbar^2}{2m_2 * \Delta y^2}$$

Where x and y are the lattice constants for m1 and m2,

And $t_j = \frac{t_1 + t_2}{2}$

For the discrete 1-D lattice having seven points the equation can be written as,

$$\hat{H}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\\\psi_7\end{Bmatrix}=\begin{bmatrix}-2t_1 & t_1 & 0 & 0 & 0 & 0 & 0\\ t_1 & -2t_1 & t_1 & 0 & 0 & 0 & 0\\ 0 & t_1 & -2t_1 & t_1 & 0 & 0 & 0\\ 0 & 0 & t_1 & -2t_j & t_2 & 0 & 0\\ 0 & 0 & 0 & t_2 & -2t_2 & t_2 & 0\\ 0 & 0 & 0 & 0 & t_2 & -2t_2 & t_2\\ 0 & 0 & 0 & 0 & 0 & t_2 & -2t_2\end{bmatrix}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\\\psi_7\end{Bmatrix}+\begin{bmatrix}U_1 & 0 & 0 & 0 & 0 & 0 & 0\\ 0 & U_2 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & U_3 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & U_4 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & U_5 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & U_6 & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & U_7\end{bmatrix}\begin{Bmatrix}\psi_1\\\psi_2\\\psi_3\\\psi_4\\\psi_5\\\psi_6\\\psi_7\end{Bmatrix}$$

Where the Hamiltonian matrix is,

$$\hat{H}=\begin{bmatrix}-2t_1 & t_1 & 0 & 0 & 0 & 0 & 0\\ t_1 & -2t_1 & t_1 & 0 & 0 & 0 & 0\\ 0 & t_1 & -2t_1 & t_1 & 0 & 0 & 0\\ 0 & 0 & t_1 & -2t_j & t_2 & 0 & 0\\ 0 & 0 & 0 & t_2 & -2t_2 & t_2 & 0\\ 0 & 0 & 0 & 0 & t_2 & -2t_2 & t_2\\ 0 & 0 & 0 & 0 & 0 & t_2 & -2t_2\end{bmatrix}+\begin{bmatrix}U_1 & 0 & 0 & 0 & 0 & 0 & 0\\ 0 & U_2 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & U_3 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & U_4 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & U_5 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & U_6 & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & U_7\end{bmatrix}$$

And the potential profile, $U(x)=\begin{bmatrix}U_1 & 0 & 0 & 0 & 0 & 0 & 0\\ 0 & U_2 & 0 & 0 & 0 & 0 & 0\\ 0 & 0 & U_3 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & U_4 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & U_5 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & U_6 & 0\\ 0 & 0 & 0 & 0 & 0 & 0 & U_7\end{bmatrix}$

The above equations can be solved as done previously, to obtain a set of Eigen values and Eigen vectors.

2.7 Simulation of potential wells by solving Schrödinger equation

For a 1-D infinite potential well, the electron wavefunction for different energy levels can be calculated by solving the Schrödinger equation. Fig.2.1 below shows a 1-D infinite potential well. Solving the Schrödinger equation, the electron wave functions for discrete energy levels are found inside the well as shown. Fig.2.2 illustrates the electron wavefunction for a 2-D potential well.

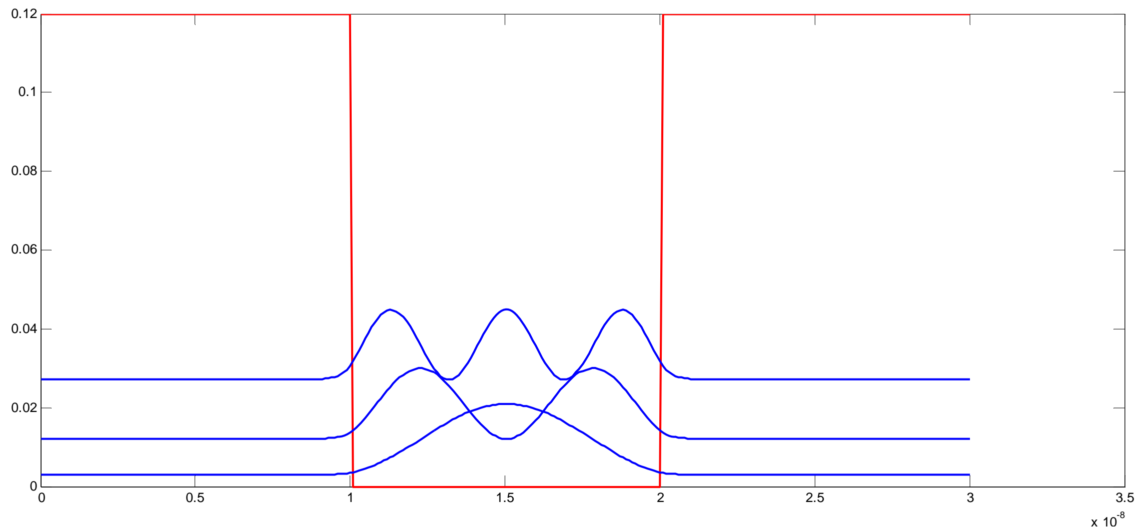


Fig. 2.1: An infinite potential well with discrete energy levels having different shaped electron wave functions.

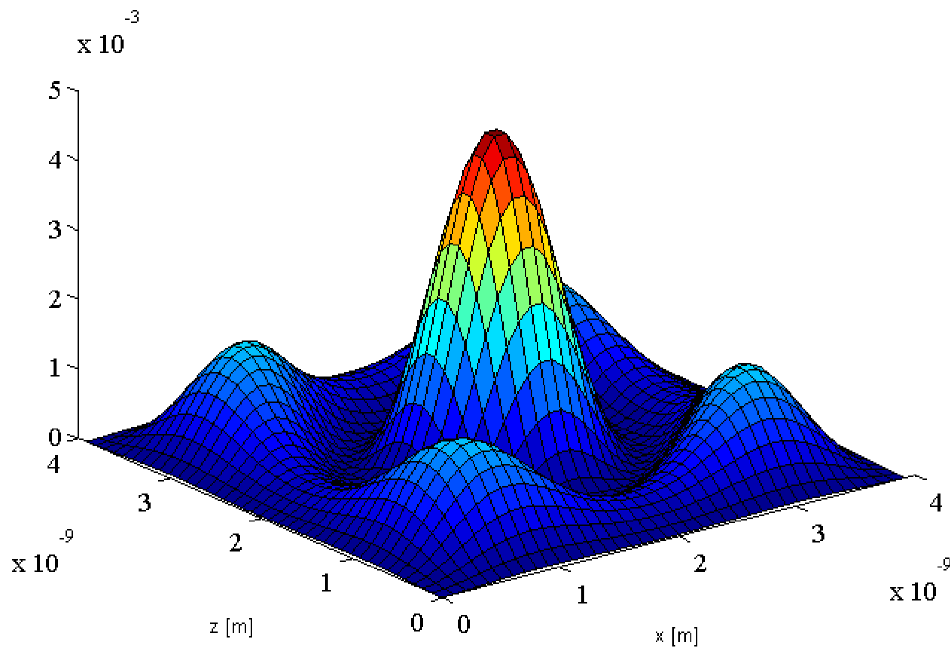


Fig.2.2: An electron wavefunction inside a 2-D potential well.

3. SOLUTION OF POISSON'S EQUATION

3.1 Poisson's equation

Poisson's equation is a partial differential equation. Poisson's equation can be solved to find the electric potential in a material for a particular charge density.

The general form of the Poisson's equation can be written as,

$$\nabla^2 \varphi = -\frac{\rho}{\varepsilon}$$

Where,

∇^2= Laplacian operator

φ = Electric potential

ρ = Charge density

ε = Absolute permittivity of the material, $[\varepsilon = \varepsilon_0 \varepsilon_r]$

Where, $\varepsilon_0 =$ Vacuum permittivity

$\varepsilon_r =$ Relative permittivity of the material

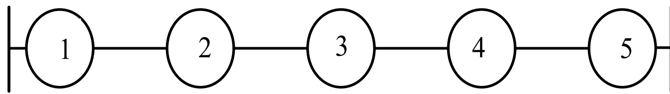
3.2 Solving Poisson's equation for a 1-D lattice using Finite difference method

Poisson's equation can be solved numerically using the finite difference method.

Using the central difference approximation we can write the second order derivative as,

$$f''(x) \approx \frac{f(x_{i+1}) - 2f(x) + f(x_{i-1})}{(\Delta x)^2}$$

Considering a 1-D discrete lattice of five points,



For the above case the Poisson's equation can be written in the following matrix form,

$$\begin{bmatrix} -2 & 1 & 0 & 0 & 0 \\ 1 & -2 & 1 & 0 & 0 \\ 0 & 1 & -2 & 1 & 0 \\ 0 & 0 & 1 & -2 & 1 \\ 0 & 0 & 0 & 1 & -2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} = - \begin{bmatrix} \rho_1 / \varepsilon_1 \\ \rho_2 / \varepsilon_2 \\ \rho_3 / \varepsilon_3 \\ \rho_4 / \varepsilon_4 \\ \rho_5 / \varepsilon_5 \end{bmatrix}$$

Where, $V_1, V_2 ..... V_5$ = electric potential

$$\text{Or, } \begin{bmatrix} -2\varepsilon_{r1} & \varepsilon_{r1} & 0 & 0 & 0 \\ \varepsilon_{r2} & -2\varepsilon_{r2} & \varepsilon_{r2} & 0 & 0 \\ 0 & \varepsilon_{r3} & -2\varepsilon_{r3} & \varepsilon_{r3} & 0 \\ 0 & 0 & \varepsilon_{r4} & -2\varepsilon_{r4} & \varepsilon_{r4} \\ 0 & 0 & 0 & \varepsilon_{r5} & -2\varepsilon_{r5} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} = - \begin{bmatrix} \rho_1 / \varepsilon_0 \\ \rho_2 / \varepsilon_0 \\ \rho_3 / \varepsilon_0 \\ \rho_4 / \varepsilon_0 \\ \rho_5 / \varepsilon_0 \end{bmatrix}$$

$$\text{If } [A] = \begin{bmatrix} -2\varepsilon_1 & \varepsilon_1 & 0 & 0 & 0 \\ \varepsilon_2 & -2\varepsilon_2 & \varepsilon_2 & 0 & 0 \\ 0 & \varepsilon_3 & -2\varepsilon_3 & \varepsilon_3 & 0 \\ 0 & 0 & \varepsilon_4 & -2\varepsilon_4 & \varepsilon_4 \\ 0 & 0 & 0 & \varepsilon_5 & -2\varepsilon_5 \end{bmatrix}, \quad [V] = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix}, \quad [F] = - \begin{bmatrix} \rho_1 / \varepsilon_0 \\ \rho_2 / \varepsilon_0 \\ \rho_3 / \varepsilon_0 \\ \rho_4 / \varepsilon_0 \\ \rho_5 / \varepsilon_0 \end{bmatrix}$$

Then,

$$[A][V]=[F]$$

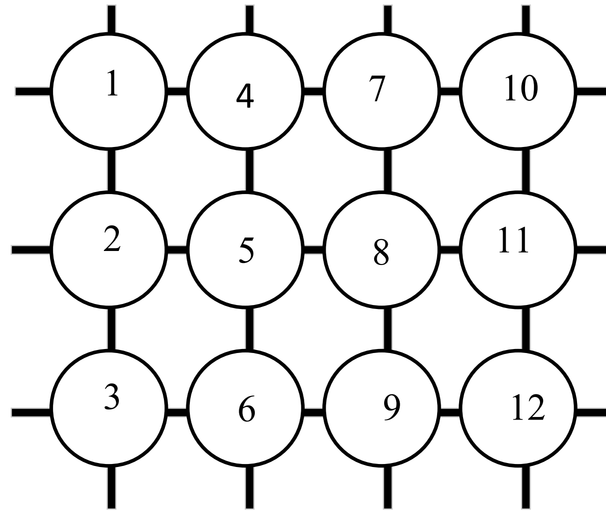
Or, $[V]=[A]^{-1}[F]$

Where,

$[A]^{-1}$ is the inverse matrix of matrix $[A]$

3.3 Solving Poisson's equation for a 2-D lattice

Considering a 2-D lattice,



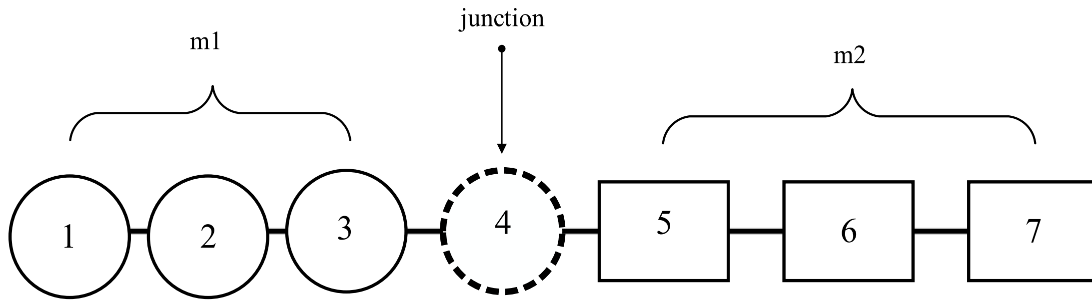
The Poisson's equation for the above can be written in the following matrix form,

$$\begin{bmatrix} -4 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -4 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -4 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -4 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & -4 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & -4 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & -4 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 1 & -4 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & -4 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & -4 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & -4 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & -4 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \\ V_8 \\ V_9 \\ V_{10} \\ V_{11} \\ V_{12} \end{bmatrix} = - \begin{bmatrix} \rho_1 / \varepsilon_1 \\ \rho_2 / \varepsilon_2 \\ \rho_3 / \varepsilon_3 \\ \rho_4 / \varepsilon_4 \\ \rho_5 / \varepsilon_5 \\ \rho_6 / \varepsilon_6 \\ \rho_7 / \varepsilon_7 \\ \rho_8 / \varepsilon_8 \\ \rho_9 / \varepsilon_9 \\ \rho_{10} / \varepsilon_{10} \\ \rho_{11} / \varepsilon_{11} \\ \rho_{12} / \varepsilon_{12} \end{bmatrix}$$

Or,

$$\begin{bmatrix} -4\varepsilon_{r1} & \varepsilon_{r1} & 0 & \varepsilon_{r1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \varepsilon_{r2} & -4\varepsilon_{r2} & \varepsilon_{r2} & 0 & \varepsilon_{r2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \varepsilon_{r3} & -4\varepsilon_{r3} & 0 & 0 & \varepsilon_{r3} & 0 & 0 & 0 & 0 & 0 & 0 \\ \varepsilon_{r4} & 0 & 0 & -4\varepsilon_{r4} & \varepsilon_{r4} & 0 & \varepsilon_{r4} & 0 & 0 & 0 & 0 & 0 \\ 0 & \varepsilon_{r5} & 0 & \varepsilon_{r5} & -4\varepsilon_{r5} & \varepsilon_{r5} & 0 & \varepsilon_{r5} & 0 & 0 & 0 & 0 \\ 0 & 0 & \varepsilon_{r6} & 0 & \varepsilon_{r6} & -4\varepsilon_{r6} & 0 & 0 & \varepsilon_{r6} & 0 & 0 & 0 \\ 0 & 0 & 0 & \varepsilon_{r7} & 0 & 0 & -4\varepsilon_{r7} & \varepsilon_{r7} & 0 & \varepsilon_{r7} & 0 & 0 \\ 0 & 0 & 0 & 0 & \varepsilon_{r8} & 0 & \varepsilon_{r8} & -4\varepsilon_{r8} & \varepsilon_{r8} & 0 & \varepsilon_{r8} & 0 \\ 0 & 0 & 0 & 0 & 0 & \varepsilon_{r9} & 0 & \varepsilon_{r9} & -4\varepsilon_{r9} & 0 & 0 & \varepsilon_{r9} \\ 0 & 0 & 0 & 0 & 0 & 0 & \varepsilon_{r10} & 0 & 0 & -4\varepsilon_{r10} & \varepsilon_{r10} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \varepsilon_{r11} & 0 & \varepsilon_{r11} & -4\varepsilon_{r11} & \varepsilon_{r11} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \varepsilon_{r12} & 0 & \varepsilon_{r12} & -4\varepsilon_{r12} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \\ V_8 \\ V_9 \\ V_{10} \\ V_{11} \\ V_{12} \end{bmatrix} = - \begin{bmatrix} \rho_1 / \varepsilon_0 \\ \rho_2 / \varepsilon_0 \\ \rho_3 / \varepsilon_0 \\ \rho_4 / \varepsilon_0 \\ \rho_5 / \varepsilon_0 \\ \rho_6 / \varepsilon_0 \\ \rho_7 / \varepsilon_0 \\ \rho_8 / \varepsilon_0 \\ \rho_9 / \varepsilon_0 \\ \rho_{10} / \varepsilon_0 \\ \rho_{11} / \varepsilon_0 \\ \rho_{12} / \varepsilon_0 \end{bmatrix}$$

3.4 Solving Poisson's equation for 1-D lattice with different materials



Assuming the same 1-D discrete lattice of two different materials with seven points as the Schrodinger solution in the previous section. The separation between the points is Δx. The generalized Poisson solution would be,

$$\nabla^2 V = -\frac{\rho}{\varepsilon}$$

Where,

$$\varepsilon = \varepsilon_0 \varepsilon_r$$

The Poisson equation will become,

$$\begin{bmatrix} -2 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & -2 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & -2 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -2 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & -2 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & -2 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & -2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \end{bmatrix} = - \begin{bmatrix} \rho_1 / \varepsilon_0 \varepsilon_{r1} \\ \rho_2 / \varepsilon_0 \varepsilon_{r1} \\ \rho_3 / \varepsilon_0 \varepsilon_{r1} \\ \rho_4 / \varepsilon_0 \varepsilon_{tj} \\ \rho_5 / \varepsilon_0 \varepsilon_{r2} \\ \rho_6 / \varepsilon_0 \varepsilon_{r2} \\ \rho_7 / \varepsilon_0 \varepsilon_{r2} \end{bmatrix}$$

Or,

$$\begin{bmatrix} -2\varepsilon_{r1} & \varepsilon_{r1} & 0 & 0 & 0 & 0 & 0 \\ \varepsilon_{r1} & -2\varepsilon_{r1} & \varepsilon_{r1} & 0 & 0 & 0 & 0 \\ 0 & \varepsilon_{r1} & -2\varepsilon_{r1} & \varepsilon_{r1} & 0 & 0 & 0 \\ 0 & 0 & \varepsilon_{r1} & -2\varepsilon_{tj} & \varepsilon_{r2} & 0 & 0 \\ 0 & 0 & 0 & \varepsilon_{r2} & -2\varepsilon_{r2} & \varepsilon_{r2} & 0 \\ 0 & 0 & 0 & 0 & \varepsilon_{r2} & -2\varepsilon_{r2} & \varepsilon_{r2} \\ 0 & 0 & 0 & 0 & 0 & \varepsilon_{r2} & -2\varepsilon_{r2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \end{bmatrix} = - \begin{bmatrix} \rho_1 / \varepsilon_0 \varepsilon_{r1} \\ \rho_2 / \varepsilon_0 \varepsilon_{r1} \\ \rho_3 / \varepsilon_0 \varepsilon_{r1} \\ \rho_4 / \varepsilon_0 \varepsilon_{tj} \\ \rho_5 / \varepsilon_0 \varepsilon_{r2} \\ \rho_6 / \varepsilon_0 \varepsilon_{r2} \\ \rho_7 / \varepsilon_0 \varepsilon_{r2} \end{bmatrix}$$

Where,

$$[A] = \begin{bmatrix} -2\varepsilon_{r1} & \varepsilon_{r1} & 0 & 0 & 0 & 0 & 0 \\ \varepsilon_{r1} & -2\varepsilon_{r1} & \varepsilon_{r1} & 0 & 0 & 0 & 0 \\ 0 & \varepsilon_{r1} & -2\varepsilon_{r1} & \varepsilon_{r1} & 0 & 0 & 0 \\ 0 & 0 & \varepsilon_{r1} & -2\varepsilon_{tj} & \varepsilon_{r2} & 0 & 0 \\ 0 & 0 & 0 & \varepsilon_{r2} & -2\varepsilon_{r2} & \varepsilon_{r2} & 0 \\ 0 & 0 & 0 & 0 & \varepsilon_{r2} & -2\varepsilon_{r2} & \varepsilon_{r2} \\ 0 & 0 & 0 & 0 & 0 & \varepsilon_{r2} & -2\varepsilon_{r2} \end{bmatrix}, \quad [V] = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \end{bmatrix}, \quad [F] = - \begin{bmatrix} \rho_1 / \varepsilon_0 \\ \rho_2 / \varepsilon_0 \\ \rho_3 / \varepsilon_0 \\ \rho_4 / \varepsilon_0 \\ \rho_5 / \varepsilon_0 \\ \rho_6 / \varepsilon_0 \\ \rho_7 / \varepsilon_0 \end{bmatrix}$$

Then again,

$$[A][V] = [F]$$

Therefore, $[V] = [A]^{-1}[F]$

$[A]^{-1}$ is the inverse matrix of matrix $[A]$

3.5 Generation of energy band-diagrams by Schrödinger-Poisson coupled simulations

Energy band diagrams in [6] are produced by Schrodinger-Poisson coupled simulations. Fig.3.1 shows the energy band diagram generated by a Schrodinger-Poisson simulation, after the first iteration. In Fig.3.3 the band diagram is reproduced after coupling. Fig 3.2 and Fig.3.4 display the charge densities before and after the coupling.

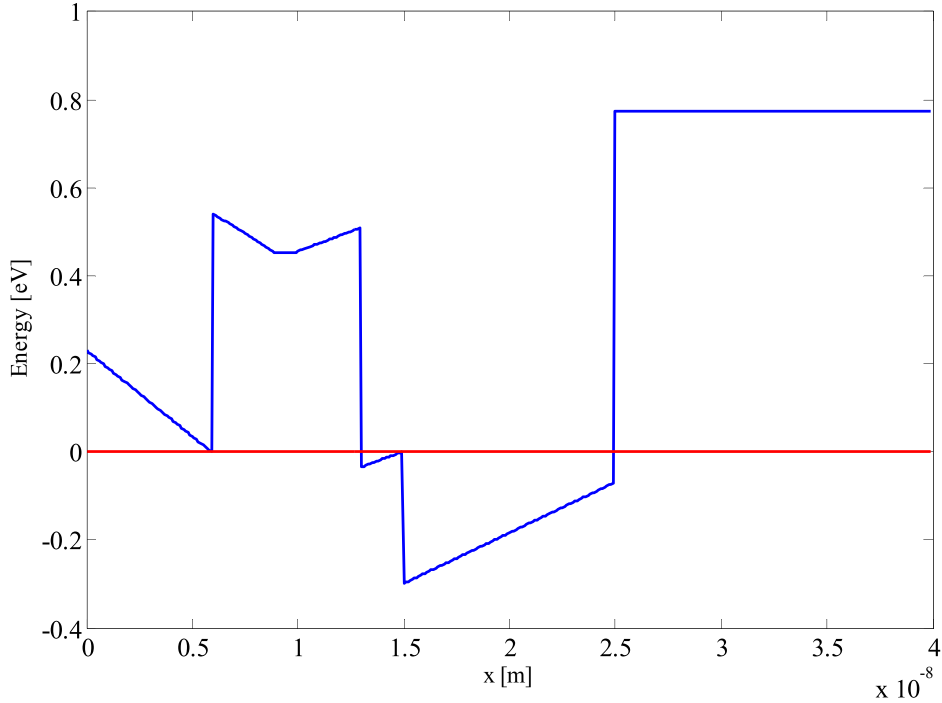


Fig. 3.1: The band profile generated after the first iteration.

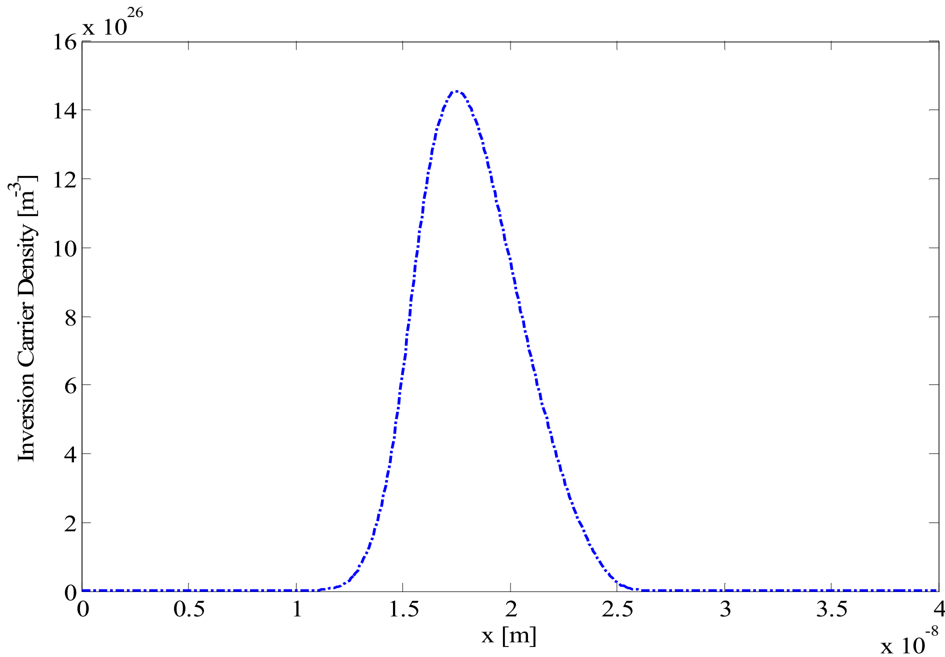


Fig.3.2: The charge density for the band diagram shown in Fig. 3.1.

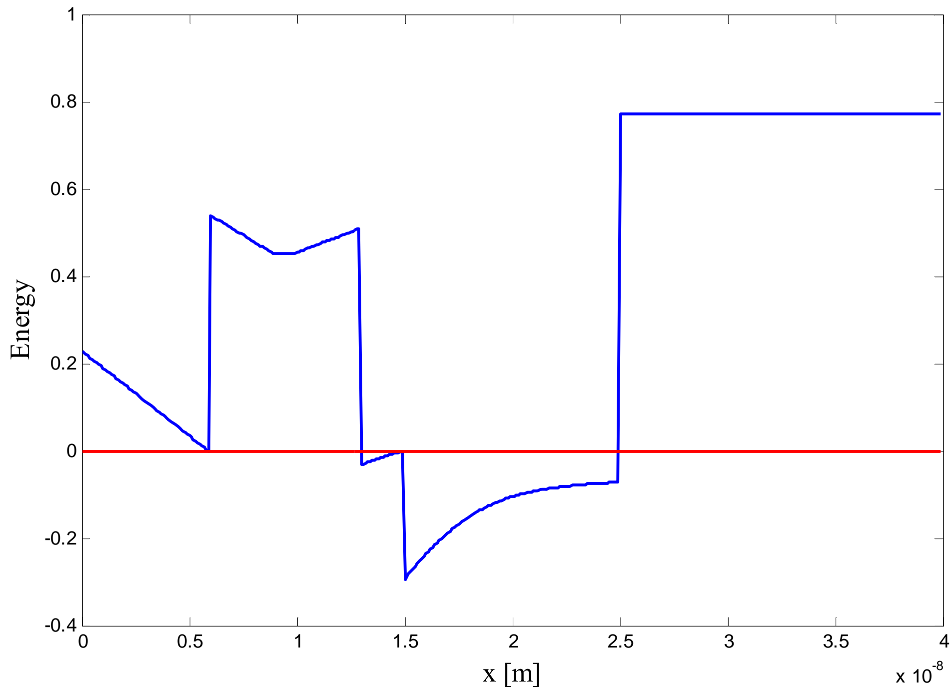


Fig.3.3: The band profile after coupling, bending occurs due to charge accumulation.

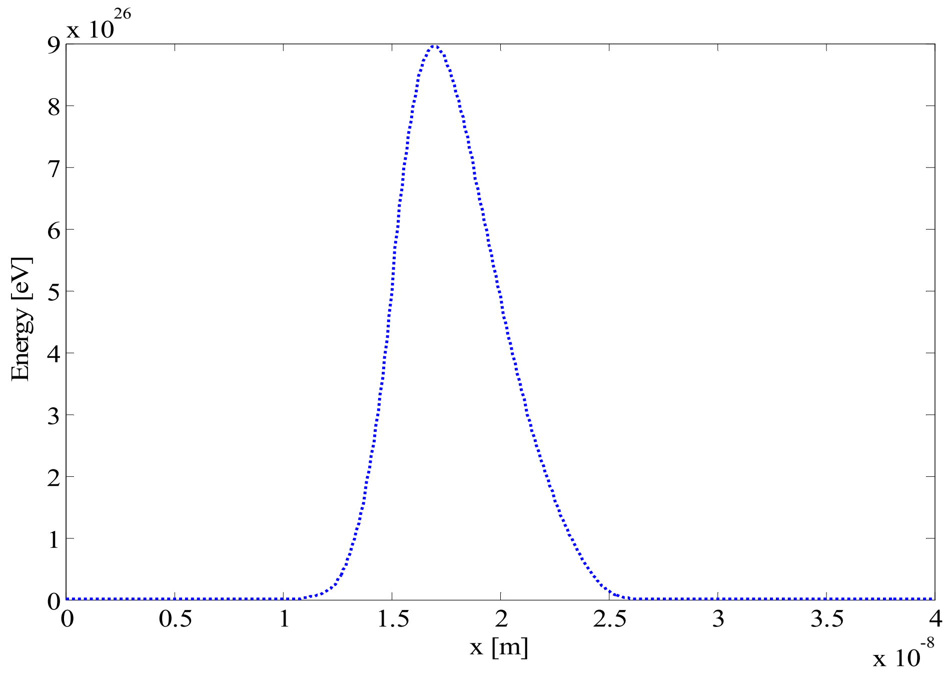


Fig.3.4: The charge density for the band diagram shown in Fig 3.3.

4. CAPACITANCE CALCULATION

Capacitance is calculated by the general formula,

$$C = \frac{Q}{V}$$

Where,

C=capacitance

Q=charge stored

V=voltage applied

From this equation it can be seen that capacitance is the rate of charge stored per unit voltage applied or

$$C = \frac{\partial Q}{\partial V}$$

Assuming charges $Q_1, Q_2 \ldots Q_5$ for varying gate voltage V_G, the first derivative can be expressed as a group of matrices using the central difference approximation as follows,

$$C = \frac{1}{2\Delta V_G}\begin{bmatrix} 0 & 1 & 0 & 0 & 0 \\ -1 & 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 1 \\ 0 & 0 & 0 & -1 & 0 \end{bmatrix}\begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \\ Q_4 \\ Q_5 \end{bmatrix}$$

Hence the capacitance can be calculated from the above expression and will take the form of a column matrix.

5. SELF-CONSISTENT SIMULATION APPROACH

5.1 Lattice construction

First step of the simulation is the construction of a 2-D lattice representing the cross-section of the semiconductor device.

5.2 Hamiltonian generation

After the lattice construction, a Hamiltonian matrix based on the 2-D lattice is produced. The different materials used in the device are accounted for by noting the points they occupy in the 2-D lattice and then multiplying the corresponding points in the Hamiltonian matrix with the relative permittivity of the individual materials. Atomistic discretization was utilized to model the devices precisely.

5.3 Poisson solver

Once the Hamiltonian matrix has been generated, a column matrix [*F*] is created having the same number of points as the lattice. The different material interfaces in the 2-D lattice are traced and the points are noted. The corresponding points of the [*F*] matrix are multiplied by summation of the difference in Fermi-level of the materials and the inverse charge density. After this is completed, the potential profile [*V*] is calculated by multiplying inverse matrix of [*H*] with the [*F*] matrix, i.e $[V] = [H]^{-1}[F]$

5.4 Band-diagram generation

The energy band profile of the semiconductor device is generated by adding the electron affinity values (χ) of the different materials to the potential profile or [*V*] matrix.

5.5 Schrödinger solver

The energy band profile is used in solving the Schrödinger equation to obtain the charge density. The first steps in solving the Schrödinger equation are similar to the Poisson solution, a 2-D lattice is created and a corresponding Hamiltonian matrix [*H*] is formed. The matrix is multiplied by a constant $t = \frac{\hbar}{2m^{*}\Delta x^{2}}$ and solved for the Eigen values and Eigenvectors.

5.6 Charge density

The Eigen values and Eigen vectors obtained by solving the Schrödinger equation are essentially the different energy levels (*E*) and wave function values (Ψ) of the electrons. These

are used in the Fermi-Dirac distribution to calculate the charge density of the semiconductor device using the equation in [2].

5.7 Schrödinger-Poisson coupling

After the Schrodinger equation has been solved for the 2-D lattice, a charge density is obtained which is placed in the [F] to reform the matrix and solve the Poisson's equation again to calculate $[V]$. In short, a loop is created where first a potential profile $[V]$ is generated without solving the Schrödinger equation and then χ values are added to it. The matrix formed is then used to solve the Schrödinger equation and generate Eigen values and Eigen vectors and calculate the charge density. The charge density obtained is then used to recalculate the $[V]$. Similar work involving Schrödinger-Poisson coupling has been done in [16].

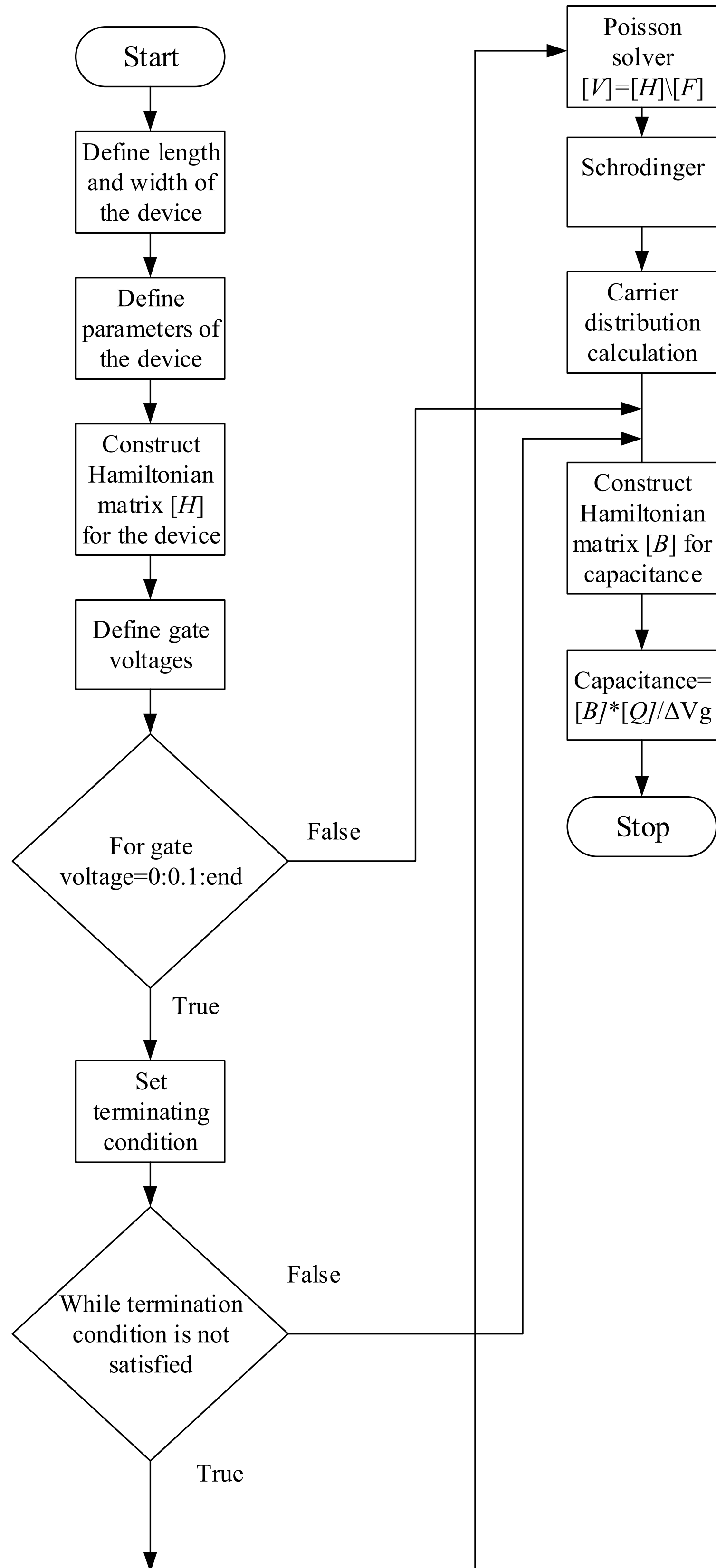
5.8 Variation in gate-voltage

The Schrödinger-Poisson coupled simulation is repeated for a number of varying gate voltages and the resulting charge densities are recorded in a column matrix.

5.9 Capacitance calculation

The capacitance is calculated using the charge densities for varying gate voltages. A matrix $[B]$ is formed which is multiplied to the charge density matrix to calculate the capacitance and then plotted against the gate voltage.

5.10 Flowchart of simulation



6. BENCHMARKING

Before the semiconductor devices were simulated, the simulator was first thoroughly benchmarked to ensure quality simulations. The InGaAs QWFET with an InP spacer layer [3] was simulated, and the C-V graph was obtained. The C-V curve of the simulated device bore a close match to the original C-V curve. Fig.6.2 illustrates the simulated C-V curve and the original C-V curve. The 3-D model of the InGaAs QWFET with InP spacer layer is shown in Fig.6.1.

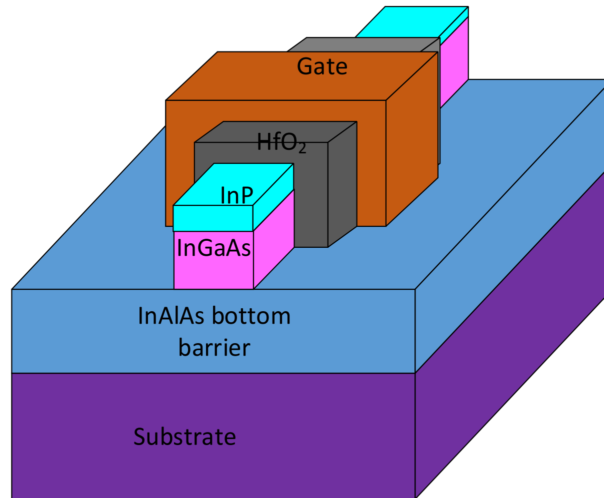


Fig. 6.1: A 3-D model of InGaAs QWFET with InP spacer layer.

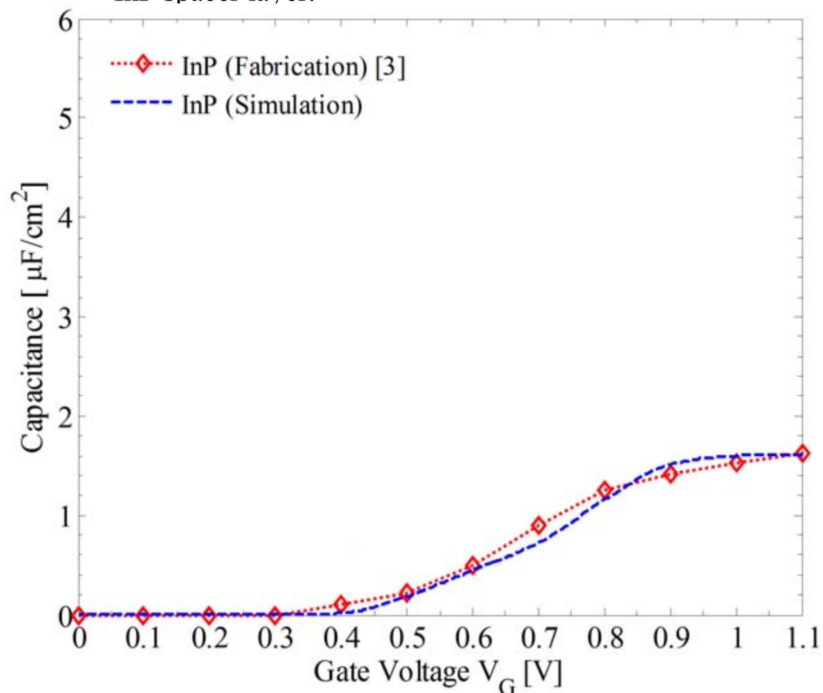


Fig.6.2: The C-V curves of the simulated device and the original

7. 3-D MODEL OF SIMULATED DEVICES

The two devices chosen to be analysed in this paper are of the non-planar type. In the past Si MOSFETs and III-V MOSFETs with non-planar, multi-gate architectures were examined for enhanced electrostatics [4], [5]. III-V QWFETs with non-planar, multi-gate architectures possess better electrostatistics and have higher scalability compared to their planar counterparts [3]. Both the InGaAs QWFET with the InAlAs spacer layer and the InGaAs QWFET with the Si-δ doping layer inside the InAlAs spacer layer take the form of typical non-planar structures as shown in Fig.7.1 and Fig.7.2. The gate surrounds the device on all the sides except the bottom followed by the oxide layer consisting of HfO_2. Next comes the InAlAs layer which acts as the spacer and then the InGaAs layer which forms the channel. The last two layers are comprised of the InAlAs barrier layer and the substrate. The only difference between the two devices is the Si-δ doping layer inside the InAlAs spacer layer present in the second QWFET.

Each layer in the structure has its specific functions. The oxide layer is used to avoid the formation of a Schottky barrier between the metal gate and the semiconductor layer. The InAlAs spacer was chosen specifically because its lattice constant matches that of the channel material which is shown in Table 1. If the channel was directly placed with the oxide layer without the spacer in between there would have been a lattice mismatch which in turn would cause the presence of trap charges in the channel. Hence, the spacer is added to the structure to prevent trap charges from accumulating in the channel and hampering device performance. The Si-δ doped layer is basically a one atom thick sheet of Si atoms. This layer is situated in the InAlAs spacer layer as mentioned above and it aids in greater charge accumulation when the device is turned on [18][19]. The lower InAlAs barrier ensures that the charges accumulated when the device is on is trapped in the channel only and does not move to other regions [8].

Material	Lattice parameter (Å)
InGaAs	5.93
InP	5.87
HFO_2	5.16
Gold	4.07
InAlAs	5.94

Table 1: Lattice parameters of the materials used.

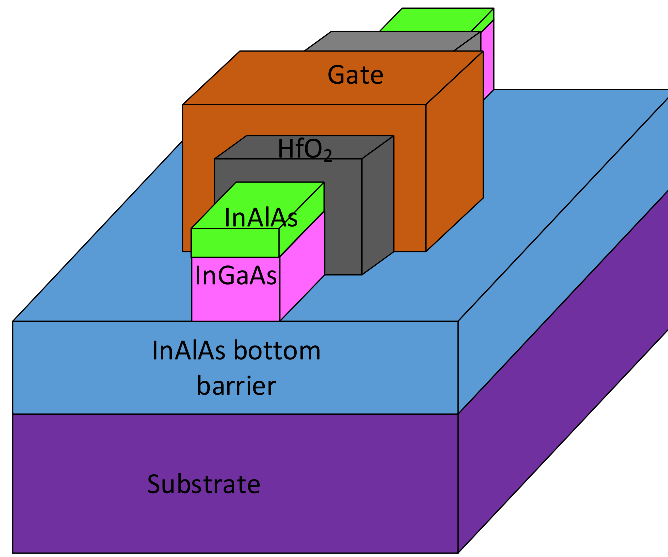


Fig.7.1: A 3-D model of InGaAS QWFET with InAlAs spacer layer.

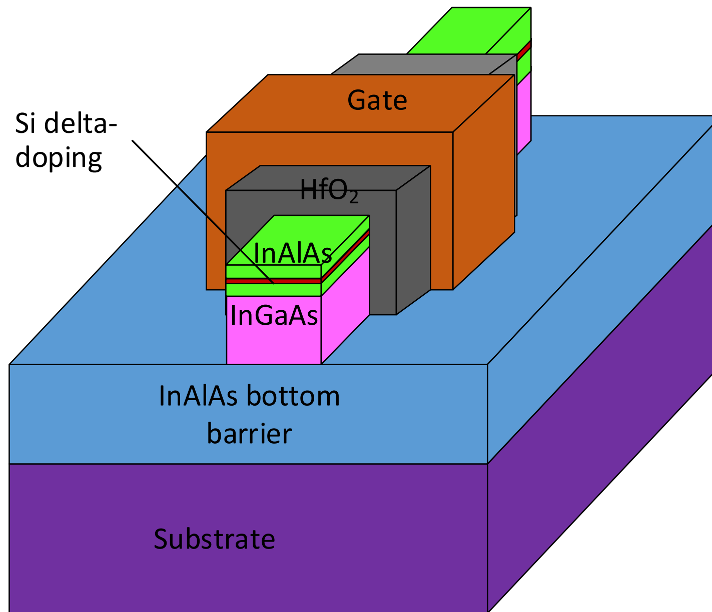


Fig. 7.2: A 3-D model of InGaAs QWFET with Si-δ doping layer inside the InAlAs spacer layer.

8. SIMULATION RESULTS

8.1 Equilibrium 3-D band-diagram

The equilibrium 3-D band-diagram of InGaAs QWFET with InAlAs spacer layer is depicted in Fig.8.1. Here the channel can be seen surrounded by the oxide layer, which in turn is wrapped by the metal gate. The InGaAs channel is below the Fermi-level which indicates the charge accumulated in that region.

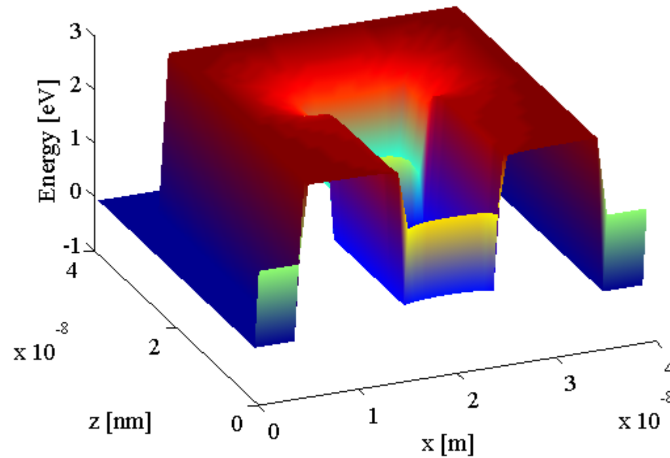


Fig. 8.1: The 3-D equilibrium band diagram of InGaAs QWFET with InAlAs spacer layer.

Fig.8.2 shows the band-diagram of InGaAs QWFET with a doped spacer layer. The Si-δ doping layer can be seen as a sharp dent in the conduction band which is a typical feature of δ doping. The idea behind the InGaAs QWFET with a Si-δ doping layer is to allow electrons in the doping-layer to tunnel into the InGaAs channel from the spacer layer, consequently leading to a greater charge accumulation in the channel.

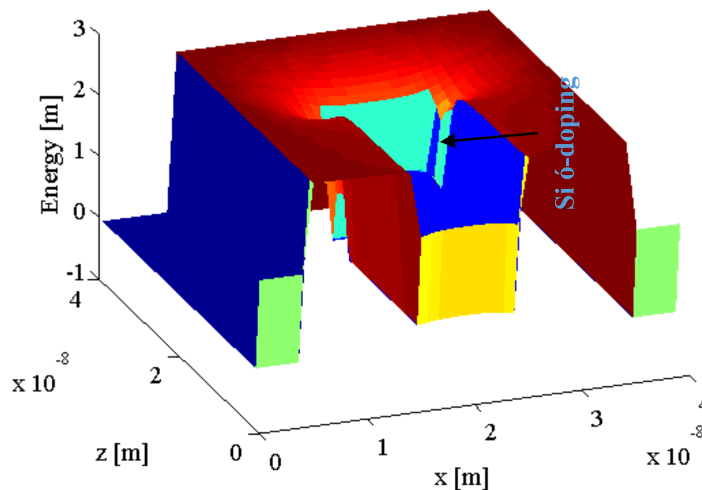


Fig. 8.2: The 3-D equilibrium band diagram of InGaAs QWFET with InAlAs spacer layer containing a thin Si-$\boldsymbol{\delta}$ doping layer.

8.2 Contour plots of band-diagram

The contour plots give a top view of the devices which aids in identifying the different layers precisely. Fig.8.3 is the contour plot of the undoped InGaAs QWFET.

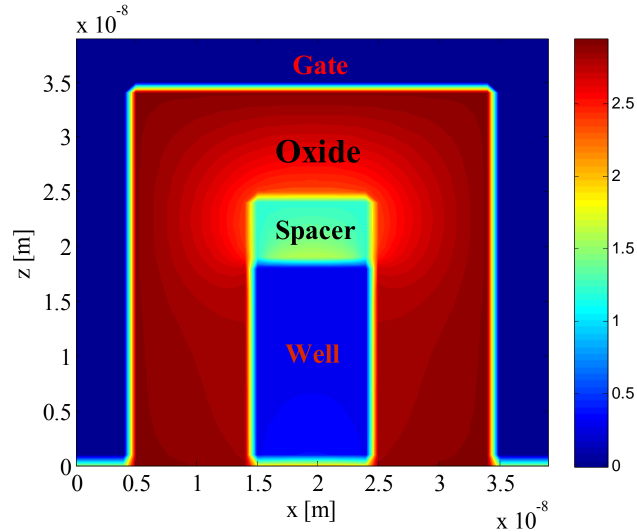


Fig.8.3: Contour plot of QWFET with plain InAlAs spacer layer.

Fig.8.4 shows the contour plot of the Si-δ doped QWFET. From the contour plot, the Si-δ doping layer can be seen to be positioned just above the InGaAs channel making it easier for the electrons to tunnel through the spacer layer into the channel.

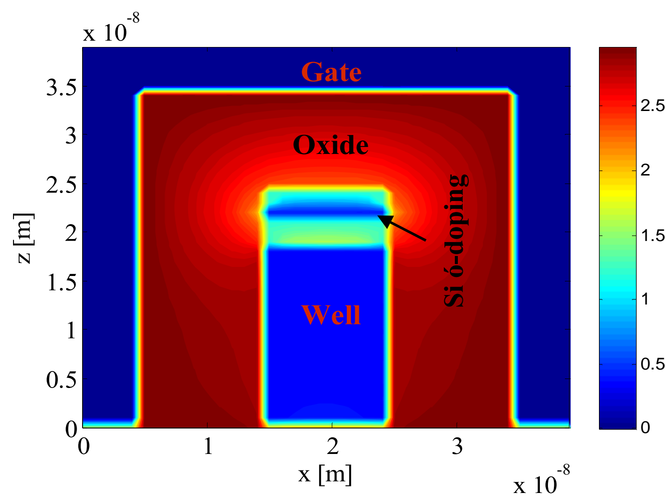


Fig.8.4: Contour plot of QWFET with Si-$\boldsymbol{\delta}$ doping layer inside InAlAs spacer layer.

8.3 Band profiles for varying gate voltages

Band-profiles of the semiconductor devices along the x and z planes are obtained for different gate voltages. As the gate voltage is increased the band- profile is seen to fall further below the Fermi-level in the channel region which is indicative of higher charge accumulation. Fig.8.5 shows the band-profile of the undoped QWFET along the x-axis and Fig.8.6 represents the band profile along the z-axis.

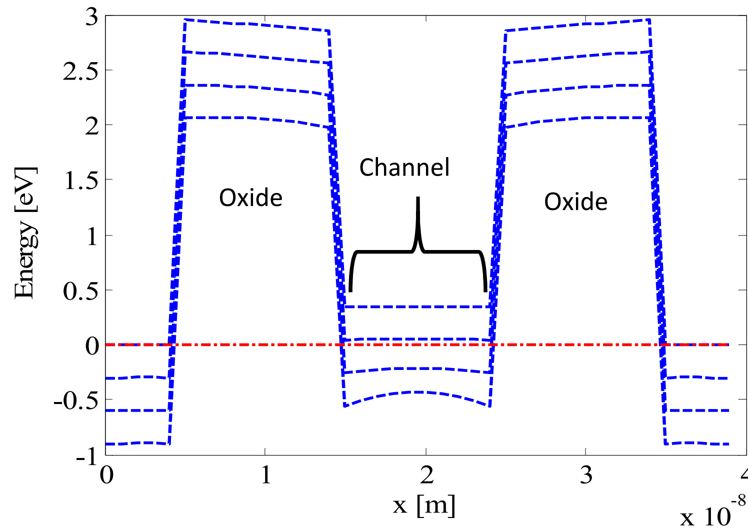


Fig.8.5: Band profile of undoped QWFET along x-axis for V_G= 0V, 0.3V, 0.6 V and 0.9V.

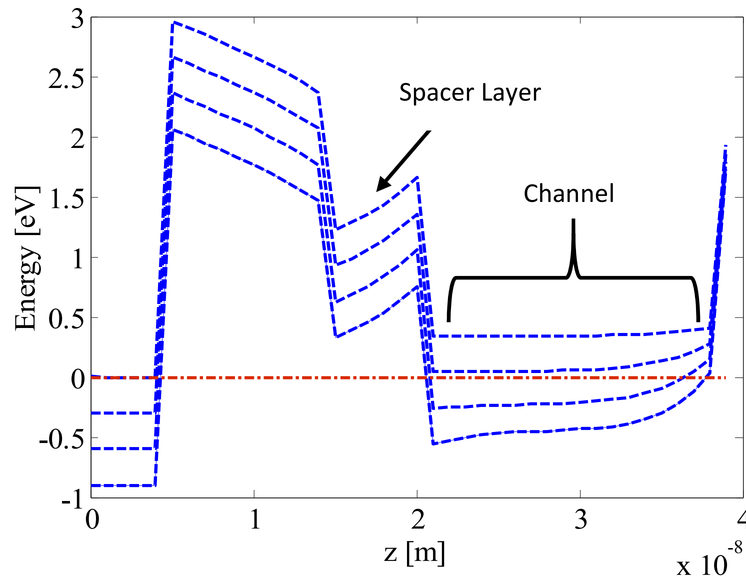


Fig.8.6: Band profile of undoped QWFET along z-axis for V_G = 0V, 0.3V, 0.6 V and 0.9V.

In Fig.8.7 and Fig.8.8 the band profiles of doped QWFET along x-plane and z-plane are depicted. Compared to the undoped QWFET, the Si-δ doped QWFET has more band bending in the channel region, hence it is capable of greater charge accumulation.

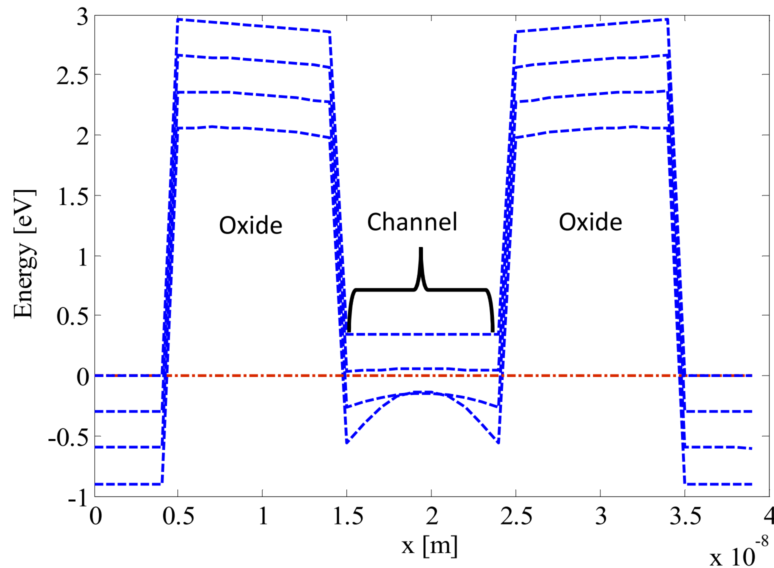


Fig.8.7: Band profile along x-axis for $V_G = 0V$, 0.3V, 0.6 V and 0.9V.

In Fig.8.8 the Si-δ doping layer can be seen adjacent to the channel. As the voltage increases, the doping layer falls further below the Fermi-level leading to larger electron build up in the layer and consequently increasing the probability of more electrons tunnelling into the channel.

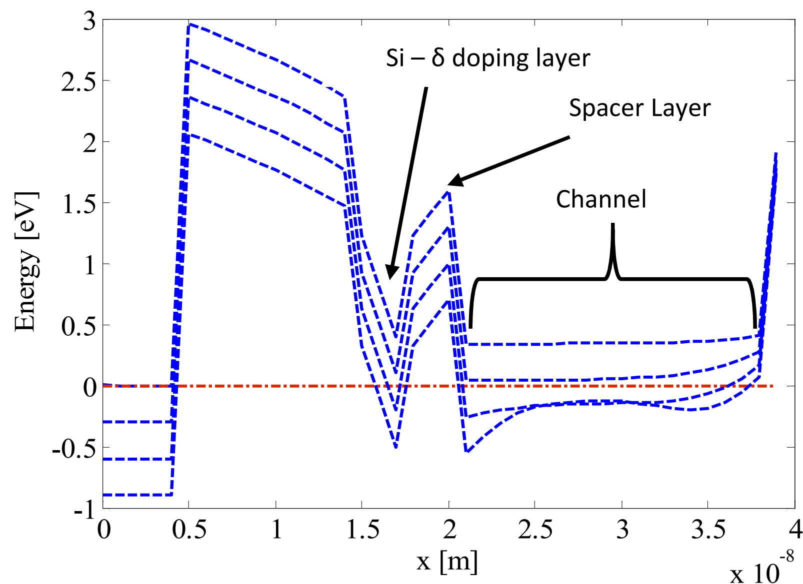


Fig.8.8: Band profile along z-axis for $V_G = 0V$, 0.3V, 0.6 V and 0.9V.

8.4 Charge density plot

The charge density plots in Fig.8.9 and Fig.8.10 (a, b) portray the charge accumulation in the InGaAs channels of the semiconductor devices. Fig.8.9 is the charge density plot of the InGaAs QWFET with undoped spacer-layer and Fig.8.10(a, b) is the charge density plot of the InGaAs QWFET with doped spacer-layer for gate voltage 0.9V and 1.1V.

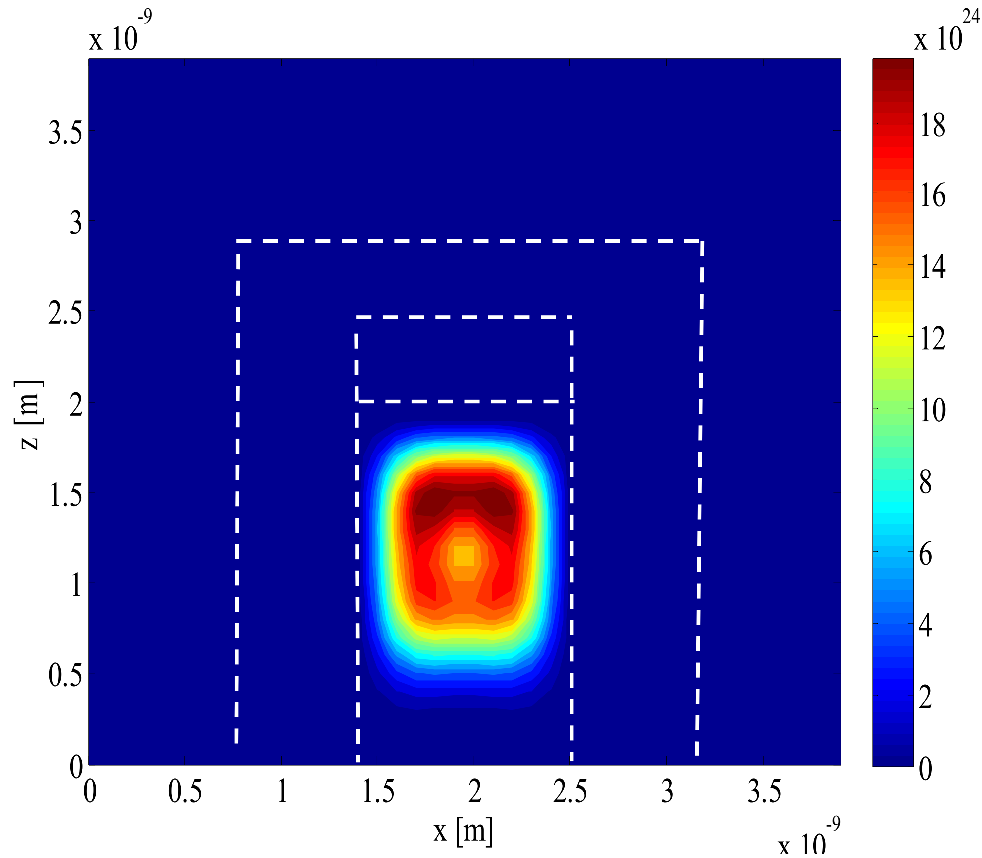


Fig. 8.9: Charge density plot of undoped QWFET.

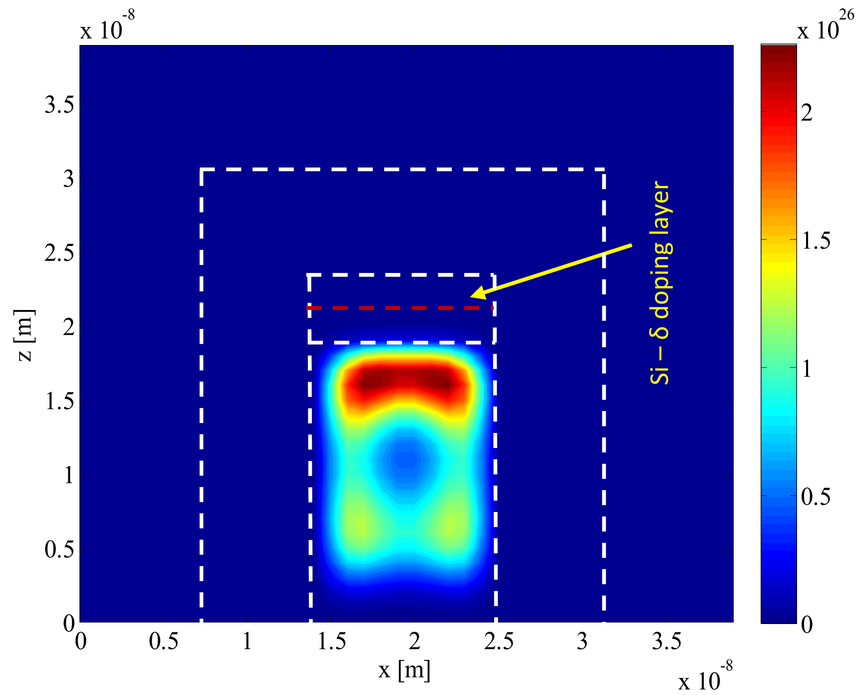


Fig.8.10a: Charge density plot of doped QWFET at V_G=0.9V

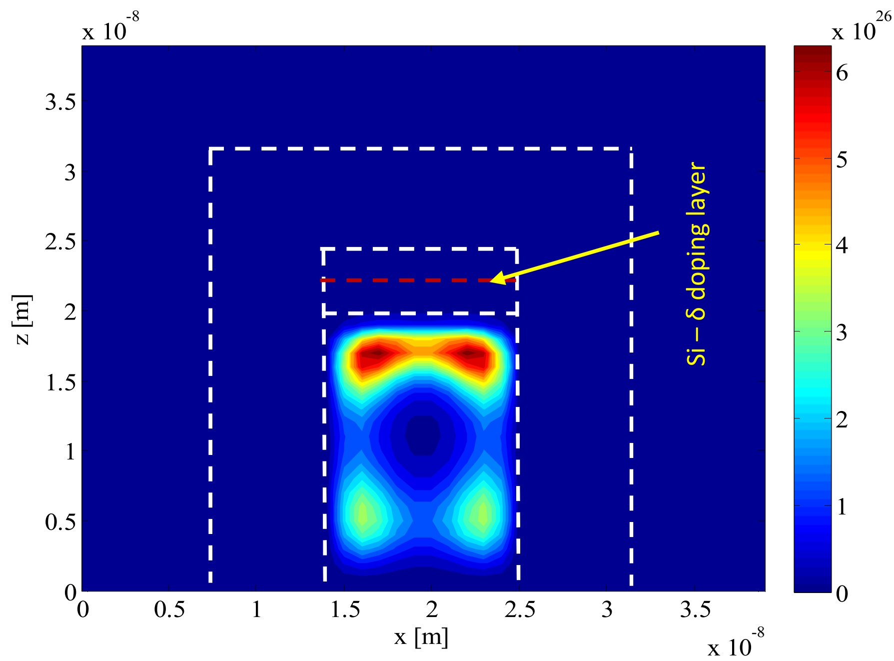


Fig.8.10b: Charge density plot of doped QWFET at V_G=1.1V

8.5 Charge density vs. gate voltage graph

Fig.8.11 and Fig.8.12 show the charge density vs. the gate voltage graphs of the two semiconductor devices. Fig.8.11 is the charge density vs. gate voltage graph of the undoped device and Fig.8.12 represents that of the doped device. By comparing the two graphs, it can be seen that for the same gate voltages, the Si-doped QWFET has a much higher charge density than that of the undoped QWFET.

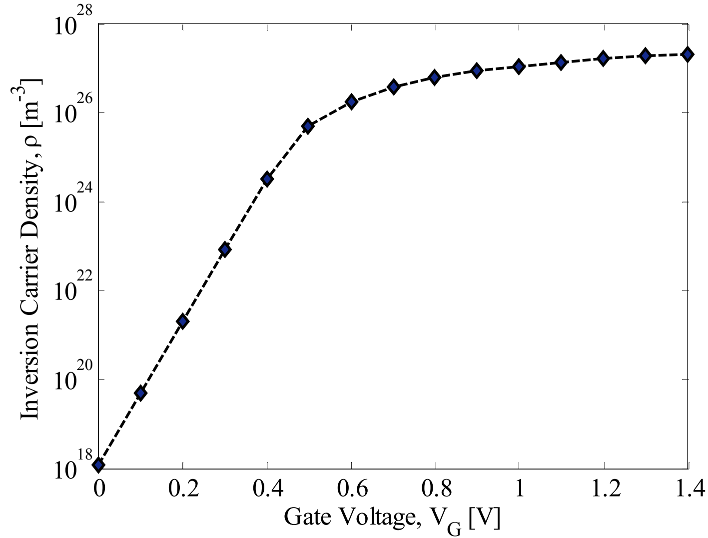


Fig.8.11: Charge density vs. gate voltage graph of undoped QWFET

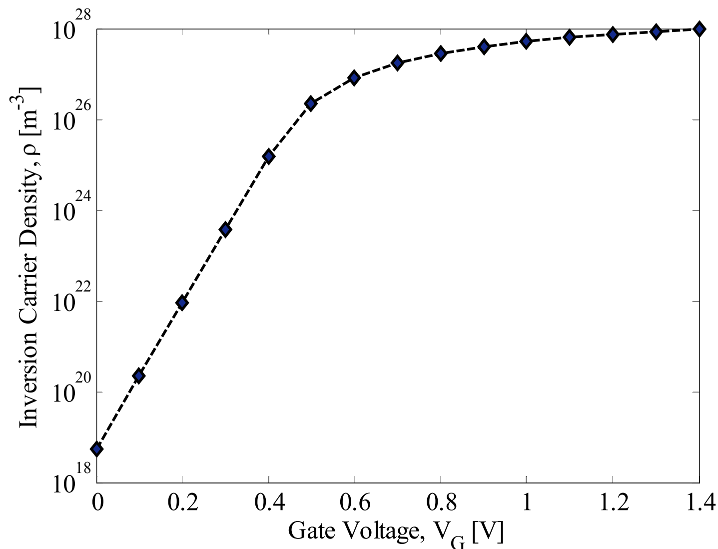


Fig.8.12: Charge density vs. gate voltage graph of doped QWFET

8.6 Capacitance vs. gate voltage curve

The capacitance vs. gate voltage graphs of the two QWFETs are shown in Fig.8.13 .The capacitance curve of the InGaAs QWFET with InAlAs spacer layer is similar to the original QWFET with InP spacer layer [3] as shown in Fig.8.13. The capacitance curve of the InGaAs QWFET with Si-δ doping layer is also shown. From the graph it can be seen that the Si-δ doped QWFET has a lower threshold voltage (0.2V) compared to threshold voltage of undoped QWFET which is 0.3V. Moreover, Si-δ doped QWFET has an improved C-V characteristics compared to the undoped QWFET. This means it has better current drive and is faster than the undoped QWFET.

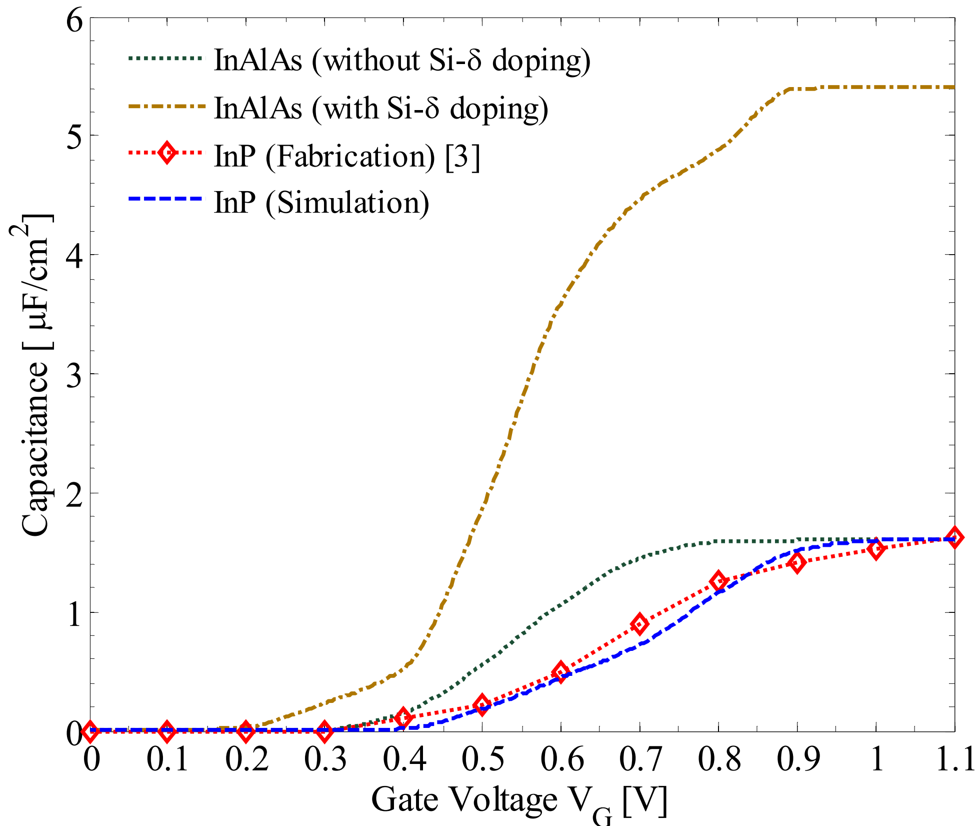


Fig.8.13: C-V curves of the four different QWFETs. The Si-δ doped QWFET has the greatest capacitance.

9. CONCLUSION

In this paper, a 2-D Schrodinger-Poisson coupled simulator was developed. The simulator was benchmarked by simulating an InGaAs QWFET with InP spacer layer and comparing the C-V curves. The C-V curve obtained after simulation was almost identical to the original C-V curve of the device. Next, two QWFET devices were simulated. The first one was an InGaAs QWFET with an InAlAs spacer layer and the second was an InGaAs QWFET with a Si-δ doping layer inside the InAlAs spacer layer. These types of non-planar structures have shown improvements in performance, scalability and gate control and hence, have been the topic of various research over the past decades.

From the simulation results it was seen that the QWFET with the Si-δ doping layer in the InAlAs spacer layer has better charge accumulation. Moreover, the QWFET with the Si-δ doping layer exhibits a larger capacitance. Both QWFETS, with and without the Si-δ doping layer in the InAlAs spacer layer, has low threshold voltage. The InGaAs QWFET with only the InAlAs spacer layer has similar characteristics to the InGaAs QWFET with InP spacer layer.

One negative aspect of the QWFET with Si-δ doping layer was the fact that there was too much power consumption when the device was on. As a result, the device cannot be used for low power applications. However on the positive side, the QWFET with Si-δ doping layer in the InAlAs spacer layer showed greater charge density and higher capacitance compared to the InGaAs QWFETs with the InP and InAlAs spacer layers making it faster and ideal for lower scaled voltage logic applications.

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