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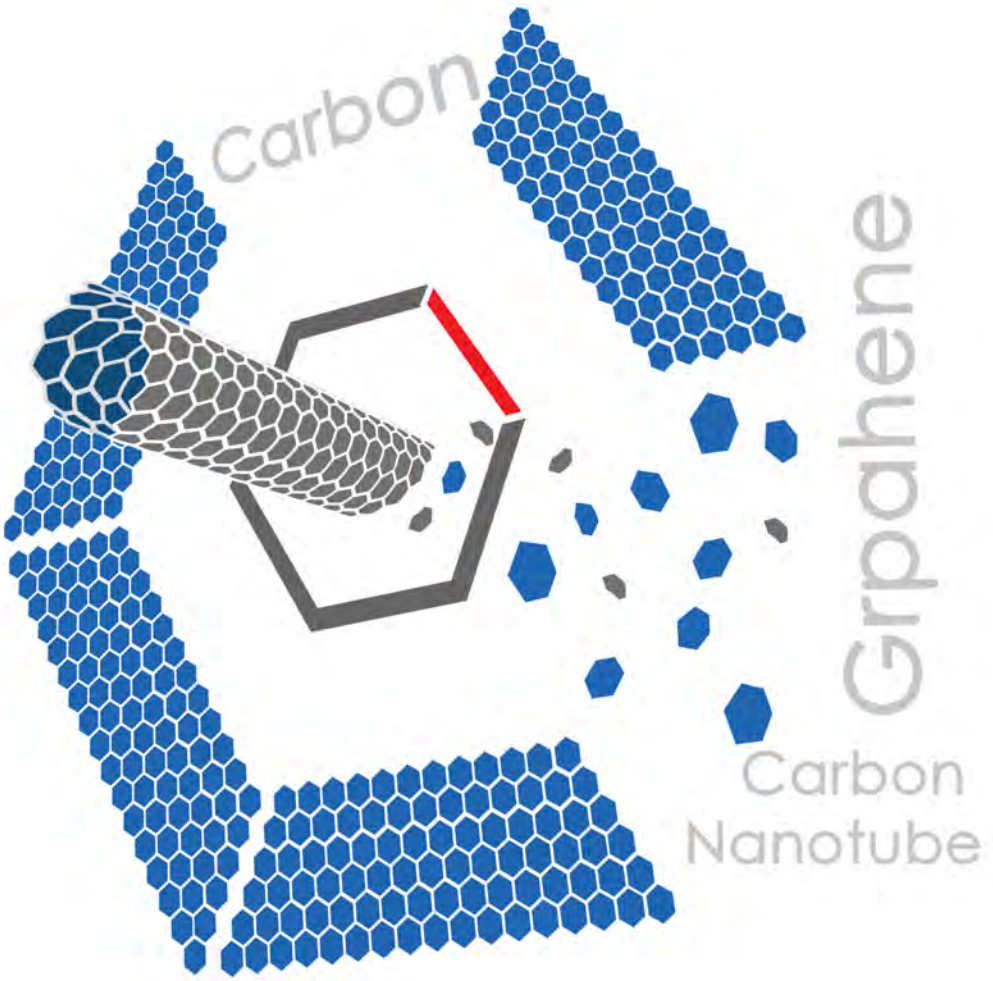

Prospects of Graphene and Carbon Nanotube For Nanoscale Interconnects

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Department of Electrical and Electronic Engineering
BRAC UNIVERSITY
Dhaka, Bangladesh 2017

Undergraduate thesis 2017

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Cover: Md Shifat Uddin

Printed by: Ananna Stationary
Mohakhali, Dhaka 2017

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Abstract

Interconnects are the channels that provide power and carry signals between various components on an integrated circuit. As technology is shrinking to nano scale the thickness of the interconnect wire is also decreasing. Currently, copper (Cu) is being used as interconnect material but with the scaling in nanometer regime, it exhibits much difficulties in terms of IC performance and reliability. Which is the bottleneck for improving IC performance in future. When the thickness of the copper wire reduces to $41nm$ its resistivity becomes approximately 1.5 times of the bulk resistivity[56]. When this thickness is $10nm$ the resistivity is infinite. Not only this to keep pace with the current technology node of interconnets a large amount of current has to flow within a very thick wire. for this reason the wire has to withstand with a high current density. But copper at nanometer range only sustain in $10^6 A/cm^2$[81] of current densities with some structural defects. Also in this current density copper wire exhibits very high joule heating consequently degrades the IC's performance. Progressively high curent density leads to electromigration faliure which degrades wire life time. As a result IC lose its longevity. To tackle this challenges and difficulties faced by copper wires it is high time to think of another material which can be used as interconnect for future devices. The new material have to have sustainability in nanoscale with higher breakdown current density, Elecromigration antagonist and joule heating preventive which leads to high performance IC's. Also the new material need to be reliable which makes the interconnect lifetime higher. In this paper we are proposing two new material named graphene and carbon nanotube(CNT) which can be the effective replacement of copper. Graphene and CNT can be implemented in nanoscale interonnects for their magical characteristics. Both of this material have nanoscale physical configuaration. Graphene has low resistivity ($1u\Omega cm$)[72] is even lower compared to other good conductor like silver ($1.5u\Omega cm$). Not only this CNT's and Graphene can withstand current densities up to $10^9 A/cm^2$[81] which make them electromigration antagonist. But The only challenge for graphene is schottkey barrier it creates at the junction of the metal and semiconductor which causes a barrier height for electron to pass through. Another compound mixing where the barrier height is less can solve the problem of graphene. If this issue is resolved, we may then directly use Graphene and CNT for nano scale interconnects. This paper extensively illustrates why Graphene and CNT can be the best alternative for replacing copper. In the beginning of the paper different kinds of interconnect has been described. Later that the paper delivers a comprehensive review of the previous, existing materials used for interconnects

and then described the new materials for interconnects. The paper also elaborates the major limitations of copper in nanoscale interconnects and then successfully delineate the major advantages we may get from graphene and carbon nanotube as interconnect material. After that the production route of graphene has been described. In this dissertation we tried to establish the major issues of copper and the best alternative for that. Further study is needed for the capping material of graphene which will increase the lifetime of the interconnect.

Keywords: interconnects; Graphene; carbon nanotube; RC delay; electromigration; integrated circuit

Acknowledgements

To our life-coach,our parents: because we owe it all to you. Many Thanks!
We are grateful to our siblings who have provided us through moral and emotional support in our life. We are also grateful to our other family members and friends who have supported us along the way.
A great gratitude to our thesis supervisor Anamul Haque for paving the way to research on this topic
And finally, last but by no means least, also to everyone in the impact hub... it was great sharing laboratory with all of you during last four years.
Thanks for all your encouragement!
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MD.Shakhawat Hossain Rayhan, MD. Shifat Uddin, Jannatul Tazrin Biva, MD. Shafiqul Huda. December 2017

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1

Introduction

The world is connected in each and every way as possible, making the tasks easier for everyone. Starting from the computer we use, the phones we call to connect to others, and the printers we need to print out documents, each and everything are electronics. These electronics are the main reason we can take faster decisions, but what are these electronics? Firstly, electronics are those which consists of using transistors, microchips and other components on a circuit board. After the invention of the transistor in 1960 at Bell laboratory we have entered a new era of modern technology. When the world has got its first integrated circuit it has only five transistors. After that, the number of transistors in an IC increased with time. Gordon Moore, the founder of Intel described this number will double in every two years in a paper in 1965. Today even in a small IC holds more than one billion transistors integrated on it. In order to connect those transistors metal lines are used which are called interconnect. It is a thin film of conducting material that provides electrical connection between transistors on a silicon chip. In the early days Aluminum (Al) were used on this purpose as it is one of the abundant material. Unfortunately due to higher electro-migration in Al, Copper (Cu) supplants Al in 1997. Use of Cu as interconnect material for better performance and low heat dissipation were first introduced by IBM with assistance from Motorola. Nowadays $65 - 45nm$ wide interconnect is being used. As scientists want to accommodate more and more transistors on same small substrate interconnect lines also shrinking. With the shrink of interconnects Cu is facing difficulties such as increased resistivity, electro-migration. Also in nano-scale Copper interconnects cannot survive with a high current density more than $10^6 A/cm^2$[81] . To survive with the need a new material for interconnects is required. Graphene and Carbon nano-tube(CNT) shows such characteristics which can be the potential candidate for future interconnects. Graphene being a material can allow large carrier mobility and thermal conductivity, coupled with a small material volume, emerges as a viable alternative to copper interconnects in electronic circuits. With unprecedented carrier mobilities, the most natural applications for graphene would be in the interconnects region. This however in the experimental realization of lower resistivity in graphene tool some time to achieve, and it is only recent that graphene is being seriously considered as an alternative replacement to copper. Carbon nano tube is also another material which can replace copper in the interconnects region. Carbon nano tube can be considered being a semiconducting material or metallic. Metallic carbon nano tubes has been identified as being another alternative of replacing copper in the interconnects region. There are obviously a few short comings regarding graphene where it creates a barrier called “Schottky Barrier” in between the silicon and graphene. Carbon nano tube

also has a problem, which can be solved resulting a break though of the entire electronics industry providing faster, compact and efficient electronics.

1.1 Scope of the Thesis

The scope of this thesis is to analyze the characteristics of Graphene and CNT as well as describe their potentiality for future interconnects. Copper has several limitations when its dimension shrinks below 40nm. Reducing the dimensions leads to narrower lines and smaller spaces between lines. As a result the resistivity of Copper and capacitance increase which causes RC delay. When the resistance increases more heat is produced. Besides that, the lifetime of the Copper interconnects reduces due to electro-migration. As well as grain boundary scattering and electron phonon interaction effects the flow of electron in Copper. Regarding all this limitations implement of new material is needed. On this thesis Graphene and Carbon nano-tube has been studied thoroughly. It has been found that Graphene has higher mean free path than Copper. As a result it has less electron scattering and better electron mobility. Also the band structure and schottky barrier of Graphene with other material has been studied.
This thesis also illustrates the single walled and multi-walled CNTs after that current densities of CNT and comparision with Copper. Carbon Nanotubes have decreased resistance, increased thermal conductivity and antagonism to electromigration which make them consummate candidate for interconnects.
In the later part the production route of Graphene has been described. The main challenges with Graphene production is large area fabrication. If we overcome these limitations Graphene and CNT will revolutionize the semiconductor industry.

2

What are Interconnects

Interconnects are the connections in the Integrated circuit used to connect transistors locally and globally throughout the device. The devices performance largely depends on interconnection. In order to create the next generation interconnect we have to solve some significant drawbacks like RC delay, power consumption and cross talk.

2.1 Interconnect

The history of Interconnects began as soon as the integrated circuit was invented in 1949 by German engineer Werner Jacob when he put five semiconductor devices on a single substrate. From then more and more devices began to add on the small substrate and until now it follows Moore's Law of doubling the number of transistor every year. However, the size of interconnects also shrinks with the time. Today 1um to 0.25um wide interconnects is being used and some time even smaller up to 10um which puts the limits of currently used material. The role of interconnection or wiring arrangement is to give out clock and other signal transmission. Also to provide power or ground between various circuits system on the chip. These clock and signal functions is distributed among three parts of interconnection which are local, semi-global and global. Depending on interconnects length it can be classified any one of them.

2.1.1 Local interconnect

The lowest means first levels are the local interconnects which consist of very thin lines and used for very short interconnects at the device level. Connecting gates, sources and drains in MOS technology and collectors, bases and emitters in bipolar technology for execution of any unit or useful block like cache memory, embedded logic or address adder on the chip. Normally few gates of first layer are covered by local interconnects but in case of multilevel it spans to second metal layer.[78]Polycrystalline Si is used as local interconnect in MOS technology, also used as the gate electrode material. There is another region acting as local interconnect which is silicided gates and silicided source/drain. [57]Furthermore, by-product from silicided gate process TiN can be used for local interconnect and W is sometimes used as well. TiN is generally discarded but in the gate and junction silicide process the 0.1micrometer layer of TiN is patterned and etched for local interconnect.[86][85]The increasing packing density of devices reduces the wire lengths and the length of a local interconnect is also scaled down with the scaling of technology

nodes. They have higher resistivity for their short distance than global interconnect but they must be resistive to higher processing temperatures. Local interconnect offers less lateral coupling capacitance and driver loading for improved performance. As technology scales down from 22nm to 5nm nodes the interface contact resistance increases. For MIS(metal-insulator-Si) contact the contribution is $14\% - 35\%$and for silicided case is $44\% - 66\%$.[25]

Table 2.1: Scaling of local interconnect

Interconnection Parameter	Scaling Factor(S)
Cross sectional Dimensions (W , L , T)	$1/S$
Inter-electrode capacitance	$1/S$
Resistance per unit length	S
Capacitance per unit length	$1/S$
Line response time	1
Line voltage drop	1
Line current density	S

2.1.2 Intermediate interconnect

For the increasing complexity of modern ICs interconnects a median level, semi-global interconnect is introduced between global and local interconnect. It is used to connect devices within a block. This level distributes clock and signals within a functional block around 3-4nm lengths. Semi-global wires provide lower resistance clock paths or signal. They are wider and taller than local interconnect.[78]

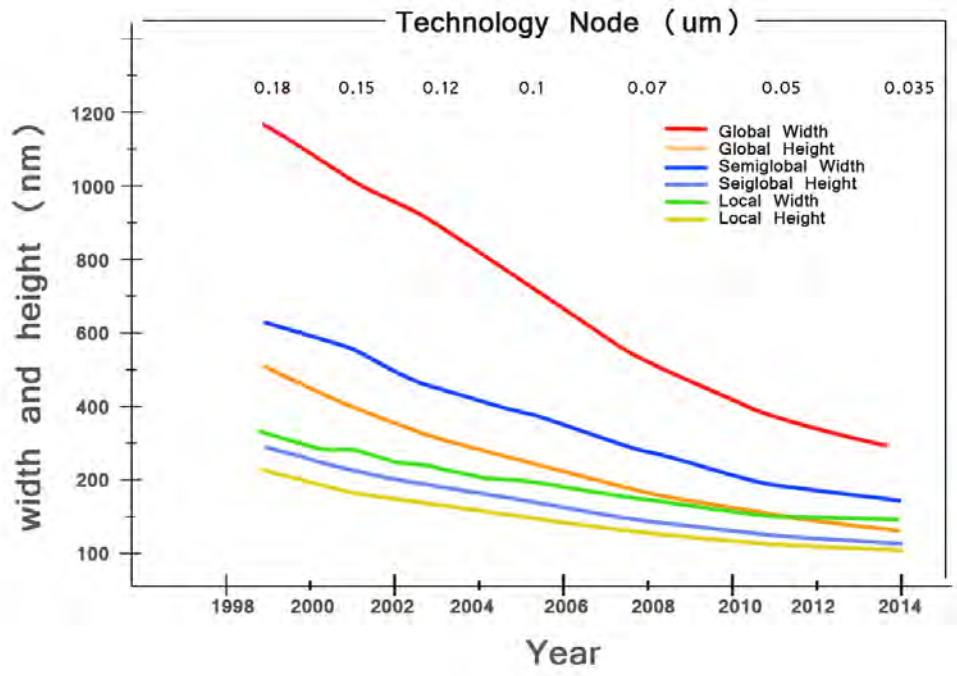


Figure 2.1: decreasing trend of height and width of interconnect

2.1.3 Global interconnect

Connection between the blocks and long interconnects along with power, ground and clocks, global interconnection is used. The top one or two layers with length of 3000um-15000um[45]are global interconnect layers whose length increases with die size proportionally. It can be half of the chip perimeter.[78]At nanometer regimes, if the aspect ratio of wires is approximately 2-2.5 than the RC time constant reduces for width increment and therefore the delay is improved per unit length. It is much wider than other interconnects and mostly made of Al. As a result, the resistance of global interconnect is small. Global interconnects covers long distances between different devices and parts of the circuit. The scaling down decreases the gate delay and local wire delay rapidly but the global interconnects delay increases. This delay can be reduced by the insertion of repeater.[66]

Table 2.2: Scaling of global interconnect

Interconnection Parameter	Scaling Factor(S)
Long distance interconnection Dimensions (W , L , T)	$1/S$
Long distance interconnection Dimensions L_max	S_C
Inter-electrode capacitance	S_C
Resistance per unit length	S^2S_C
Capacitance per unit length	S_C
Line response time	$S^2S_C^2$
Line voltage drop	SS_C
Line current density	S

2.2 Challanges of interconnects

Interconnection creates RC delay which slows down the device during high speed operation. This RC delay occurs due to interconnect resistivity and parasitic capacitance between interconnect separated by dielectric material. The resistance (R) and capacitance (C) depends on length(L), height(T) and width(W) of the interconnect.

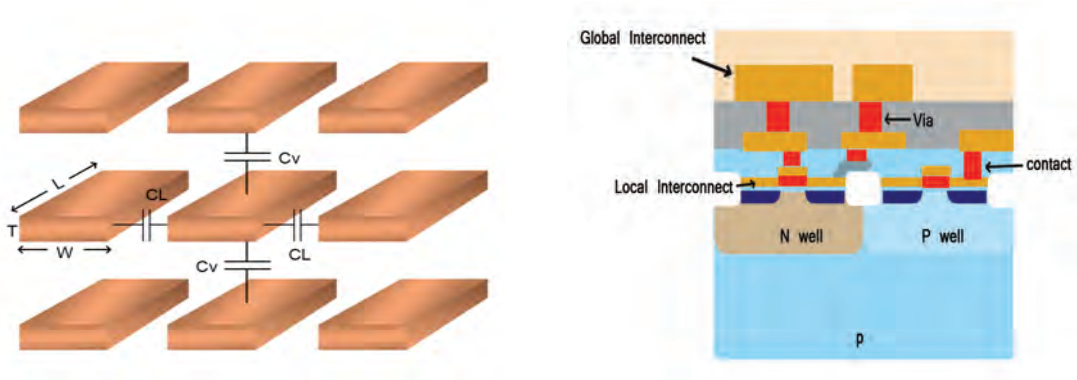
$$R = \rho\frac{L}{WT}$$

$$C = k\epsilon_o\frac{A}{d}$$

Here k is dielectric constant, ϵ_o is the permitivity of air, A and d is area and distance of interconnect surface.

$$C_L = k\epsilon_O\frac{LT}{W}$$

$$C_V = k\epsilon_O\frac{LW}{T}$$



(a) Parasitic capacitance in interconnects **(b)** Interconnect Levels in IC

Figure 2.2: Interconnect

$$V_{out} = V_{in}\Big(1 - exp(-\frac{t}{RC})\Big)$$

Another challenge is to reduce capacitive coupling among the interconnection where signal carrying wire tends to induce the signal to it's the neighboring interconnects (figure 2.3). This also known as crosstalk and it also depends on capacitance between interconnect. Advancement of DSM technology has affected the crosstalk noise problem as the feature size reduces. As a result, unwanted coupling voltage appears in between two adjacent wires. With the advancement of technology the metal layers increment, the density of integration, narrower spaces between lines and increment of line thickness all of these factors have great impact on crosstalk problems. Inter-wire capacitance becomes dominating factor when multilayers interconnects are introduced as they are away from the substrate. Crosstalk is a result from that and causes noises interference from neighboring signal wire. Noise is the unwanted signal which is proportional to signal swing and depends on the transient value of neighboring signal. At high frequencies crosstalk induces glitch when the victim line is static position and causes delay during the signal transition when noise is injected from aggressor line. This delay causes system failure but these effects can be minimized. However, this can be costly to redesign the whole circuit.[78]

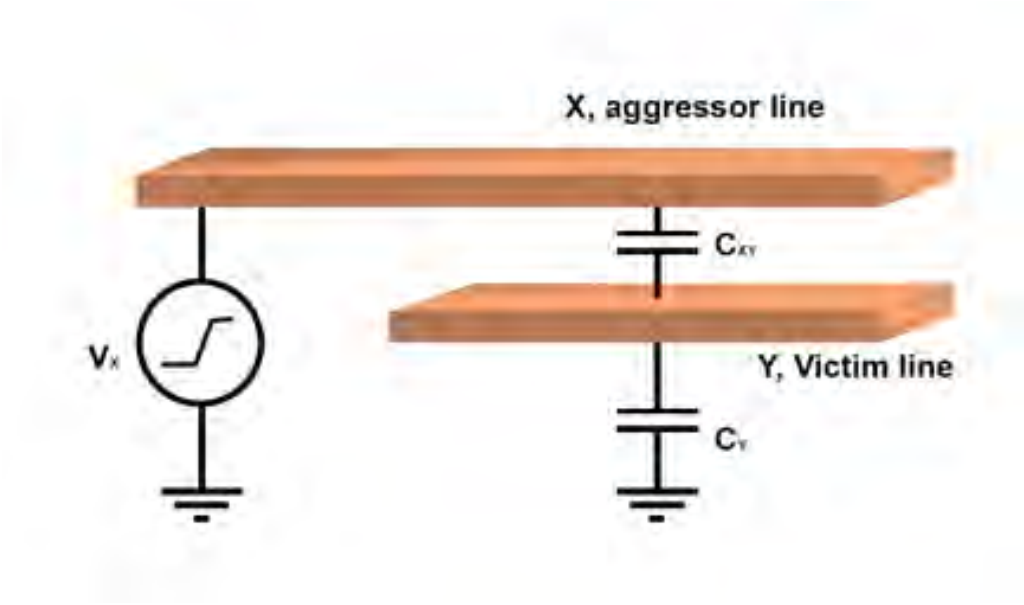


Figure 2.3: Cross Talk within interconnect

$$\Delta V_y = \frac{C_{xy}}{(C_x + C_y)} \Delta V_x$$

At higher frequencies the non-uniform current density increases and current flows near the interconnect surface which is called skin effect. The interconnect resistance is increased as the cross sectional area is reduced. The current density normally drops to 1/e at skin depth which is below the conductor surface and determined by

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}$$

Where μ is the conductor permeability. The resistance equation is mainly for DC resistance and it does not remain accurate if delta becomes smaller than the wire cross sectional dimension. With the frequency increment the skin depth decreases slowly. This non-ideal effects consideration totally depends upon circuits operating and modelling accuracy. For Cu line the skin depth is 2um and for Al is 2.8um at 1GHz. This effects the wider lines most than narrower lines but it totally depends on the geometry and surrounding metals. [19][16]
On the other hand this capacitance also significantly increase power consumption of the device. With the scaled devices, due to the interconnect capacitance the dynamic power can be much higher than total dynamic power by 50%. There are three sources of power consumption in CMOS Gates. Firstly, the switching power results from the fill swing charging and discharging nodes, P_{sw}

$$P_{sw} = \alpha f_{clk} C V_{dd}^2$$

Here α, f_{clk} and V_{dd} is the switching activity of node, the clock frequency and supply voltage respectively. The second one is caused by the input signals rise and fall time

which results into short circuit power,P_{sc}. At that time, both NMOS and CMOS are turned on for a short period of time causing shorts between V_{dd}.

$$P_{sc} = \frac{\beta}{12}(V_{dd} - 2V_T)^3 \frac{\tau}{T}$$

Here β, τ, and T is the transistor gain factor, signal rise and signal period respectively. Thirdly, the most important is the leakage power, P_{leak}. It is found in sub-threshold leakage, reverse biased diode junction leakage and gate leakage. The power dissipation has increased dramatically with on-chip integration levels and for higher frequencies. The dynamic power consumption consists of P_{sw} and P_{sc} is increased at higher frequencies. For reducing it V_{dd} is scaled down which ultimately reduces the channel gate control ability. All of these leads to increase huge amount of P_{leak} because the V_T and gate insulator thickness also need to be reduced. So, the portable applications battery life and budget for complex and large VLSI circuits is threatened and it concludes that the V_{dd} and V_T cannot be scaled same as device geometric rate while keeping the maximum transistor driver current.[19][79]So it is clear that we need to reduce the resistance R and capacitance C of the interconnect layer to get better performance.

3

Literature Review

This chapter extensively illustrates the materials which are currently using and used in the past for interconnects as well as some potential new materials. Also detail review of the materials which can outperform the currently using interconnects materials will be discussed with there properties extensively.

3.1 Aluminum

First of all, we all do know the element Aluminum. We see aluminum products like the window frames, expensive sports car bodies, airplane bodies, etc. Is that even available just as a metal in nature? Well, that is not the case over here. Aluminum is found as an ore named bauxite,[28] a combination of a lot of elements. Aluminum lies on the 3rd group of the periodic table consisting of 13 protons and electrons in equal number, and a mass number of 26.981 27. Electrons are arranged as $2, 8, 3$ in aluminum.[28] It has 3 electrons on the outer most shell, thus lies on the 3rd group. It is one of the most abundant material of the crust, and it makes about 8% of the Earth's core.[28] The diagram of the nuclear composition and electron configuration of an atom of aluminum-27(Atomic number 13), the most common isotope of this element. The nucleus consists of 13 protons(red) and 14 neutrons(blue). The black dots are electrons. It falls in group 3 as it has 3 valance electrons.

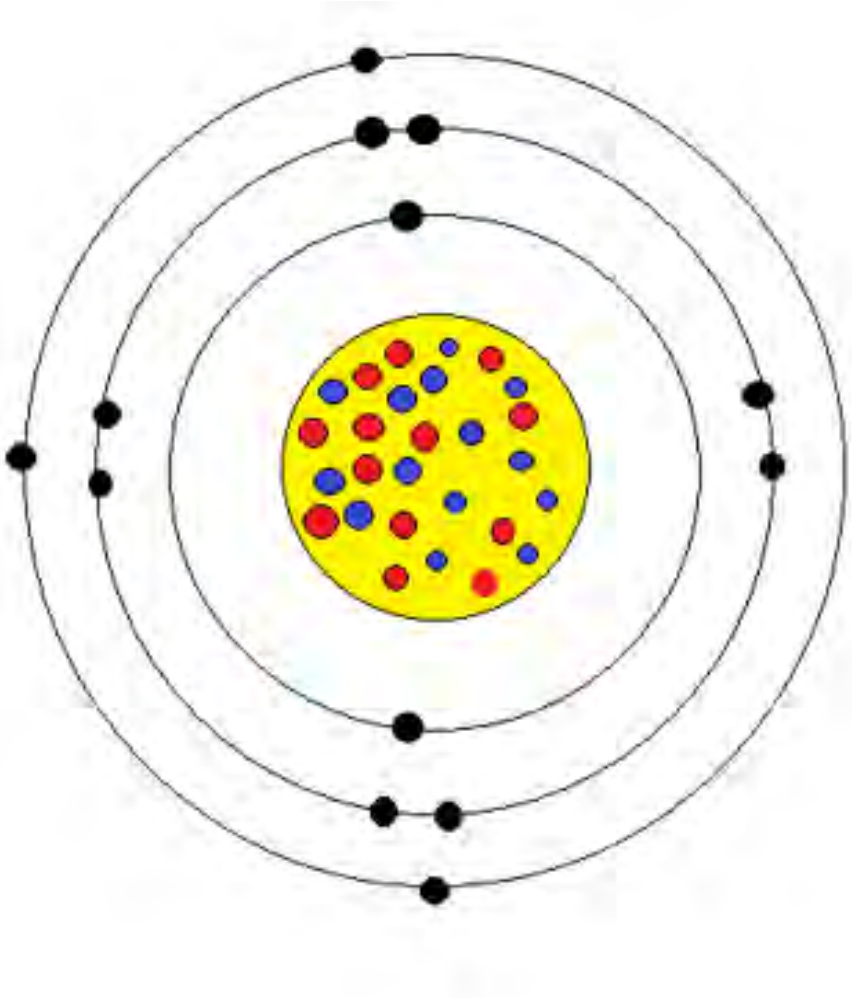


Figure 3.1: Aluminum Electron Structure

Table 3.1: Properties of Aluminum

Melting point	$933.47K$
Boiling Point	$2743K$
Density	$2.70g/cm^3$
Crystal Structure	Face centered cubic
Magnetic ordering	Paramagnetic

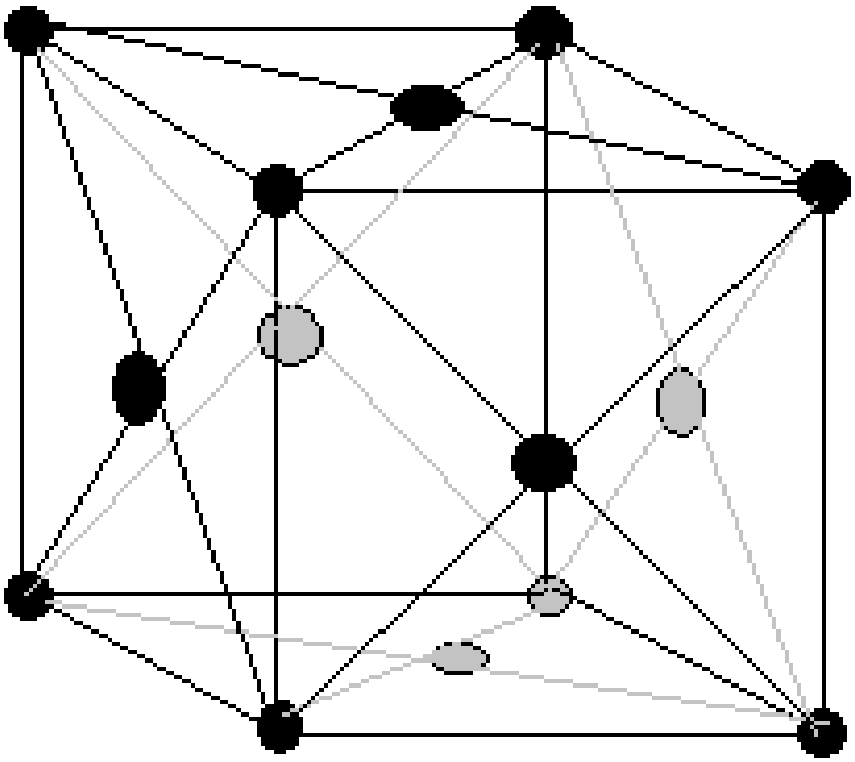


Figure 3.2: Structure of Aluminum - Face Centered Cubic

3.1.1 Mechanical Properties

Obviously, aluminium is a metal and it loves to donate electrons. Thus, giving us the advantage to use that as a metal conductor and heat conductor. The reason that aluminium is found as an impure form or rather called ore, is due to the fact that it is readily reactive. Pure aluminium is silvery grey metallic solid(relatively soft), light weight, durable and a malleable metal. It does not ignite and it is non-magnetic.[28] The uses of aluminium is huge in quantity. It is the second material after iron to be used this vastly. It is used for both mechanical and electrical purposes. The reason it is used for mechanical purposes are due to the fact that aluminium has a low density and therefore low weight, huge tensile strength and superior malleability, easy to machining, and an excellent corrosion resistant material. It is also a very good heat and electrical conductor. And to maintain the Earth's "Go Green" dialog, it is very easy to recycle.[40] We do hear a lot that aircrafts and sports cars have aluminium bodies rather than steel bodies. It is due to the fact that aluminium is 1/3 of steel's weight. The less weight does not necessarily mean that aluminium is not durable. Aluminium being light weight does not compromise in strength.

Aluminium alloys relatively has $200MPa - 600MPa$ of yield strength.[28] At lower temperatures, the strength of aluminium increase but as we scale up the temperature the strength increases, that must be taken into account while designing something. Compared to other metals, aluminium has a greater tendency to have a linear expansion. Aluminium is very easy to work with regarding machining. Machining methods include milling, drilling, cutting, punching, bending, etc. Also, the amount of energy required for this are not that much, thus it is much friendly to work with. Aluminium has a superior quality in terms of malleability for extrusion.[74] This eventually means that it can either be rolled into strips or foils, and also bending in either hot or cold conditions. Aluminium is an excellent conductor of both heat and electricity. Having approximately half of the weight of copper but a very good conductor.[28] In terms of joining aluminium, it is quite easy like fusion welding, friction stir welding, bonding and taping. Aluminium is a very good reflector of both visible light and radiated hear. Screening EMC means to block of screen off electromagnetic radiation .The better the conductivity of a specific material the greater the shielding.[74] Aluminium reacts with oxygen in the air to form an oxide layer which helps it to to prevent corrosion. The layer is thin though, but helps in protection. Aluminium is known to be very durable and neutral. Aluminium is a non-magnetic material and it is used in magnetic X-ray machines as it avoids magnetic interference.[74]

3.1.2 Electrical Properties

Obviously aluminium does not only have these sort of normal properties, but it also does play a major role in the electrical department as well. Aluminium is used in cables. Not only in small dimensional wires, rather power cables to be exact. Aluminium foil winding also helps in winding the capacitors from the smallest types used in lightning fittings and to large power capacitors. Foil Windings are also suitable for some transformers, reactors and also solenoids. Foil thickness may range from $0.040mm$ to $1.20mm$ in 34 steps, a better space factor than a wire of copper coil obtains ,the aluminium conductor occupying some 90% of the space as against 60% for copper wire.[74] Heating and cooling are aided by better space factor and smaller amount of insulation needed for foil wound coils. Rapid radial heat transfer ensures an even temperature gradient. Aluminium foils are however almost exclusively used for then HV windings of cast resin insulated transformers as it has a thermal expansion coefficient closer to that or the resin encapsulation material than does copper which thus reduces the thermal stress arising under load.[74] Aluminium foils heating elements have been developed but are not widely used at present. Applications include foil firm wallpapers, cutting concrete and possibly soil warming. Heatsinks are very common through the world for cooling systems. High thermal conductivity of aluminium and ease of extruding or casting into solid or hollow shapes with integral fins makes the material ideal for heatsinks. Semiconductor devices and transformers tanks illustrate the wide diversity of applications in this field.[74] Its light weight makes it ideals for pole mounted transformer tanks and it has the added advantage that the material does not react with the transformer oil to form a sludge.

3.2 Copper

Copper is the only metal which we can find in a directly usable form of metallic in nature. Copper is the earliest metal which humans have used. Most of the copper is mined or extracted from large open pit mines in porphyry copper deposits that contain 0.4 to 1 % Cu. It is found in solid form and its atomic number is 29 and the electron configuration is [Ar]3d104s1. Copper is a d block metal which is in the group 11 and period 4.

Table 3.2: Properties of Copper

Property	**Value**
Melting point	$1357.77K$ [51]
Boiling Point	$2835K$[51]
Electrical conductivity	$5.98x10^7(S/m)$[51]
Thermal conductivity	$401w/(m.k)$[51]
Crystal Structure	Face centered cubic
Magnetic ordering	Diamagnetic
Maximum permissible current density	$3.1x10^6A/m^2$[33]

3.2.1 Mechanical properties:

Electrical and thermal conductivity both are present in copper which explains its softness.[51] Cu has one s-orbital electron and filled d electron shell so that it is characterized by high ductility and toughness, thermal and electrical conductivity and excellent corrosion resistance. With incomplete d shell, the metallic bonds lack covalent character which is relatively weak.[32] All of these characteristics are the result of Copper's structure. Cu has a face-centered cubic (fcc) crystal structure where cu atom is found at every corner and in the center of each face of the cube.

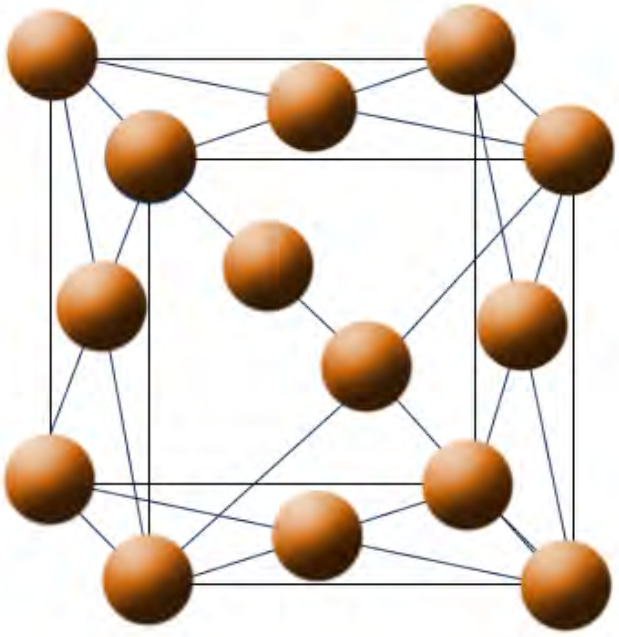


Figure 3.3: Face centered cubic (FFC) copper lattice with the lattice constant of 3.597 Å at 300K [26]

This unit cell is separated into three-dimensional spaces for building up the copper crystal structure. A cloud of free electrons can be found uniquely inside copper's atomic lattice which transfers electrical current and also thermal energy. Atomic attraction holds up the atoms in place inside the structure. As a result, cu gives us its high ductility and toughness for face-centered cubic arrangement. For single crystal lattice at macroscopic scale grain boundaries and materials hindrance flow under applied stress increases its hardness.[80] There is common phenomena in all metals that is called slip. For slip the atoms within the metal slide past one another in groups. The cu cell has four planes, as a result, the movement can occur in any direction or all of three directions along a specific geometric plane of atoms. Hence, cu metal experiences slip which turns out to excellent ductility and toughness of copper. At low temperature, it does not suffer from embrittlement. Besides this, its excellent corrosion resistance is available for the combination of electronic and crystallographic structures. The free electron cloud form coherent films protects the lattice from further corrosion. The face-centered cubic structure also cause another characteristic on the very planes with the slip. The atoms are packed so closely that makes difficult for hydrogen ions to pass through the small spaces in between them and causes stress corrosion cracking except in the most aggressive environments.[52]

3.2.2 Copper interconnect technology:

Copper is used as a conductor and for different purposes. Previously aluminum was used in interconnect for integrated circuits. The impact on the memory applications which consists of DRAM and flash memory has high sensitivity, high aspect ratios and little critical dimensions to line resistance. Nevertheless, the evolution to memory has its own challenge. The ever-increasing need for faster devices with shrinking dimensions has made interconnect RC delay parameter important which determines the IC design, design rules, packing density and device performance.

Table 3.3: RC delay for various process nodes[2]

Process Node	X-section Area	R/um (Ohm)	C/um (fF)
$180nm$	0.15	0.25	0.15
$130nm$	0.07	0.30	0.12
$90nm$	0.05	0.40	0.14

Table 3.4: RC delay for various process nodes[2]

SoC Freq. (MHz)	JwL/um	RC Delay/um
500	$0.01j$	0.040
1000	$0.023j$	0.036
1500	$0.040j$	0.056

So, to satisfy the increasing demand for $sub - 0.25um$ technology nodes and faster signal transport the cu thin film with low k dielectric materials have replaced aluminum for high performance integrated circuits.[11, 62, 27] Cu and low k dielectric materials combination can reduce 50% of RC delay of that for Al/SiO_2.[53] Besides that, Cu has lower electrical resistance and superior resistance to electromigration which makes it better conductor than Al. So, the chips which are using this technology can have tinier metal components, reduced energy to pass electricity through them and reduced number of interconnect levels.[27] Cu was first introduced by IBM, with assistance from Motorola, in 1997. During this transition process, Cu has to go through improvements of fabrication techniques which includes patterning the metal with different methods and introduction of barrier metal layer so that Silicon cannot damage the cu atoms potentially.

3.2.2.1 Fabrication:

Previously aluminum was patterned with the technique of photoresist masking and plasma etching which couldn't be used further for cu patterning. With the continuous progress per century, many form of volatile copper compound was found which were never used in industry. So, with the inability to use plasma etching process, industry has to rethink about new process for cu patterning which results into Damascene or dual damascene process and electroplating. Damascene process is a traditional technique of metal inlaying. The common process steps for cu fabrications are- firstly the damascene or dual damascene interval or interval dielectric

is deposited. This deposited dielectric may be multilayered and it may be etched stops such as SiN. The chemical mechanical planarization (CMP) may be needed for this step. Secondly the damascene or dual damascene structure is needed be etched and patterned into the dielectric. Thirdly the insulating underlying layer is patterned with open trenches which is significantly filled with thick coating of Cu. For electrodeposition a barrier or seed stack is deposited. After that the CMP is used to remove Cu if cu overburden the insulating layer. As the sunken Cu is not removed from trenches it turns into patterned conductor. This process is repeated for multilayered interconnection. In the damascene process single feature with cu is formed per damascene stage wherein the dual damascene process two features(via trenches) are formed at once. The interconnection is produced by layering the multi-layer of insulating layer and copper. Cu coating in a planer and uniform fashion can be removed by CMP and it prevents repetition at the copper-insulator interface.[62]

3.2.2.2 Barrier metal layer:

Copper diffuses very quickly in Si and conventional dielectrics. If it is not checked properly, it can cause severe threshold voltage shifts and junction leakage. In order to maintain a good electronic contact cu diffusivity has to be reduced.[62] A barrier metal all over interconnections prevents the diffusion of copper into surrounding materials. This barrier layer is mostly consists of TiN, Ta or W.[11] Silicon causes deep level traps when it is doped with cu which degrade the materials properties.[3] The thickness of the barrier metal has also influence on interconnect. If it is too thin, cu contacts can be poisonous to the connected devices and for thick layer the stack of two barrier metal films and Cu increases resistivity more than al interconnect as a result. The barrier layer usually has a high resistivity that causes an increase in the effective resistivity of Cu wires ($\rho = 2.2x10 - 6Ohm.cm$ compared to$\rho = 1.7x10 - 6Ohm.cm$for bulk Cu).[3] A thin barrier metal promotes low ohmic resistance. From past to present the improvement of conductivity is ongoing with the enrichment of technology. The improvement is modest but not as expected with the comparison of bulk conductivity of Al and copper. Al doesn't require any barrier metal on the metal lines as it doesn't diffuse intoSiO_2 insulators. On the other hand, the addition of barrier metals on all sides of cu conductor reduces the cross-sectional area of the conductor. Hence, scientist are searching for new ways to avoid using buffer layers to reduce diffusion of Cu into the Si substrate. For instance, using Cu-Ge alloy as interconnect vanishes the use of buffer layer.[96]

3.2.2.3 Electromigration:

Electromigration is needed for high direct current density applications. With the pace of time the integrated circuits are shrinking down which has raised up the practical significance of electromigration effect. When current flows through a conductor, there are two forces produced. The individual metal ions are exposed to the forces. The electrostatic force caused by electrostatic field can be ignored because the positive metal ions are shielded to some extent by negative electrons in the conductor. The other force momentum transfer within conducting electrons and metal atoms causes significant movement of the ions which results into electromi-

gration.[53]Cu has higher electromigration resistance which is 10 times better than aluminum, allows higher current flow through it at any given size.[11]

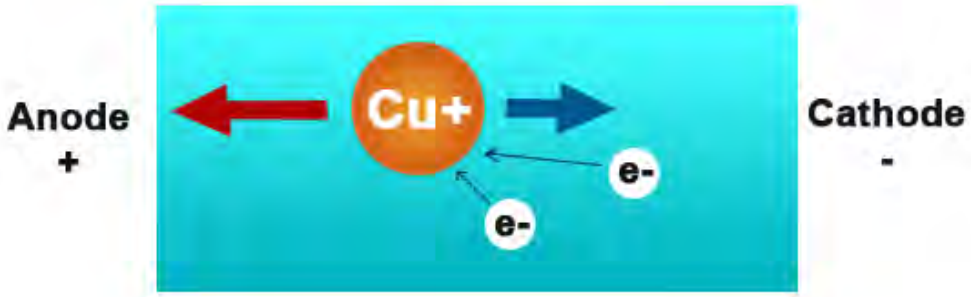


Figure 3.4: Electromigration occurs due to gradual movement of Cu^+ ions caused by momentum transfer among electron and Cu atom

Table 3.5: Properties of Copper and Aluminum

Property	**Al**	**Cu**
Lattice Diffusion	$1.4eV$	$2.2eV$
Grain Boundary Diffusion	$0.4 - 0.8eV$	$0.7 - 1.2eV$
Bulk Resistivity	$2.67uOhm.cm$	$1.67uOhm.cm$

A metal conduction shapes under the influence of a current flowing through it and which eventually leads to the breaking of the conductor because of electromigration resistance. The higher conductivity, lower resistance along with improved electromigration have made copper more attractive for interconnects. Overall improved performance has increased its benefits so that the full-scale investment is driven to cu based technology. Also, the fabrication method has improved. All of these has made it possible to replace aluminum with copper in interconnect.

3.3 Graphene

Now a day's world has huge demand for high-speed devices. As a result researchers have already put huge effort on making electronic devices faster. On this situation Graphene shows great potential. In 2004 two Russian-born physicists Andre Geim and Konstantin Novoselov physically discovered this mystery material what had been existed in theory among the physics and chemistry community throughout the century. this discovery eventually won the Nobel prize later. However, This material is made of pure carbon atom which has exceptional mechanical and optical property. Along with this Graphene gets lot of attention of researchers on electronic field due to its electrical and material property.

Table 3.6: Property of graphene

Property	**Value**
Electrical Conductivity	$1.96x10^{10}Sm^{-1}$ [24]
Thermal Conductivity	$2000Wm^{-1}k^{-1}$ [73]
Relative permittivity	$1.62 - 4.06$ [73]
Tensile strength	$130.5Gpa$ [38]
Light Absorbs	2% [68]

Graphene is single atom thick 2D material consist of carbon atoms. The electron configuration of an isolated Carbon atom is $1s^2 2s^2 2p^4$ but on a molecule 2s and 2p orbital can form sp^3 or sp^2 hybridization. In case of Graphene each carbon atom connects with neighboring carbon atom with sp^2 hybridization. Naturally this carbon atoms form a 2D plane with the angle of 120 degree apart from each other. As a result Graphene has a strong densely packed honeycomb structure as well as remaining p orbital provide free electrons to make it very good conductor for electricity and heat. Due to hexagonal lattice structure graphene two types of orientation zigzag and armchair.[15]

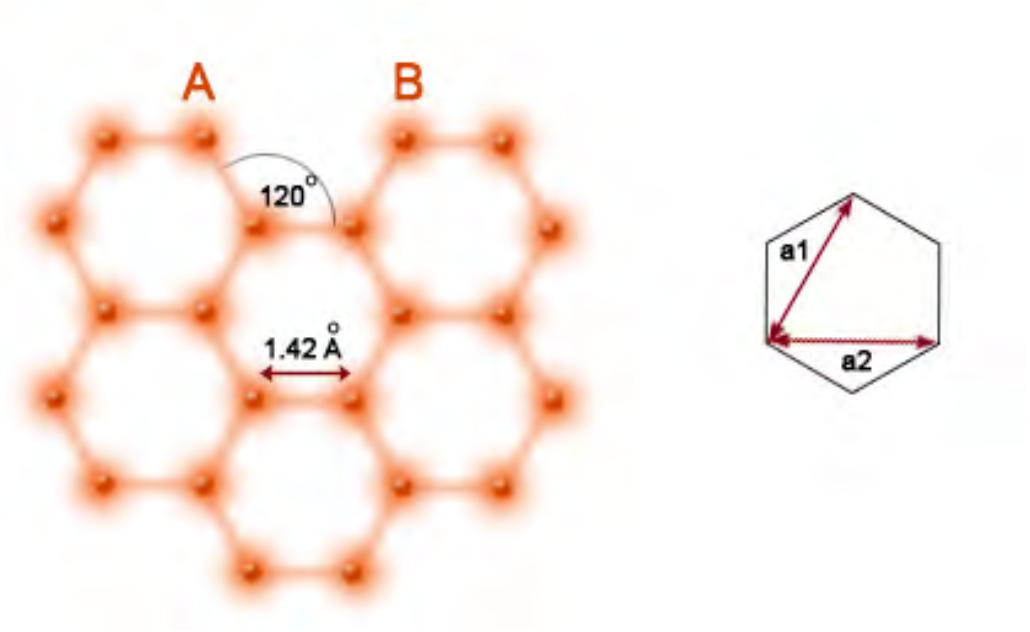


Figure 3.5: Graphene Lattice Structure

Mechanically graphene is one of the most strong material with tensile strength of 130 .5 Gpa and Young modulus of 1TPa [48] as carbon-carbon bond is only 0.14nm [38] in length. However, Graphene is a 2D material it is not perfectly 2D. There is small deformation of nearly 1nm [63] .

Here referring to figure 2.1 the lattice vector written as

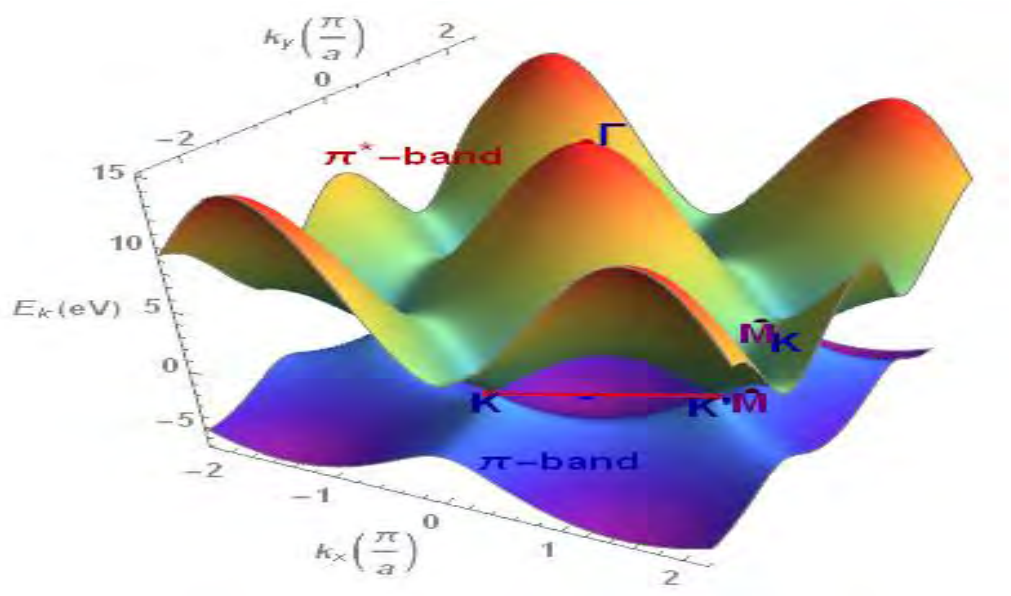
$$a_1 = a_0\sqrt{3}\Big(\frac{1}{2}, \frac{\sqrt{3}}{2}\Big)$$

$$a_2 = a_0\sqrt{3}\Big(-\frac{1}{2}, \frac{\sqrt{3}}{2}\Big)$$

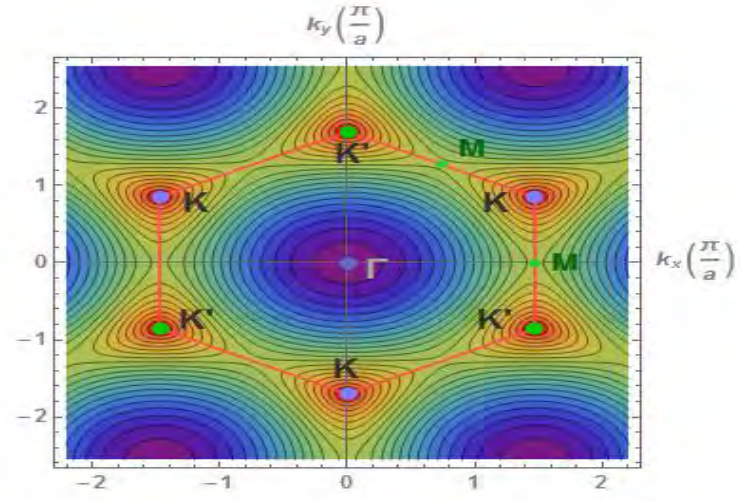
And after some simplification on wave function and with help of Hamiltonian the energy distribution over Reciprocal space is given by.

$$E\Big(k_x, k_y\Big) = \pm\gamma\sqrt{1 + 4\cos\left(\frac{\sqrt{3}ak_y}{2}\right)\cos\left(\frac{ak_x}{2}\right) + 4\cos^2\left(\frac{ak_x}{2}\right)}$$

Where $a = \sqrt{3}a_0$ is a lattice constant.



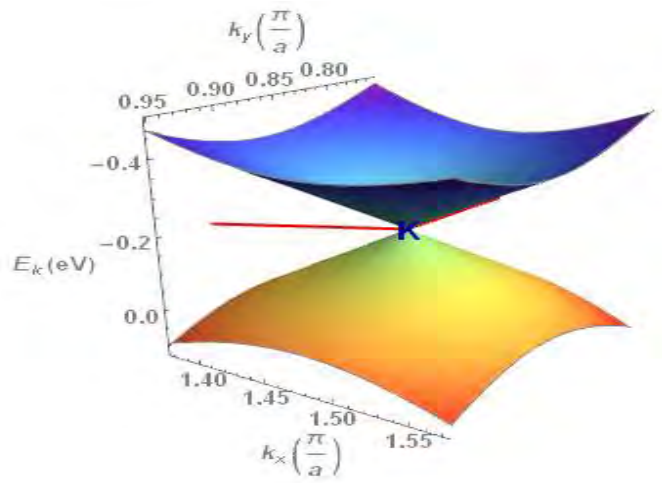
(a) Complete band dispersion over the whole Brillouin zone for π (lower surface or valence band) and π^* (upper surface or conduction band) bands of graphene



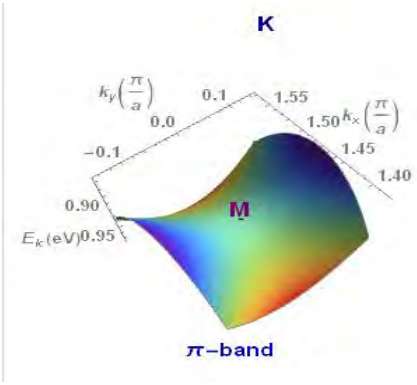
(b) Six K points at the corners of the Brillouin zone

Figure 3.6: Band Structure of Graphene along the whole Brillouin zone

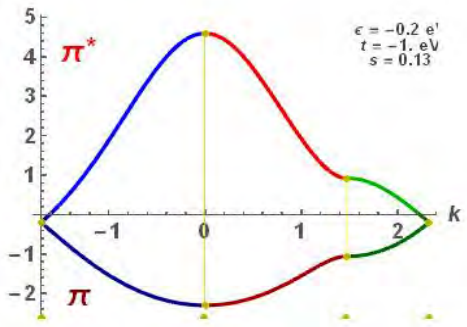
However, for this unique band structure graphene considered as semi metal and also by adding some impurity band gap can be created. On the other hand, optically graphene is almost transparent. A single layer graphene absorb about 2.3 % of incoming white light [68]



(a) six touching cone K-points where energy depends linearly on the wave vector



(b) nontouching m-points on Brillouin zone



(c) spaghetti diagram band structure of graphene along Brillouin zone forπ(lower surface orvalence band) and π^*(upper surface or conduction band)

Figure 3.7: Points of band Structure of Graphene

As mentioned earlier due to loosely bonded electron at p orbital makes single layer graphene very good conductor but as the layer increase the conductivity reduces due to inter layer interaction. Mainly this property makes graphene a very good material for interconnect. Not only that due to its strong mechanical and electrical characteristic manufacturing of very small scale devices is possible unlike never before.

3.4 Carbon Nano-Tube

To commence the discussion on carbon nanotube first we need to know what carbon nanotube is. If a paper sheet is rolled then a tube is formed and if the sheet is made of graphite then the rolling tube is called the carbon nanotube. Precisely we can call a rolling graphene sheet which is like a cylinder shape is the carbon nanotube.

A carbon nanotube can be in two structures either in single or multi-walled. Single walled nanotubes (SWNT) have diameter on the order of 1nm and can up to be centimeters long. Multi-walled nanotubes (MWNT) are comprised of several concentric single walled nanotubes which are detached by 0.35 nm distance. MWNT's have diameter from 2 to 100 nm and they can be tens of microns long [87]. We will delineate this two structures at this instant.

3.4.1 Single Wall Nanotube ($SWNT$):

A rolled graphene sheet is defined as single wall nanotube. They have diameters of $0.7 - 10.00nm$ but most observations found that their diameters are less than $2nm$. This nanotubes are one dimensional nanostructures. SWNT's composition depends on a vector which is perpendicular to the nanotube axis. This vector is called chiral vector and denoted by C_h. Also there is a variable called chiral angle θ, depending on which zig-zag and armchair configurations is determined. If $\theta = 0^o$ then its zig-zag and if its 30^o then the configuration is called armchair. If θ lies in between then it is chiral configuration. The chiral vector also known as roll up vector which can be described by the following equation:

$$C_h = na_1 + ma_2$$

[75] Where n, m are integers and a_1, a_2 unit vectors. For armchair nanotubes n = m and for zig-zag nanotubes m= 0 [75]. In figure 1 we showed the chiral vector and chiral angle which corresponds to the zig-zag and armchair configurations.

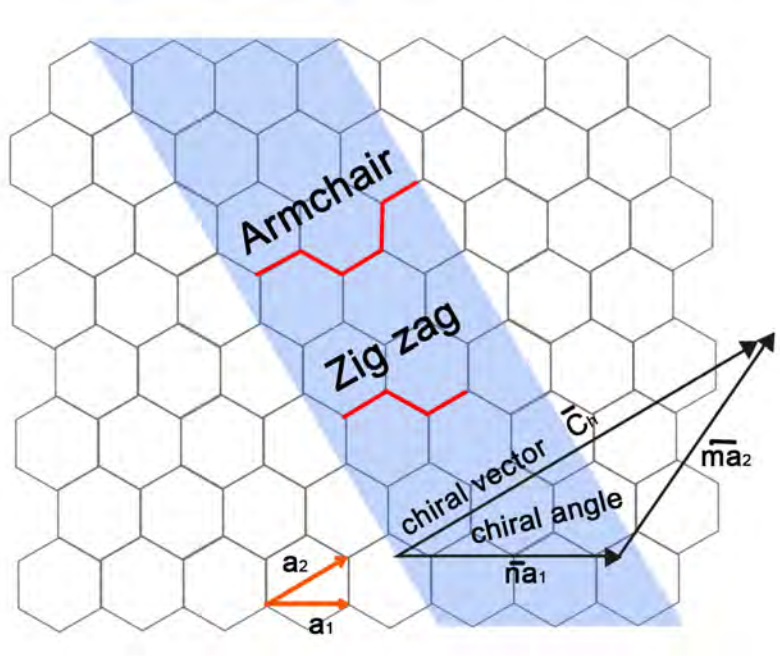


Figure 3.8: Carbon nano-tube configuration

Carbon nanotubes diameter can be determined by L/π, where L is the circumferential length of the nanotube and is given by

$L = |C_h| = \sqrt{(C_h.C_h)} = a.\sqrt{(n^2 + m^2 + nm)}$ [75]

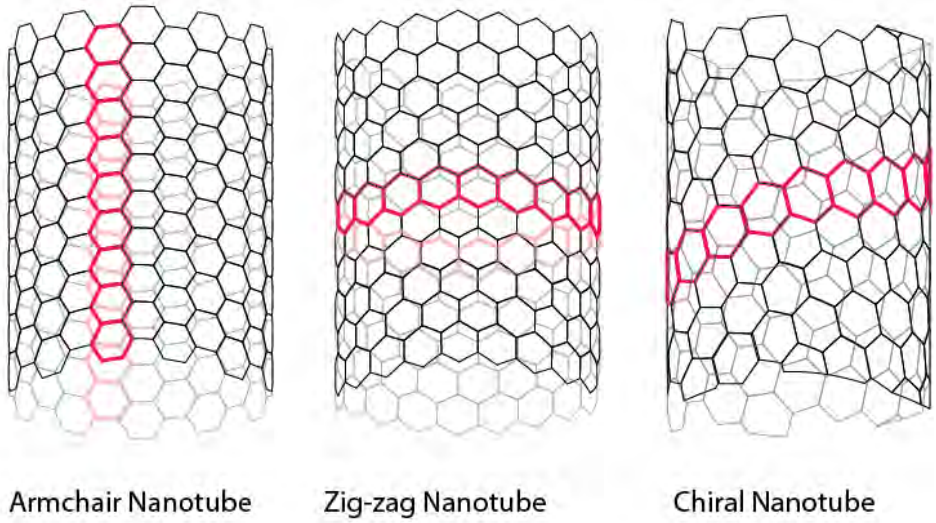


Figure 3.9: Armchair nanotube, (n,n); Zig-Zag nanotube, (n,0); Chiral nanotube, (n,m)[75]

3.4.2 Electronic Properties of SWNT

A single walled nanotube can be metallic or semiconducting which depends on its chirality and diameter. By scanning tunneling microscopy we can observe the energy gap of the semiconducting nanotube which commensurate with its diameter inversely. The armchair nanotubes (n, n) are metallic. Whereas the zig-zag tubes (n, 0) can be either metallic or semiconducting. When n is an integer multiple of 3 then the tubes show metallic behavior, other than that they shows semiconducting behavior [72]. As C_h rotates form (n, 0), Chiral nanotube with (n, m) can be demonstrate similar behavior like zig-zag tube that is when $(2n + m)/3$ is integer they are metallic otherwise semiconducting [72]. The armchair nanotubes with indices (n, n) are truly metallic with a chiral angle of 30^o [72]. The armchair nanotubes band crosses at $K = \pm 2/3$ of the one dimensional Brilluoin zone. SWNT's which are emanated by laser vaporization and arc methods, fully subsumed by metallic armchair tubes [72].

3.4.3 Multi Wall Nanotube

Multi wall nanotubes are made of various concentric single wall nanotubes where interlayer spacing is 0.35 nm.

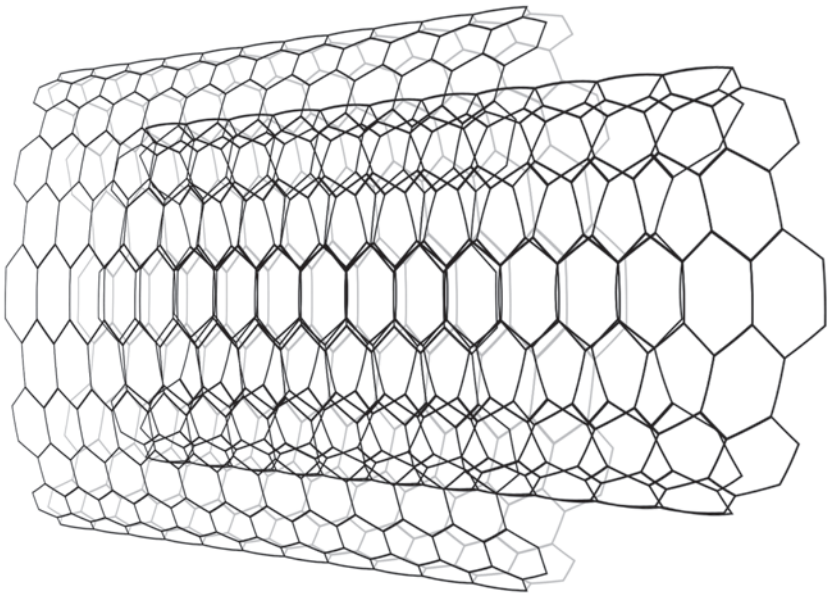


Figure 3.10: Multi Walled CNT

3.4.4 Mechanical Properties of Nanotubes

Carbon nanotubes mechanical properties sharply recline to its structures. This is because of the high anisotropy of graphite [76]. To know the Young's modulus of a material is the rudimentary stage of using the material as a structural element in variety of applications. Practically structural engineering is comprised of the theory of elasticity and stress under the elastic limit is the main concentration of designing, safe loads need to be half or less of the elastic limit [37]. Young's modulus is directly related to the chemical bonding of the materials atom. The Young's modulus of carbon nanotube is inlaid to the sp^2 bond strength and it should be tantamount to graphene when its diameter is large enough to undistort C-C bonds significantly [76].Salvetat, J.-P., et al. calculated the Young's modulus of a single tube which is greater than $10TPa$. This value is much higher than the most optimistic prescience. Then comes carbon nanotubes strength. A materials strength do not only depends on the kind of the material but it depends also on its history, the atmosphere, the pressure and the temperature, and the measuring system. Strength is closely associated to the structural defects and imperfections that a solid can have. Large diameter MWNT's have average bending strength of $14.2 \pm 0.8GPa$ which was calculated by Wong et al. [94]. Salvetat, J.-P., et al.'s work demonstrate that Young's modulus for MWNT's are subjected to the degree of order within the tube walls also they showed a schematic representation of their findings in which Young's modulus has an inverse relationships with disorders.
Carbon nanotubes theoretically predicted mechanical properties such as- high strength,

outstanding flexibility, elasticity are now observing by experimentalists.

4

The Problems with Copper

In modern days integrated circuits are built with a large number of transistors and we also need the compact finishing of the IC's. As a result the dimension of the integrated circuits shrinks. With the shrinking dimension and increased number of devices, resistivity and capacitance increase result in poor performance of the IC
Scaling down the all local dimensions of interconnect has increased the wire resistance per unit length. For better performance, the mostly used copper cannot cope up with the pace now. Copper is facing more challenges day by day. If the scaling factor is n, the capacitance will remain unchanged but the resistance will increase by a factor of n^2. For local interconnect wire delay remains unchanged but for global interconnect wire delay increases by n^2. As a result, the maximum current density increases with scaling for both of interconnects and facing more challenges. This section is going to describe how the resistivity of copper interconnect increases as the scaling goes down. Several factors like bulk resistivity, electron-electron interactions, electron-phonon interactions, mean free path, impurities and point defects etc. lead to temperature dependent resistivity. Copper interconnect has a dependency on line width as it gets narrower than 100nm its resistivity increases exponentially. Besides this, the thickness dependent resistivity increases as wire height go down. The surface and grain boundary have also a great impact on resistivity in Nano-scale.
Currently copper is mostly used for interconnection. Unfortunately it has problems of increased resistivity due to surface roughness and grain boundary scattering which significantly increase RC delay. Electromigration is also a big problem of copper interconnect. It creates hills and voids within the interconnect and create short among the wires . So Copper is not very favourable in the field of interconnect. As a result we need to switch to a new material also keeping in mind the best performance of the IC's. in this sense a promising material is graphene and carbon nanotube (CNT) which can compensate all this problems with increased performance and reliability.

Table 4.1: Schottky Barrier of Copper-Semiconductor Interfaces

Copper work function = 4.65			
Crystalline Si	**Amorphous Si**	**Ge**	**GaAs**
0.790 [88]	0.97[95]	$n-0.89, p-0.85$[90]	$n-0.89, p-0.85$[90]

Table 4.2: Schottky Barrier of Graphene-Semiconductor Interfaces

Graphene work function = 4.8			
Crystalline Si	**Amorphous Si**	**Ge**	**GaAs**
0.64	0.82	$0.4 \approx 0.43$[30]	$n - 1.08, p - 0.81$

Table 4.3: Schottky Barrier of Graphene-2D materials Interfaces

Graphene work function = 4.8		
MOS2	**WS2**	**WSe2**
0.18[43]	0.6[84]	0.22[70]

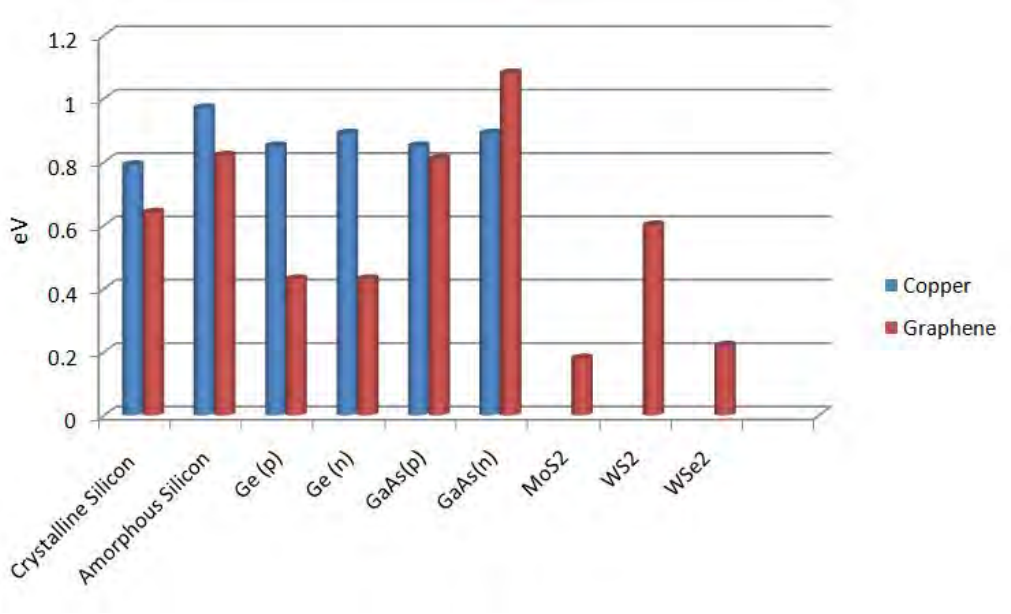


Figure 4.1: Comparison of schottky barrier between copper and graphene with different materials

4.1 Limitations of Copper

Copper is used in interconnects for more than 1 decade due to its low resistivity, high conductivity. But in nanoscale copper wires has several disadvantages that limit's integrated circuits performance. Now a day's our devices are getting smaller and smaller and the size of interconnect also getting smaller. Unfortunately, Copper, the most commonly used interconnect material cannot cope with this miniaturization. In this small scale like thickness is less than $10nm$ impose many challenges for thickness and grain size. There are many factors controlling the resistance of interconnects. Intrinsic contributions are bulk resistivity, electron-electron interactions increased by lower temperature at $T^{-0.5}$. The product of mean free path λ and the resistivity

ρ at any given temperature T is given by the equation.

$$\rho(T).\lambda(T) = \frac{(12\pi^3 h)}{(e^2 S_F)} = 6.6X10^{-12}\Omega.cm^2$$

[44] Where Fermi surface of free area is S_F and h is Planck's constant. Along with it electron phonon interaction decreased by lower temperature, localization, quantized effects on nano-wires and thin films. Electron phonon interaction described by Bloch-Gruneisen formula.

$$\rho(T) = \rho(0) + \alpha_{(el-ph)} \frac{T}{\Theta_R}^{n} \int_0^{\frac{\Theta_R}{T}} \frac{x^n}{(e^x - 1)(1 - e^{-x})} dx$$

[44] Where the $\theta_R and \alpha_{(el-ph)}$ are material-dependent Debye Temperature and prefactor. Besides those, the impact of impurities and point defects on electrical resistivity is observed when the internal phonons spaces exceed the distance between the impurity scattering sites. This effect is added to intrinsic temperature dependent resistivity as temperature independent contribution. It reduces the electron mean free path as additional sources. In the fabrication process of Cu interconnects Cu deposits initially causes high resistivity. At room temperature the grain growth of bulk Cu is much larger than Cu deposit's thickness. Quantifying Size Effects is the other thing affecting resistivity of copper interconnects. In smaller device below $100nm$ specularity and grain boundary reflectivity can be measured accurately without considering geometrical dimensions. However, the resistivity of copper interconnect largely depends on line width and when it gets narrower than $100nm$ resistivity gets exponentially larger.

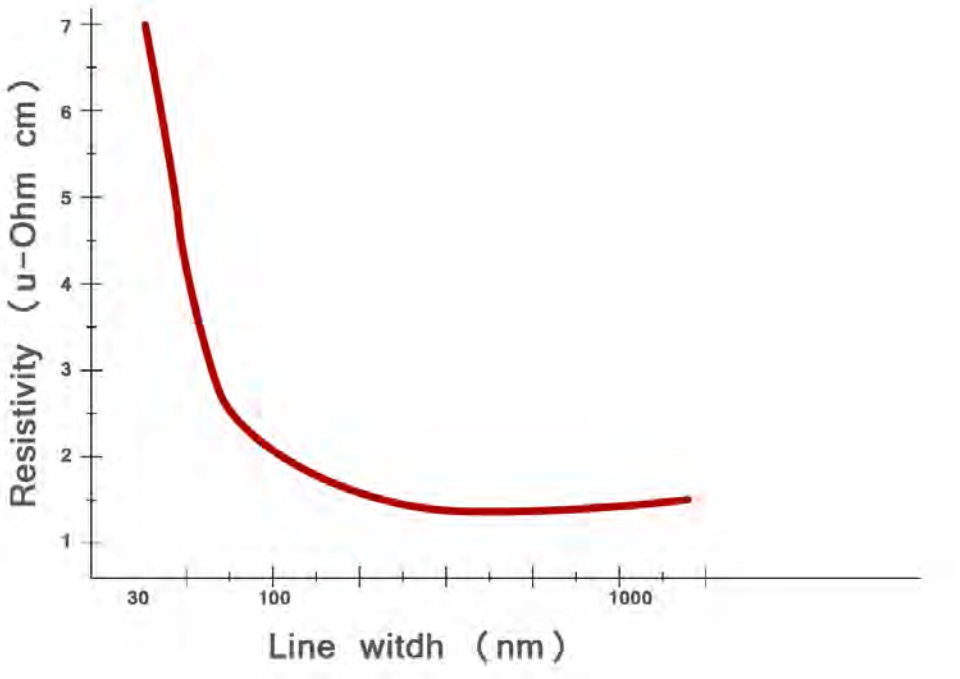


Figure 4.2: Dependency of resistivity on interconnect line width

On the other hand in nano-scale along with line width resistivity also depends on wire height. Here in the plot below $90nm$ wire shows more resistive than $185nm$wire. So over all smaller cross-sectional area shows more resistivity in nanoscale

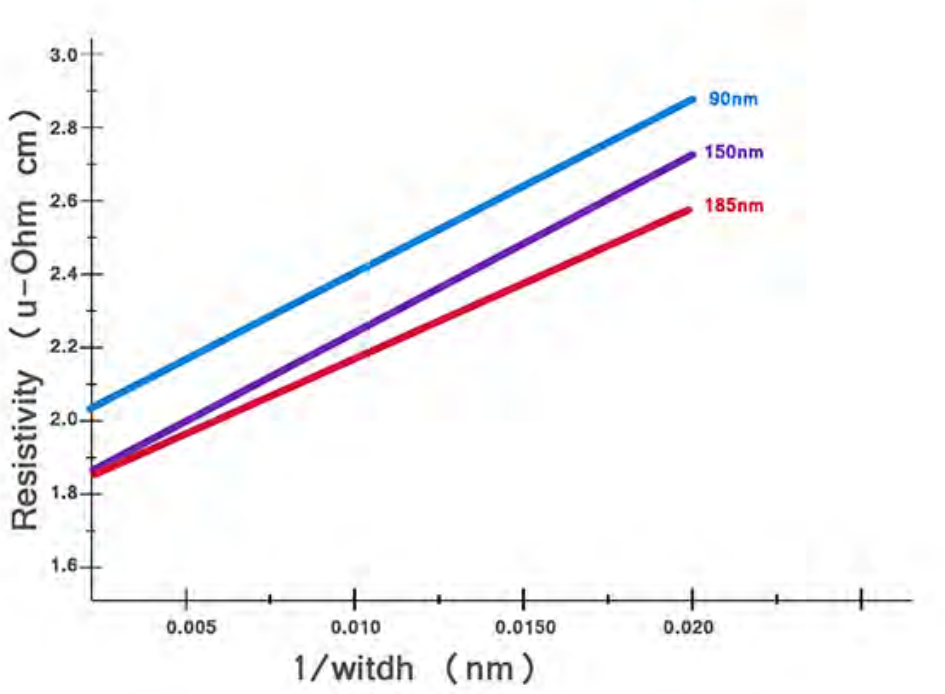


Figure 4.3: Plot of resistivity and 1/line width

Here Cross-sectional area shows point of interest. Though measuring this is theoretically straightforward, In practice it is challenging in nano-scale as ion beams can easily modify Cu/low-k dielectric structure. So, It measured by average value of thermal depends of line resistance[39]. The resistivity and cross-sectional area approximated by the equation [49].

$$\rho = \frac{R_T.\frac{d\rho_\theta}{dT}}{\frac{dR}{dT} + R_T.CTE} \approx R_T.\frac{\frac{d\rho_\theta}{dT}}{\frac{dR}{dT}}$$

$$A = \frac{L.\frac{d\rho_\theta}{dT}}{\frac{dR}{dT} + R_T.CTE} \approx L.\frac{\frac{d\rho_\theta}{dT}}{\frac{dR}{dT}}$$

In this equation $\frac{dR}{dT}$ is temperature dependence of line resistance which can be determined from experiment and $\frac{d\rho_\theta}{dT}$ is temperature dependence of bulk resistivity. For copper it is $0.0677W.cm/K$ in the range of $200K - 400K$. L is the line length and CTE is coefficient of thermal expansion. For copper it's $16.7X10^{-6}K^{-1}$. R_T is the linear resistance at given temperature. However, our focus will be on surface and grain boundary scattering that affects resistivity in nanoscale. Electrical conduction is affected by non uniform surfaces which approve perfect specular scattering. Monte-Carlo[7] approximate the the change of resitivity as the interconnect thick-

ness is t and surface roughness of that material is sinusoidal with the wavelength of .

$$\frac{\rho}{\rho_0}(S,\lambda) \approx 1 + 0.375(1-p)\frac{S\lambda}{t} + 1.5\frac{R}{1-R}\frac{\lambda}{g}$$

Where p is the specularity of the surface, R is the grain boundary reflectivity and g is the grain size. For $t = 60nm$ and $\lambda = 20nm$ for a Cu thin film a $0.7\Omega.cm$ increase in the resistivity is predicted if the upper surface modulation amplitude increases from 0 to $5nm$. It is not known if this surface roughness can be controlled or not. This phenomenon has been identified by understanding the behavior of lines with varying width and above conduction area contribution, change of resistivity of the lines have no significance. The resistance on $20nm$ wide lines can be increased only by 3% to 6% over the ideal case, is predicted by another study[83].
Another important aspect is grain boundary scattering. When Copper is deposited on substrate, grain boundaries forms. This periodically spaced grain boundaries present along the interconnect line and electron scattered along with those. Mayadas and coauthors [60, 59]. Derived the expression where a relationship has been found between the resistivity of material with grain boundaries ρ_{gr} and without grain boundaries ρ_0

$$\frac{\rho_0}{\rho_{gr}} = 1 - \frac{3\alpha}{2} + 3\alpha^2 - 3\alpha^3 ln(1 + \frac{1}{\alpha})$$

$$\alpha = \frac{\lambda}{r_{gr}}.\frac{R}{1-R}$$

Here r_{gr} is the grain size , R is the probability of reflecting electron at grain boundaries and λ is mean free path below bulk value. From above relation it has seen that resistivity increases with decreasing mean free path. So here copper has 39nm mean free path. So material with higher mean free path has nice potential in the field of interconnect.

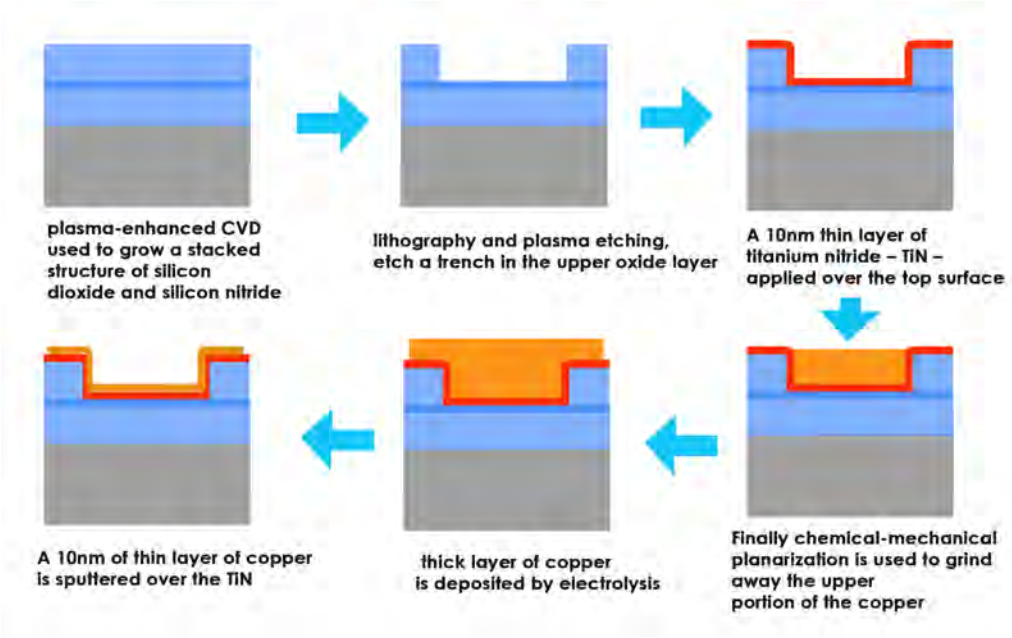


Figure 4.4: Damascene process

Another challenge is copper deposited on substrate via damascene process. Copper can easily diffuse in silicon substrate so to stop this Titanium nitrate (TiN) is used and this insulating layer cannot be removed . However the main problem is deposited copper cannot be etched away chemically. As a result chemical mechanical planarization (CMP)[98] has to be used and this is not efficient.

5

Graphene, Carbon Nano-Tube and Interconnects

Copper was the most commonly used material in interconnects in the integrated circuits for a long time. Things came into such a state where more speed and less resistivity is need in order to make more efficient devices and more compact devices for the near future. The more the resistance, the more the heat resulting the dropping of efficiency. Devices are shrinking leading to the limitation of the use of copper. The reasons why graphene is better than copper are in a couple of factors. Firstly, the resistance, where the resistance is zero.This is because graphene has de-localized electrons which allow it to be a very good conductor. Also, the zero resistance is caused due to the free area where the electrons can move on smoothly without crashing into any places. Electro-Migration Characteristics is present in copper where as it is not present in graphene. This happens when the electrons are constantly bombarding the copper ion, resulting the movement of the copper ion and thus compiling at one end and loss of the copper ion makes the other part a void. This causes the copper line to gain in resistance and can also cause a short circuit inside the system causing a system failure. Also, as we are decreasing the size of the electronics and making much complex systems, we need smaller connections connecting a lot of components inside the system. This leads to high current flowing in a much smaller wire. This is the most limiting factor which causes the copper to reach it's maximum point. In order to turn up the pace in regards the speed and efficiency graphene is the better alternative for this. One day or the other current systems will be out matched by the future systems by newer and faster components, which leads to a better interconnect. This leads the idea of graphene.

When graphene is interfaced with any other compounds, it creates a Schottky barrier. Schottky barrier is an electrostatic depletion layer which is formed at the junction of a metal and a semiconductor, which eventually causes to act as an electrical rectifier. From the figure 5, we can see that the barrier height is greater, thus electrons have to waste a lot of energy in order to pass through. Thus, that can be solved by putting another compound into the mix where the barrier height is less.

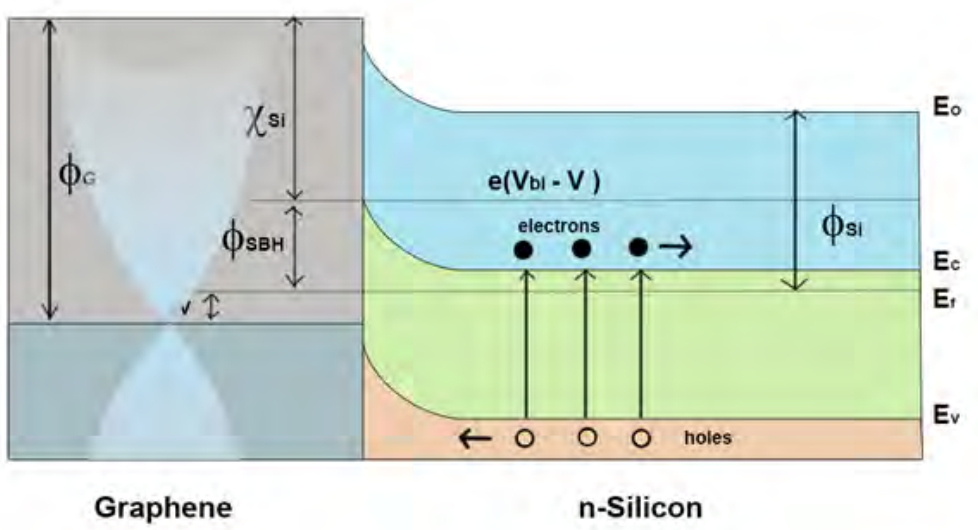
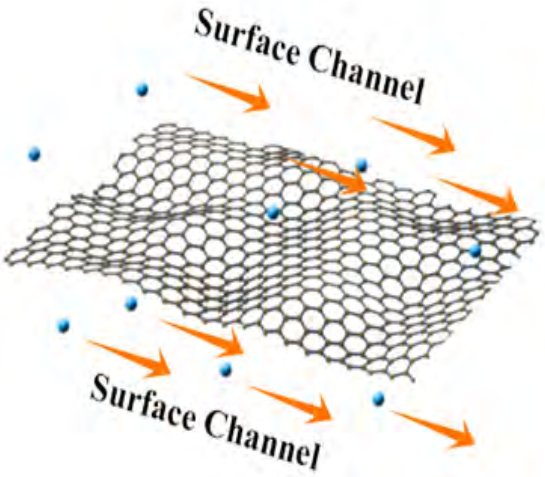


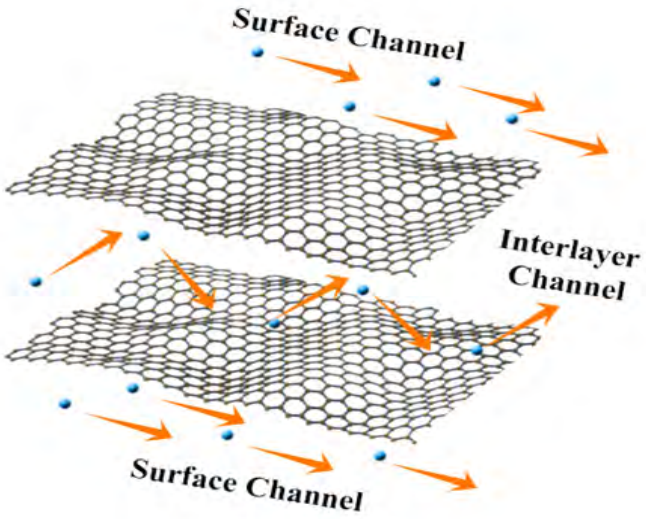
Figure 5.1: The Schottky barrier of Graphene n-si

5.1 Graphene as interconnect

As device getting smaller, the thickness of interconnect also gets smaller. Unfortunately we have already seen that resistivity of copper increases exponentially with decreasing thickness. On the other hand Graphene shows something opposite. Graphene has lower electrical resistivity ($1.0u - Ohm - cm$) [71, 9, 55] even lower than other good conductors like silver($1.5u - Ohm - cm$). In theory Graphene has good electron mobility and in practice according to Geim et al.[65] its more than $2.0x10^5 cm^2 V^{-1} S^{-1}$. In order to observe the affect of thickness in graphene like single layer (SLG), few layer Graphene(FLG 2 to 9 layer) and GNs ($3nmto100nm$) Fang et al [29] uses Boltzmann transport theory and 2D electron gas model . Graphene is actually an arrangement of carbon atoms in flat hexagonal lattice where this atoms stay in sp^2 hybridization and forms stable σ bonds. On the other hand p orbital electrons form electron gas as they are connected much weaker π bonds. As a result in each graphene sheet contains two electron gas channels on both side of it. During the conduction, surface channels shows electron –electron scattering on the other hand along with this interlayer conduction affected by both electron-electron and electron-phonon scattering.



(a) electron flows on single layer Graphene



(b) electron flows on multi-layer Graphene

Figure 5.2: electron flows more smoothly in single layer as it only affected with electron-electron scattering but when layers increases along with electron-electron scattering electron-phonon scattering also take place

Here, For the area A current density along the x axis is,

$$J_x = [\frac{4\pi e^2}{2dh^2} \int_0^\infty \epsilon\tau(\epsilon) \frac{\delta f_0}{\delta \epsilon} d\epsilon] E_x$$

Where ϵ the energy level, thickness of electronic plane is is d, f_0 is the Fermi function and E_x is electric field along the axis. Now for this 2D electronic gas polynomial

approximation of this Fermi integral shows the conductivity of it as follows:

$$\sigma = \frac{2\pi e^2}{dh^2}\Big\{\epsilon_F\tau(\epsilon_F) + \frac{(\pi K_B T)^2}{6}[2\tau'(\epsilon_F) + \epsilon_F\tau''(\epsilon_F)] + ...\Big\}$$

Where electron scattering mechanism will determine τ the relaxation time for electron to move f to f_0 However during conduction fermi integral also provide average momentum as follows

$$\bar{p_e} = m_e * \bar{v_e} \cong p_F\Big[1 + \frac{1}{6}\Big(\frac{\pi K_B T}{\epsilon_F}\Big)^2\Big]$$

Here p_F is Fermi momentum,

$$p_F = \frac{h}{2\pi}\sqrt{2\pi n_{es}}$$

Where n_{es} electron concentration Fang et al combines all this equations provide a equation for conductivity of single layer Graphene

$$\sigma_{SLG} = \frac{8\sqrt{2}\pi\epsilon_0\epsilon_r}{n_{es}dh^2}\epsilon_F p_F\Big[1 + \frac{1}{3}\Big(\frac{\pi K_B T}{\epsilon_F}\Big)^2\Big]$$

And electron mobility express as

$$\mu_{SGL} = \frac{8\sqrt{2}\pi\epsilon_0\epsilon_r}{n_{es}eh^2}\epsilon_F p_F\Big[1 + \frac{1}{3}\Big(\frac{\pi K_B T}{\epsilon_F}\Big)^2\Big]$$

For the bilayer Graphene conductivity is just average conductivity of two surface layer channels and interlayer channel where interlayer channel conductivity denoted as

$$\sigma_{ic} = \frac{4\sqrt{2}\pi e^2\epsilon_0\epsilon_r m_e * \bar{v_e}}{n_{es}dh^2(e^2 + 2\sqrt{2}\epsilon_0\epsilon_r m_e * \bar{v_e}^2 d)}\epsilon_F$$

And electron mobility of bilayer graphene is

$$\mu_{ic} = \frac{4\sqrt{2}\pi e^2\epsilon_0\epsilon_r m_e * \bar{v_e}}{n_{es}eh^2(e^2 + 2\sqrt{2}\epsilon_0\epsilon_r m_e * \bar{v_e}^2 d)}\epsilon_F$$

So combining all above the equations for conductivity and electron mobility for multilayer graphene can be written as,

$$\sigma_n = \Big(\frac{2}{n}\sigma_{SGL} + \frac{n-1}{n}\sigma_i c\Big)$$

$$\mu_n = \Big(\frac{2}{n}\mu_{SGL} + \frac{n-1}{n}\mu_i c\Big)$$

Secondly, when elections flow through copper it get reflected by grain boundaries also known as grain boundary scattering of electron which dramatically increases electrical resistivity. Mayadas[61, 60] shows an equation which relates electrical

resistivity with grain boundaries. If material resistivity with grain boundaries $\rho_g r$ and for free material ρ_θ then the equation as follows,

$$\frac{\rho_\theta}{\rho_{gr}} = 1 - \frac{3\alpha}{2} + 3\alpha^2 - 3\alpha^3 ln\Big(1 + \frac{1}{\alpha}\Big)$$

$$\alpha = \frac{\lambda}{r_{gr}} . \frac{R}{1-R}$$

Where R is the probability of electrons to get reflected on grain boundaries, λ and r_{gr} is mean free path and grain size of material respectively. Now copper has the mean free path of $39nm$, on the other side graphene has $100nm$ [14] and Graphe also has lower grain size than copper.

5.2 Advantages of Graphene

Having a zero band gap, electrons in graphene acts like as massless Dirac Fermions which can give less power consumption and better performance due to prolonged carrier velocities.Graphene has an ambipolar nature that means we can use it both as a n and p type material. n and p channel can co-habit on the same layer as it is seen that charge carriers puddles in graphene layer at zero field [81]. Graphene devices have mobility limit up to $40,000 cm^2/Vs$ [20] at the room temperature because there exist trapped charges in the substrate. To increase the mobility of graphene, efficient screening [54] and/or complete removal of the basal substrate is highly requisite [13]. Mobility surpassed $200,000 cm^2/Vs$ in suspended and annealed graphene-based devices. This is the highest value of mobility in a semiconductor or in a semimetal so far [12, 12]. The mobility gets affected by chemical doping [77] or high electric field induced carrier concentration. The effect is slender which conceives that there can be a ballistic transport regime at 300k on a sub-micrometer scale [35]. Graphene is a semi metal with no energy gap but special procedure can create a energy gap in graphene. Such as

1. Inserting sp^3 hydrocarbon defects in sp2 lattice [31].
2. Distortion of the honeycomb lattice under uniaxial strain [31, 34]
3. Lateral confinement in ribbon like shapes [36]

Among these three the 3rd one is implementable in interconnects application [4] It is possible to turn graphene nano ribbons from perfectly metallic to semiconducting which is theoretically proved [69]. In graphene nano ribbons the energy gap varies with its length and width

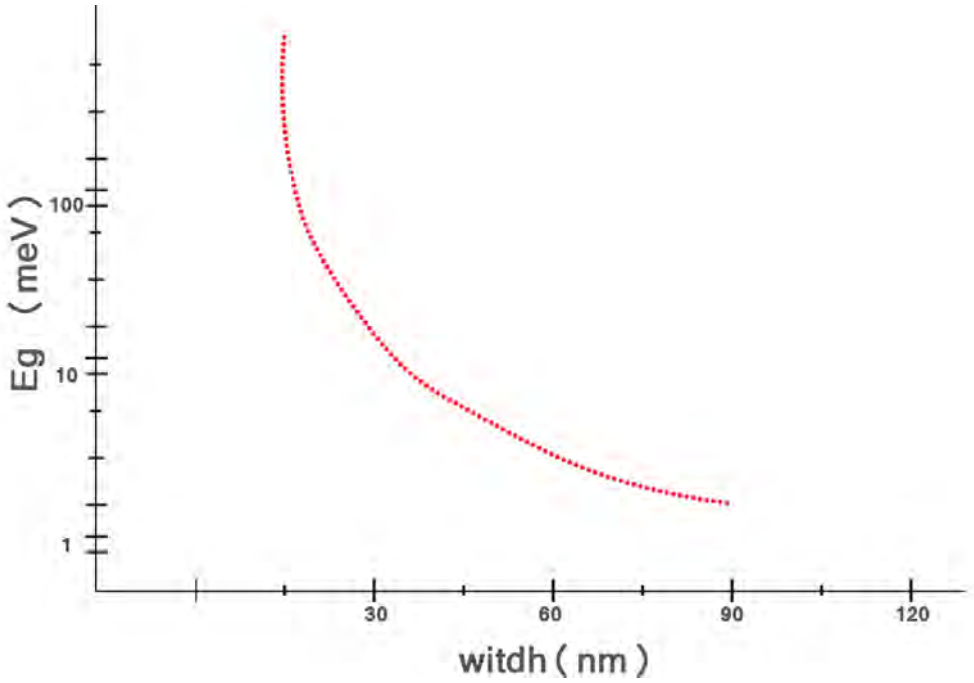


Figure 5.3: Energy gap Variation in graphene nano ribbons

There are reasons why Graphene nano ribbons (GNR) can outperform Cu in interconnects.

1. Graphene NR's has high conductivity also electron mean free path as high as few hundred nano meter.[9]
2. For strong C-C bonds in graphene, GNR has great hindrance to electromigration which gives them excellent mechanical potency and high current carrying capacity more than $10^8 A/cm^2$ down to $16nm$ widths [67]. In Cu this value is about $10^6 A/cm^2$ with scratches on the surface.
3. Thermal conductivity of sub-20 nm GNR's are more than $1000W/Km$. [67]

GNR's which are non interacting and having smooth edges and Fermi energy above 0.2 ev may outsail copper which are at small cross sectional dimensions and long lengths [42]

5.3 Reliability of Graphene Interconnects

It is important to know how graphene interconnects degrades with time means what happens to the interconnect when it is stressed at a constant current density. At nanoscale interconnects the thickness of the wire becomes very low and in this thickness graphene wires are required to withhold higher current density compared to Cu. Wire life time means the time required to breakdown or 20% decrease in conduction of actual value by what comes first order [67]. Graphene wires conductivity decreases with time when it is stressed at a constant current at 550K. Same thing happens for Carbon Nanotubes [21]

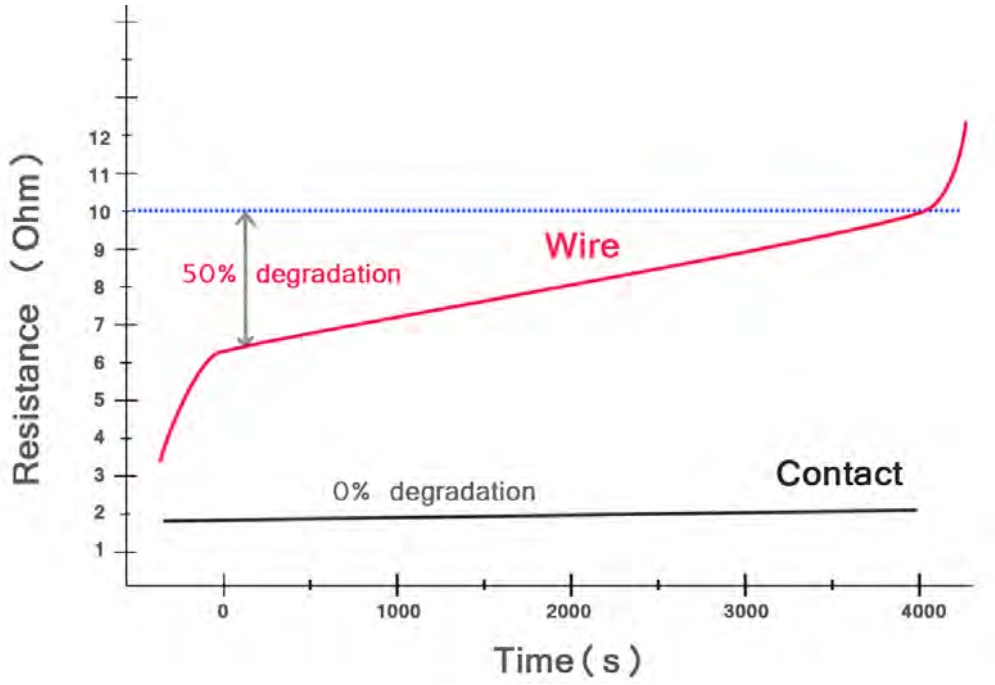


Figure 5.4: Wire resistance linearly drops

The quality of the contact remains the same since Graphene to metal contact resistance is not changed due to stress. Before breaking down the conductivity of the wire decreases 5 to 50% of the initial value. By Raman Spectral Scan map, more specifically Raman D peak intensity we can determine the defective graphene lattice structure. In Raman Spectral Scan Map the condition of a $100um$ wire stressed at $30MA/cm^2$ [21].

It is shown that before stress the defects are only on the edges of the graphene and after the stress localized in plane defects are formed along the wire and the reason behind this is graphene oxidation. This phenomenon can be correlated with the physical break that is visible in the optical image. By this we can clearly say that life time of graphene wire can be correlated directly with defect formation [21]. To calculate Mean time of a wire to fall (MTTF) we use Black equation:

$$MTTF = CJ^{-n}e^{\frac{Ea}{KT}}$$

where C is a material constant, Ea is the activation energy and n is current density exponent (value ranges from 1<= n <=2).$100um$ Graphene wire stressed at $20MA/cm^2$ shows MTTF $\approx 6hours$.[21]

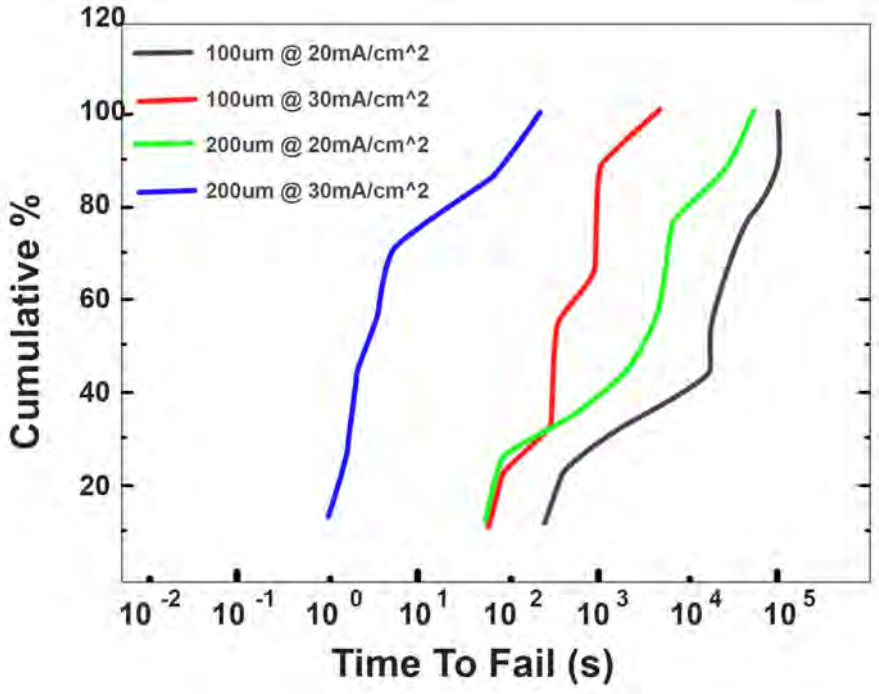


Figure 5.5: Life of interconnect of different length's wire at 550K. $100um$Graphene wire stressed at $20MA/cm^2$ shows MTTF $\approx$ 6 hours

In comparision with Cu's electromigration (EM) lifetime the MTTF of uncapped graphene is 15% better than SiCN-capped Cu EM lifetime but it is worse than COWP-capped CU (5.1) [21].

Table 5.1: Comparison of uncapped graphene wire with capped copper wire

Length(um)	125	100	100
Width(um)	0.4	2	3
Capping material	SiCN	CoWP	NA
$\mathbf{J}_{stress}(A/\mathbf{cm}^2)$	$2x10^7$	$2x10^7$	$2x10^7$
Temp.(K)	595	650	550
MTTF(hour)	5.2	8.5	6

By these understanding we see that uncapped graphene wire is better than capped Cu wire in interconnects. Although the MTTF of graphene wire is not that high future study is needed to determine capping material which can optimize the MTTF can make the graphene interconnects relaliable.

5.4 Advantages of Carbon Nano-Tubes

At nano scale (less than $100nm$) higher current densities prolong electromigration failure. For interconnects at or below $16nm$ new materials need to be introduced. Carbon Nano-tubes (CNT's) are capable of standing against greater than $10^9 A/cm^2$ of current densities with also approx. $1nm$ diameter which is three order of magnitudes greater than copper[93]. In mean free path comparison with copper it has MFP drastically higher than copper which is in the order of microns [17, 41]. In addition to higher MFP CNT's have ballistic transport and extremely high thermal conductivity [8, 22]. From two types of Single walled Nano-tubes(SWNT's, radius less than 1 nm) metallic and semiconducting, metallic SWNT's can work in GHz range and conductance of these SWNT's are approaching to their theoretically predicted values of $(4e^2)/h$. These SWNT's can work as transistors or as interconnects with this frequency range [23, 18]. Not only this, CNT's have natural geometrical shape of being a wire which make them best suit for nanoscale interconnects [97, 82]. Having dynamic behavior of c-c bond, 1D tabular shape and electronic band structure makes CNT's salutary replacement over copper in nano-scale interconnects. Decreased resistance, Antagonism to electromigration and greater thermal conductivity are three main benefits we can get from CNTs.

5.4.1 Decreased resistance

For a single tube, quantum resistance limits the short interconnects but in long interconnects densely packed bundles of nano-tubes can outsail copper in terms of conductivity [81].

5.4.2 Antagonism to Electromigration

In the hexagonal lattice shell of a CNT there are powerful C-C bonds which make this elements undergo current density of $10^9 A/cm^2$ where copper shows structural injury at $10^6 A/cm^2$ of current densities [81].

5.4.3 Thermal Conductivity

Diverse carbon nano-tubes can have greater thermal conductivity in the range of thousand W/mK [89, 92].
The energy gap of carbon nano-tube has an inverse relationship with its diameter. That's why small diameter SWNT have to be decreased while its growing as it will contribute in the reduction of the conduction of the bundles and vias architectures.

6

The Production Route of Graphene

In order to use graphene in interconnects,first we need to understand how to make the graphene. There are several ways in order to make graphene.

6.1 Micromechanical Cleavage

This process was first found out by the researchers in Manchester where they used scotch tape and repeatedly cleave graphite until there is only a single layer of graphite left , which we call it graphene[38]. Using this method is a lot of work, thus the word "micromechanical" comes in. This process is cost very cheap, but the disadvantage of this process is that it is not so efficient in terms of quality. Thus, not the best for industrial purposes.

6.2 Anodic Bonding

This method has been said to produce quality single layer flakes[64, 91]. This method consists of using borosilicate glass and Highly Oriented Pyrolytic Graphite(HOPG) are used to bond graphene flakes to glass, HOPG being used as a positive electrode and the borosilicate glass being used as the negative electrode. After a high temperature and a high electrostatic field is applied perpendicularly to the layers [Figure 6.2], resulting Na_2O impurities in the glass decomposes into Na+ and O_2- ions. The Na+ has a higher mobility and is lighter. This causes the change in polarity to move the Na+ ions to the back contact and leaving a concentrated layer of O_2- ions at the glass surface [1].This eventually causes the O_2 - to form a strong electric field at the surface allowing the bonding of the graphene flakes and the glass. There are up sides and downsides of a specific method. The up side regarding this method consists is that it is cheap to produce the graphene layers but also at a higher yield. On the other hand, the downside of the process is the higher temperature which may damage the graphene flake. Every procedure has the sweet point in order to get the best results, thus the best parameters for this deposition are the voltage range of between 0.5 and 2KV and a temperature of 200°C for the deposition time of 10-20 minutes. As charged particles are being used over here, we can also dope it in order to get an even greater yield [64].

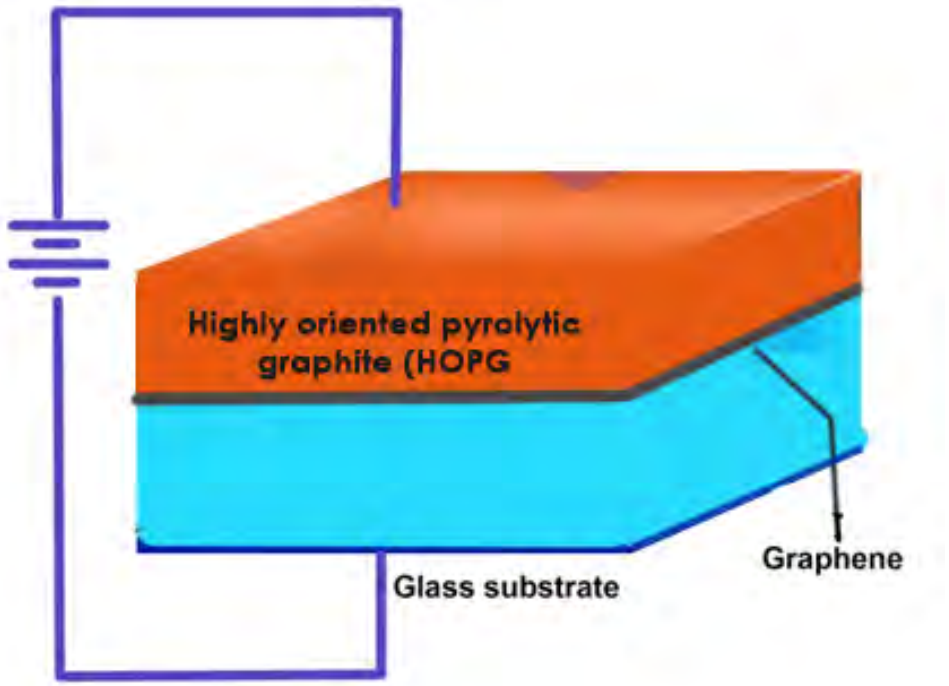


Figure 6.1: Anodic bonding experimental setup

6.3 Chemical Vapour Deposition

The first proposal about dissociating graphene with other materials was a concept which was first introduce in the 1896. [58] The first layer of graphene was grown on nickel, where the researchers saw that the formation of the carbon film on the metal substance was down and caused to segregation and diffusion of metal impurities. [58, 6] After the graphene was discovered, the process was practiced to grow single layer of graphene on metals. [58]To grow graphene films on top of metals especially on nickel and copper were very much popular back in those days, but uneven films formed when nickel was used. [6] Single and multilayer flakes formed over the substrate. On the other hand, polycrystalline copper(Cu) has been used to deposit high quality single layer graphene on a large area upto 95% of the copper surface. [58] Although this sounds fine and all, but there are obviously some challenges to overcome.

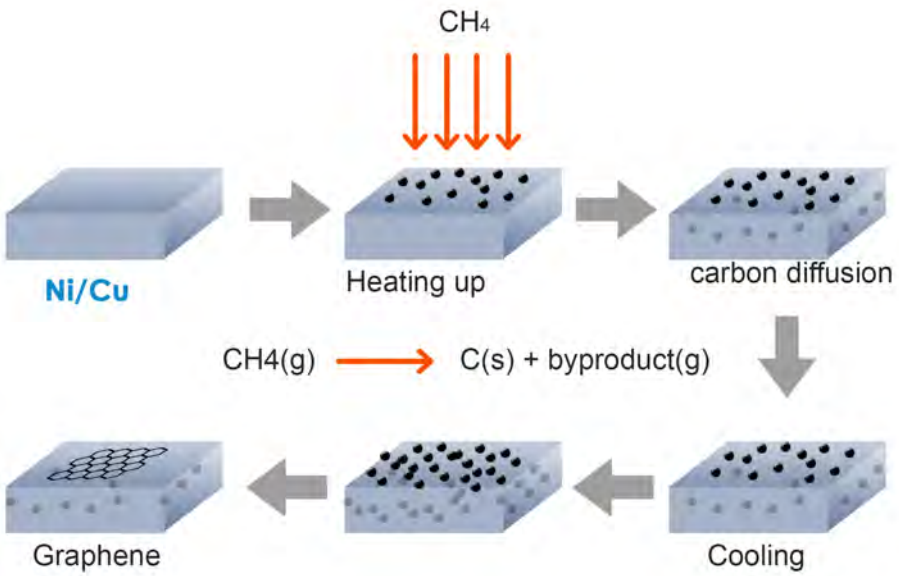


Figure 6.2: The growth of graphene on nickel (Ni) through chemical vapor deposition.

In CVD, in a heated furnace of low vacuum to approximately 1000^oC ,a metal substrate such as copper is put into it. The heat later anneals the copper by increasing its size[5]. Later on, methane and hydrogen gases are passed through the furnace. The surface of the metal substrate and methane is catalyzed due to reacting hydrogen. This eventually causes the carbon atoms from the methane gas to be deposited onto the metal surface due to chemical absorption. Later on, by quickly cooling down the furnace causes the deposition of the carbon layer which eventually aggregate into the bulk graphite, which eventually crystallizes into a contiguous graphene layer on to the surface of the metal [47].

Due to the various materials required for CVD, this method carries impurities. On the other hand, researches has been going on and the impurities can be minimized to create graphene as exfoliated flakes[50]. Due to the difference in thermal expansion between graphene and copper, the graphene from the CVD tends to wrinkle. This is still being researched, although there are possibilities in decreasing this by proper annealing[5]. Most importantly, graphene from CVD is a contiguous film as large as the underlying metal substrate in contrast to random micron sized flakes from the scotch tape method, CVD thus allows graphene to be used as a layer in a solar cell. There are a lot of ways to affect the outcome of the CVD graphene growth run. Since the grown dynamics of the carbon deposition and domain grown are not yet fully understood, finding the proper balance of the controls is a largely experimental task[46] Perhaps the most natural variable to affect a CVD outcome is the amount of the various reaction gases. Increased methane provides more carbon atoms to deposit and more nucleation sites leading to more domains while increasing hydrogen promotes the reaction and also increases the chemical process on the copper

and the surrounding environment. The temperature also affects the rate of reaction as does the speed of changes in temperature. Impurities in the copper substrate detract from the growth process by encouraging nucleation sites and thus hindering the formation of contiguous carbon domains so proper chemical cleaning of copper is essential. Annealing time of the copper also affects the level of impurity for the same reason. The geometry of the growth chamber affects the deposition rate of carbon due to its effects on gas flow patterns, specifically because of turbulent(instead of laminar) flow regimes. Finally, any leaks in the vacuum system further detract from the growth as oxygen from the air oxidizes the copper, making the carbon atoms unable to adhere to the copper surface and ruining the deposition.
Copper is not the only substrate which can be used in graphene CVD, in fact many transition metal can be used. For example, graphene CVD on nickel is somewhat common, and cobalt has also been used[10]. The main differences between metal substrates come from the differences in the metals ability to absorb carbon. Nickel and cobalt absorb more than copper, and this leads to an overabundance of carbon on foils which crystalizes into discrete graphite chunks instead of a single graphene sheet. For that reason nickel and cobalt foil cannot be used and instead thin films(<300nm for nickel must be evaporated onto a silicon substrate before growth[10]. Copper on the other hand attracts less carbon and odes so only at the surface rather than absorbing it into the bulk of the material, since the weak bonds that hold the carbon atoms to the copper can only be formed with open bonding sites at the surface of the lattice. Therefore, copper foils can be used in graphene CVD simplifying the production process as a whole and making it more robust.

6.4 Chemical exfoliation of graphite

This method is very good and it gives a very good yield. The main objective of the process in order to get the graphene is to separate the layers of graphite. This can be obtained in a number of ways, which includes chemical modification of graphite(Ex. Graphene Oxide) followed by separation. Some other methods include interacting small molecules between the layers(Ex. Liquid phase exfoliation). Every method has its own advantages and disadvantages.

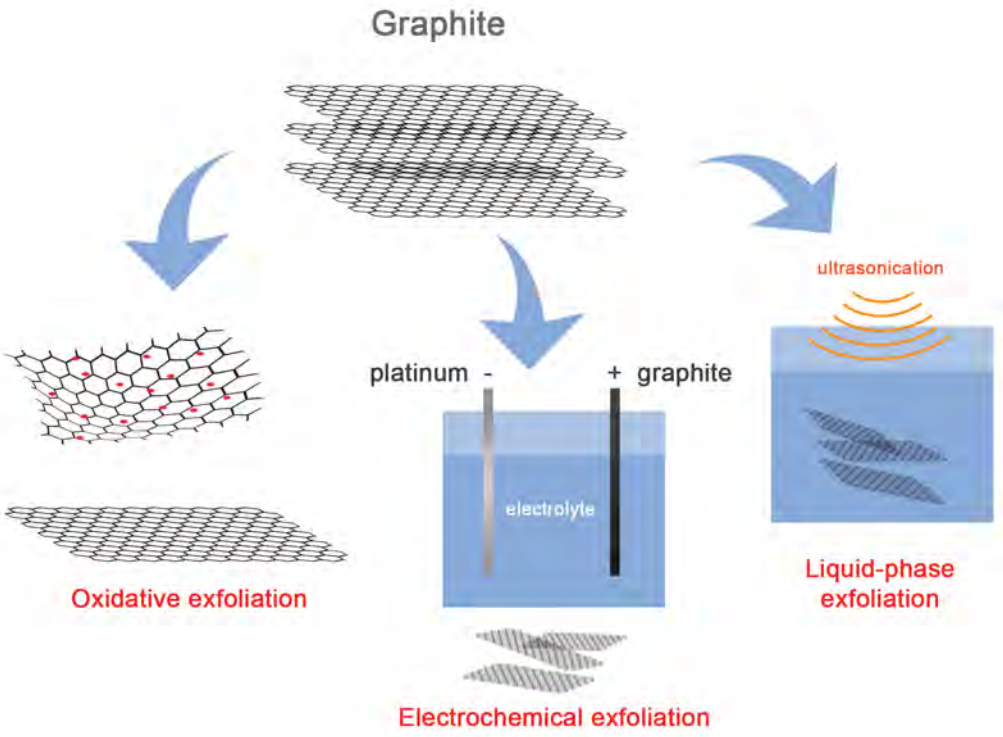


Figure 6.3: oxidative exfoliation, electrochemical exfoliation and Liquid-phase exfoliation are the most common way of producing graphene

7

Conclusion

This paper provides survey of interconnects used in integrated circuits where graphene and CNT can be used for the replacement of Cu. Graphene and CNT have schottkey barrier height problem apart from that graphene and CNT have lower resistance, greater themal conductivity and less electromigration. These have made it easier to replace Cu with it. Copper has increased resistance and electromigration problem which can cause short circuit resulting in a system failure. As the devices are getting smaller copper cannot cope with the miniaturization. Graphene and CNT production has various ways. Each productivity ways has their own advantages and disadvantages. These challenges are required to be resolved before adapting them as on-chip interconnect in ICs by the industry. As the technology node is shrinking, according to the need, the electrical properties of ballistic conduction, ability to handle high current densities(up to $10^{10} A/cm^2$) and high thermal conductivity make CNTs and graphene far superior to Cu.

7.1 Summary of the Contribution

First we demonstrated the different kinds of interconnect and then studied the bottlenecks copper is facing in nanoscale interconnects. We found out that the resistivity of copper is increasing when its thickness becomes less than its mean free path. Since scaling down of devices leads to shrink the thicknesses of the interconnect wire, copper is not capable to keep pace with this shirnking.In this aspect 1D and 2D material such as Carbon nanotube and Graphene can play industry standard role in terms of thickness delivering the high performance benefit in nanoscale. Being nanometer dimension, both of these materials my outsail copper in terms of resistivity.
In less than 40 nm node interconnect material need to withstand a large current density in order to deliver power to devices. Copper is facing structural injuries in current density of$10^6 A/cm^2$ [81]whereas graphene and carbon nanotube can withstand current densities up to $10^9 A/cm^2$[81]As a result there is no worry of electromigration with these materials but in copper electromigration takes place making the IC short circuited and less reliable. And for the reliability of Graphene wire, research has been shown that 100 um Uncapped graphene wire stressed at $20 MA/cm^2$have 6 hours of mean time to fall which is 15%better than capped copper wire[21]. By this we can demonstrate how reliable graphene is for interconnects.
Graphene and Carbon Nanotubes have thermal conductivity in thousand range which much higher than copper. That describes the potential use of these materials for intercpnnects.

After reviewing the scientific research papers it can be say that for future interconnect graphene and carbon nanotube based interconnect can replace copper with increased performance and reliability and also with much smaller dimensions. Graphene and carbon nanotube based interconnects is the future.

7.2 Required study for Graphene and Carbon Nanotube based interconnects

We have demonstrated that how graphene can outperform copper but a future study is needed with the capping material for graphene interconnect. And for carbon nanotubes, The energy gap of carbon nano-tube has an inverse relationship with its diameter. That's why small diameter SWNT have to be decreased while its growing as this can reduce the conduction of the bundles and vias architectures. Another study is needed to reduce the schottkey barrier height of graphene with differenet semiconductor material. After resolving this challenges graphene and carbon nanotube can be used as nanoscale interconnects.

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