Multi-Level Inverter Design and Topologies

A Thesis

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Declaration

We do hereby declare that the thesis titled "Multi-level inviter design and topologies" is submitted to the Department of Electrical and Electronics Engineering of BRAC University in partial fulfillment of the Bachelor of Science in Electrical and Electronics Engineering. This is our original work and was not submitted elsewhere for the award of any other degree or any other publication.

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ABSTRACT

AC power is most widely used power sources both in household appliances and industrial machines. But when AC supply is not available for a certain period of time at that time we need to convert stored DC power in to AC power. This issue can be resolved by the power electronics equipment called as an Inverter. Basically inverters are circuits that convert DC input voltage to a symmetric AC output voltage by which both magnitude and frequency can be controlled. Different types of inverters are available in the market for different purposes. In this paper we are going to represent a brief review of different multilevel inverter topologies and our proposed single phase cascaded inverter with transformer. We designed a two stage and a three stage cascaded inverter with transformer. In the paper we showed our proposed circuit's output wave shape and how their FFT analysis, PMW modulation technique controls the amplitude at desired frequency as well as how it decreases the harmonic distortions.

Keywords: Multi-Level Inverter topologies (MLI), Pulse width modulation (PWM), Total harmonic distortion (THD).

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Abbreviations

MLI-Multi-Level Inverter

THD- The Total Harmonic Distortion

VSI -Voltage Source Inverter

CPLD-Complex Programmable Logic Device

DSP-Digital Signal Processor

FPGA-Field-Programmable Gate Array

PWM -Pulse Width Modulation

EMC-Electromagnetic Compatibility

SPWM -Sinusoidal Pulse Width Modulation

SHE -Selective Harmonic Elimination

SVM -Space Vector Modulation

CM-Common-Mode

SPWM-Sinusoidal Pulse Width Modulation

SVM-Space Vector Modulation

FACTS-Flexible AC Transmission System

SDCS-Each Separate DC Source

SVC -Space Vector Control

CB-PWM -Carrier Based Pulse Width Modulation

DFT- Discrete Fourier Transform

SDC-Separate DC Sources

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CHAPTER 1

INTRODUCTION

1.1Motivation

The idea of using different small voltage levels to perform power conversion was presented more than twenty years back. Favorable circumstances of this multilevel approach incorporate great power quality, great Electro Magnetic Compatibility (EMC) [1], low switching losses and high voltage capacity. Already, a large portion of the exploration work towards multilevel inverters has been focused on the improvement of pulse width modulation utilizing space vector pulse width modulation, sine PWM [1] with single transporter and single reference, multicarrier PWM method with single reference and with corrected double reference. Up until now, execution of multilevel inverters topology with its qualities procedure has not yet been tended to. This examination work broadens the investigation of three level inverter and three stage multilevel inverter's (in future research) execution utilizing single and double references multicarrier are talked about and physically performed (software base).

1.2 Objectives

Our objective is to discuss on the different topologies of inverters. We want to design a multistage inverter circuit with a controlled amplitude at desired frequency and decrease the harmonic distortion by harmonic elimination.

1.3 Background

Multilevel inverters have been widely accepted for high-power high-voltage applications. Their performance is highly superior to that of conventional two-level inverters due to reduced harmonic distortion, lower electromagnetic interference, and higher DC voltages. However, it has some disadvantages such as increased number of components, complex pulse width modulation control method, and voltage-balancing problem. In this paper, we tried to overcome with these prejudice with our inverter circuit and its switching technique to generate modified sin wave using a new concept, which requires less power electronics components comparing to the conventional inverter circuits. A PSIM based model is developed for Single and cascaded output

voltage. THD [1] of the output voltage is reduced with the proposed circuit. Moreover for cascaded inverter, the requirements of diodes and capacitors are also reduced.

1.4 Organization

In chapter two Topologies of different multilevel. Inverters for example, such that diode clamped, flying capacitor and H-bridge are discussed. We also discussed about the cascaded inverter system in this chapter. In Chapter three Regulation systems for example, space vector. PWM, specific harmonic disposal, sinusoidal PWM are also considered. Their relevance for the different topologies is additionally focused in this part. In chapter four we have confer about our proposed inverter circuit and its switching technique to generate modified sin wave using a new concept, which requires less power electronics components comparing to the conventional inverter circuits. In chapter five we wrapped up our whole research and further work scope on this efficient scheme to take part in developing power electronics world by our mare contribution.

CHAPTER 2

INVERTER TOPOLOGIES

2.1 Introduction:

This chapter gives the brief description of conventional inverters, with their points of interest and drawbacks. Topologies of different multilevel, inverters, for example, diode clasped, flying capacitor and fell H-connect with their ideas are examined [2]. Regulation strategies, for example, space vector PWM [1], particular consonant disposal and sinusoidal PWM are exhibited and their materialness for the distinctive topologies is additionally examined in this section.

2.2 Conventional Two Level and Three Level Voltage Source Inverters:

Switching mode DC to AC inverters deliver a sinusoidal AC yield voltage whose extent and recurrence can be controlled. They are generally utilized as a part of the territory of AC acceptance engine drives. Half extension inverter is the least difficult topology which delivers the two level square wave yield voltage waveform. Circuit design of half scaffold topology is given in Figure2.1. To stay away from shoot through blame, either switch S1 or S2 is turned ON at an opportunity to give a heap voltage, VAO of +VS/2 as appeared in Figure 2.1(a). To finish one cycle, S1 turned OFF and S2 is turned ON to give a load voltage, VAO of - VS/2.

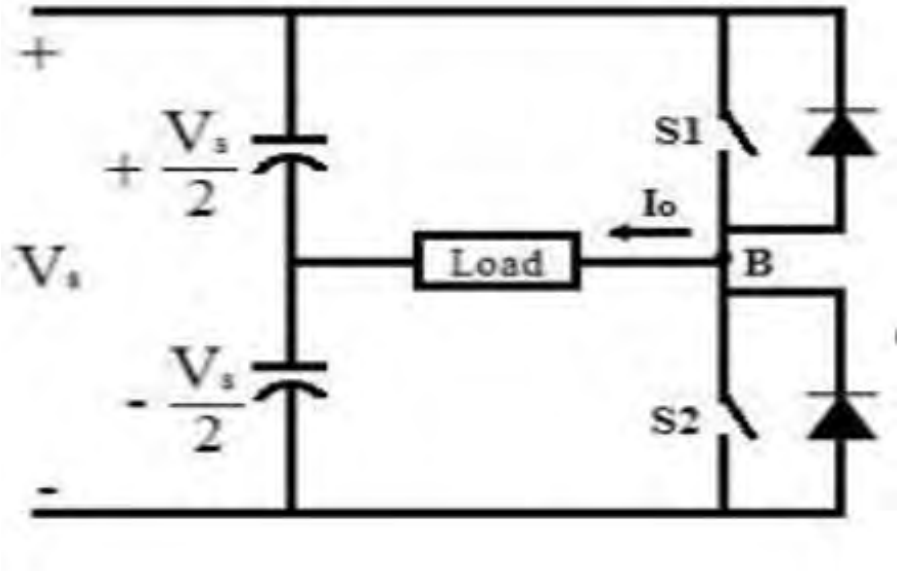

Fig 2.1(a): Half bridge configuration

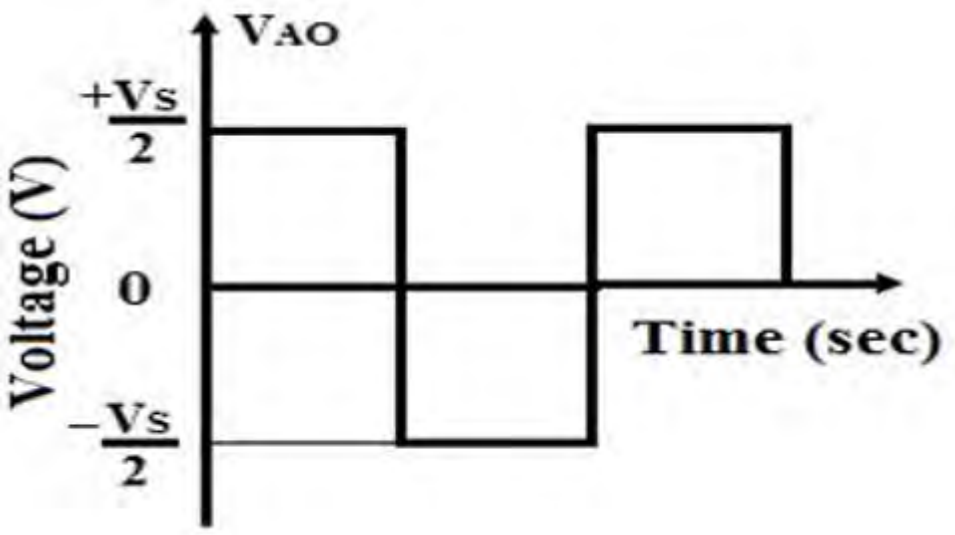

Figure 2.1(b): Output voltage waveform

Figure 2.1: Half bridge inverter with ideal switches and diodes, source: [1]

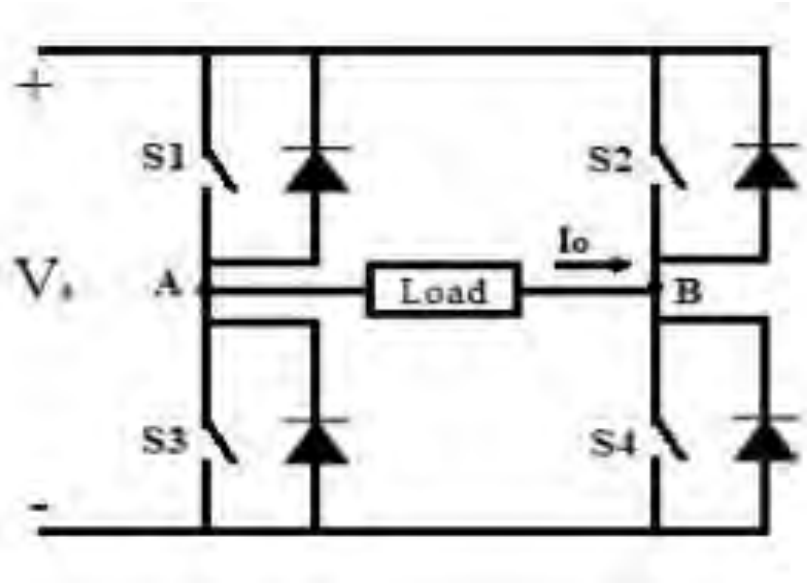

Fig 2.2(a): Full bridge configuration

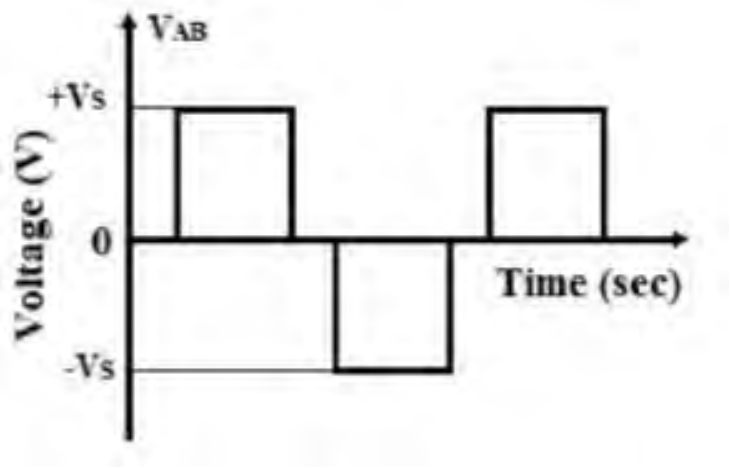

Fig 2.2(b): Output voltage waveform

Figure 2.2: Single phase full bridge ideal inverter, source: [1]

Circuit arrangement of full extension topology is given in 2. This topology is utilized to combine a three level square wave yield voltage waveform. The three conceivable levels are given in Table 2.1. Neither S1, S3 nor S2 and S4 ought to be shut in the meantime. Provided that this is true, a short out will happen over the DC source.

Conducting Switches	**Load Voltage VAB**
S1 & S4	+Vs
S2 & S3	-Vs
S1 & S2 or S3 & S4	0

Table 2.1: Load voltage with corresponding conducting switches, source: [1]

The entire DC voltage appears across each switch when it is OFF. This will be greater than the voltage rating of the individual devices. The devices will not automatically share the voltage in the OFF state because of the differences in their leakage currents. High value of parallel resistors can be used to overcome this static sharing problem. More seriously, the devices will not share the voltage during switching due to variations in switching speed. Special gate drive techniques and special snubber is required for dynamic sharing. Two level output causes very large voltage steps on the load which will create a problem for motor insulation. Harmonic content of the output voltage is larger for high switching frequency. On the flip side, classical inverters too have finite advantages. They are, Standard PWM [1] techniques can be used. Number of power circuit components is less as compared to other inverter circuits. Redundancy can be incorporated to improve reliability by using more series devices than actually required. From the above discussion, it is clear that the conventional inverter have many drawbacks than merits. So alternative solution to meet the high power demand is through multilevel inverter concept.

2.3 Multilevel Inverter:

Numerous industrial applications have begun to use high power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt control levels. For a medium voltage matrix, it is troublesome to associate just a single power semiconductor switch specifically. Thus, a multilevel inverter structure has been presented as an option in medium and high power applications [2]. With this sort of inverters, enhancements in the consonant nature of the yield voltage can be accomplished. Multilevel inverter achieves high power appraisals, as well as empowers the utilization of sustainable vitality sources. Sustainable power sources, for example, photovoltaic, wind and power modules can be effectively interfaced to a multilevel inverter framework for medium what's more, high power applications. Multilevel inverter creates a coveted AC voltage waveform from a few levels of DC voltages. These DC voltages might be or may not be measure up to. Air conditioning voltage created from these DC voltages is of ventured waveform. One downside of utilizing multilevel inverter is to inexact sinusoidal waveforms from ventured waveform. The staircase waveform delivered by the multilevel inverter contains sharp advances. Fourier arrangement hypothesis makes clear that this marvel brings about sounds, notwithstanding the basic recurrence of the sinusoidal waveform. The power nature of the power framework is influenced by the sounds created on the AC side.

The power nature of the multilevel inverter is enhanced by playing out the power change in little voltage steps. Multilevel inverter broadly replaces the customary two level three stage Voltage Source Inverter (VSI) [2] by its execution, for example, bring down exchanging push (dv/dt) and bring down THD [2] on output voltage. The multilevel inverters begin from three levels. As the quantity of levels achieve endlessness, the output THD approaches zero. The quantity of the achievable voltage levels is constrained by voltage unbalance issues, voltage clamping requirement, circuit layout and packaging constraints. A multilevel inverter has several advantages over a conventional two level inverter that uses high switching frequency PWM.

The attractive features of a multilevel converter can be briefly summarized as follows:

Multilevel inverters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses. Therefore electromagnetic compatibility problems can be reduced. Multilevel inverters produce smaller CM [2] voltage; Therefore, the stress in the bearings of a motor connected to a multilevel inverter drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation techniques. Multilevel inverters will draw input current with low distortion. Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

The principle disadvantage of multilevel inverters is that the quantity of switches increments with the quantity of levels. In beginning times of multilevel inverters, advancement of control hardware for expansive number of energy switches was a huge issue. In any case, constant advancement of CPLD, DSP what's more, FPGA gadgets effectively explained this burden. Other disadvantage of this inverter is the necessity of different quantities of DC voltage sources, for the most part gave by capacitors. Adjusting the voltage sources amid operation under various load conditions is an essential test. Despite these disadvantages, presenting multilevel inverters will diminish exchanging misfortunes happened in the influence gadget. By contrasting and two level inverters, littler size channel is required for the disposal of sounds. This diminishes the inverter weight, measurement and cost. Numerous multilevel inverter topologies have been

proposed amid the last two decades. Contemporary research has advanced novel inverter topologies and one of a kind tweak plans. Also, three diverse major multilevel inverter structures have been accounted for in the writing. They are,

1. Diode clamped /Neutral clamped Multilevel Inverter
2. Flying capacitors /Capacitor clamped Multilevel Inverter
3. Cascaded H-bridge Multilevel Inverter

Abundant modulation techniques and control paradigms have been developed for multilevel inverters such as Sinusoidal Pulse Width Modulation (SPWM) [2], Selective Harmonic Elimination (SHE-PWM) [2], Space Vector Modulation (SVM) [2] and others. Multilevel inverters replace the existing two level inverters from the applications such as power supplies, traction drive systems, industrial medium-voltage motor drives, utility interface for renewable energy systems and Flexible Alternating Current Transmission System.

2.4 Multilevel Notion:

The idea of multilevel inverters has been presented since 1975 [3]. Be that as it may, the basic idea of a multilevel inverter to accomplish high control is to utilize a progression of energy semiconductor switches with a few low voltage DC sources to perform control change by combining a staircase voltage waveform. One stage leg of multilevel inverter is appeared in Figure 3. In this schematic outline, operations of semiconductors are appeared by a perfect switch with a few states. The exchanging calculations of switches and compensation of them permit the expansion of the capacitor voltages as brief DC voltage sources, while the semiconductors ought to withstand constrained voltages of capacitors.

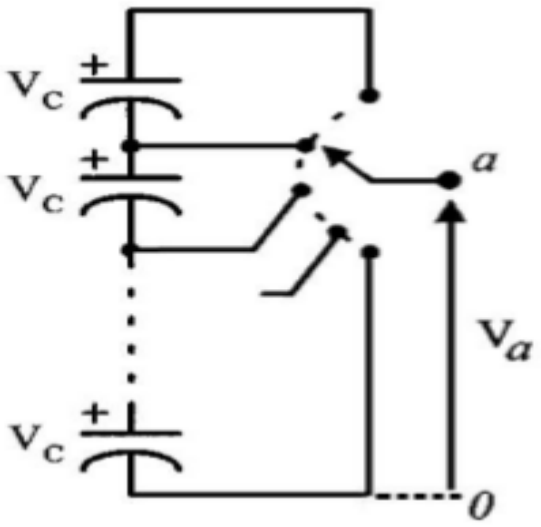

Figure 2.3: One phase leg of a multilevel inverter, source: [3]

Nearly for the three decades, multilevel inverters are being used in the world of power electronics. They are named by the number of voltage levels they generate and the different topologies they have. Usually the number of output voltage levels is odd instead of even. It means that the definition of a zero voltage level in the output of inverter, like in three level or in five level inverters, makes it more sinusoidal with less harmonics.

2.4.1 Diode Clamped Multilevel Inverter:

Three phase eleven level diode clamped inverter is shown in Figure 2.4. Each phase of the inverter shares a common DC bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is Vdc and the voltage stress across each switching device is limited to Vdc through the clamping diodes.

Switching states of diode clamped multilevel inverter is given in Table 2.2.

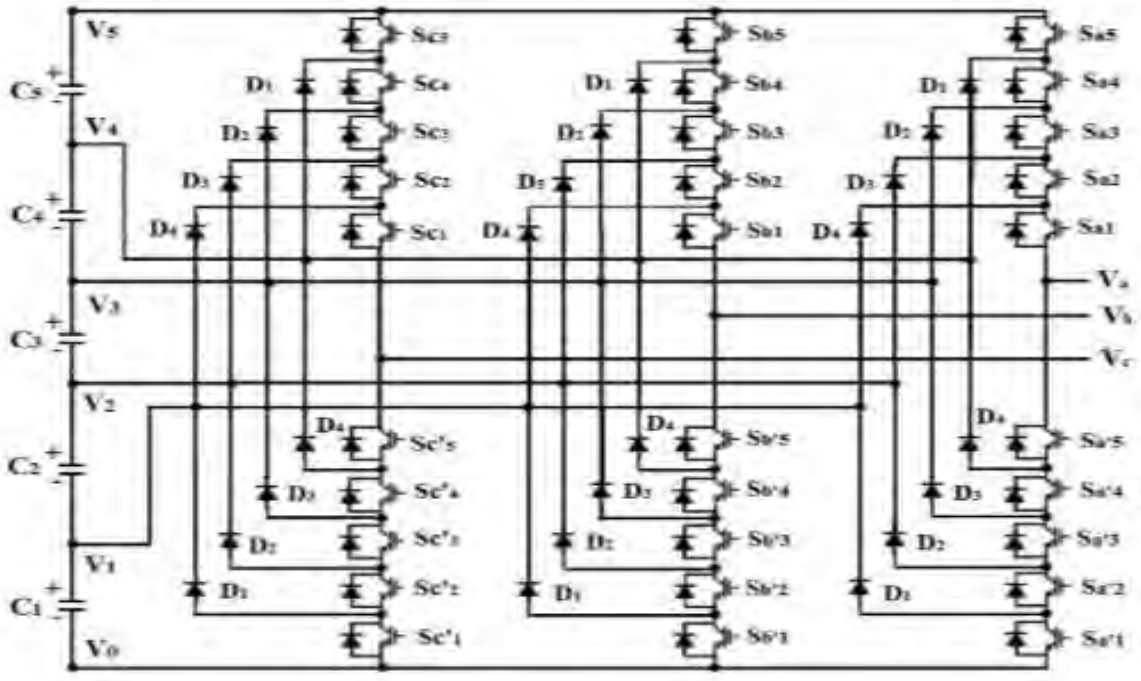

Figure 2.4: Three phase eleven level structure of a diode clamped inverter, source: [3]

Voltage Va0	**Switch State**									
	Sa5	**Sa4**	**Sa3**	**Sa2**	**Sa1**	**Sa'5**	**Sa'4**	**Sa'3**	**Sa'2**	**Sa'1**
V5=5Vdc	1	1	1	1	1	0	0	0	0	0
V4=4Vdc	0	1	1	1	1	1	0	0	0	0
V3=3Vdc	0	0	1	1	1	1	1	0	0	0
V2=2Vdc	0	0	0	1	1	1	1	1	0	0
V1=1Vdc	0	0	0	0	1	1	1	1	1	0
V0=0	0	0	0	0	0	1	1	1	1	1

Table 2.2: Diode clamped eleven level inverter voltage levels and corresponding switch states, source: [3]

Table 2.2 lists the output voltage levels possible for one phase of the inverter with the negative DC rail voltage V0 as a reference. Switch state condition one (1) means the switch is ON, and zero (0) means the switch is OFF. Each phase has five complementary switch pairs such that turning ON one of the switches of the pair requires that the other complementary switch be turned OFF. The complementary switch pairs for phase leg-A are (Sa1, Sa'1), (Sa2, Sa'2), (Sa3, Sa'3), (Sa4, Sa'4) and (Sa5, Sa'5). The switches that are ON for a particular phase leg is always adjacent and in series. For an eleven level inverter, a set of five switches are ON at any given time. The resulting line voltage is an eleven level staircase waveform as shown in Figure 2.5. The line voltage Va-b consists of a phase leg-A voltage and phase leg-B voltage. This means that NL level diode clamped inverter has NL level output phase voltages and a (2NL -1) level output line voltages.

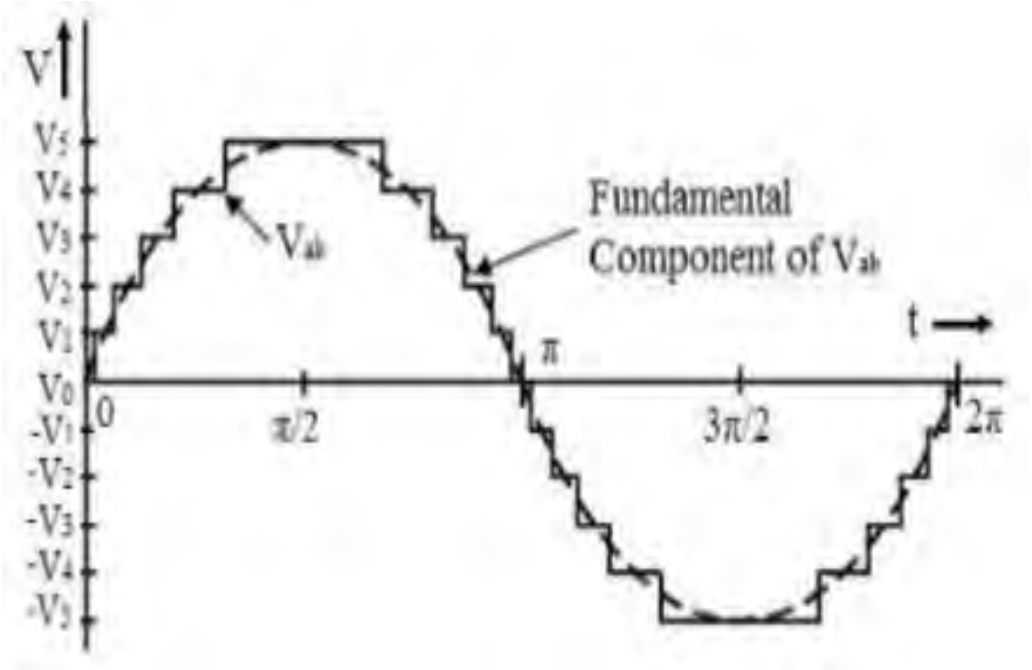

Figure 2.5: Line voltage waveform of eleven level diode clamped inverter, source: [3]

Major advantages of diode clamped multilevel inverter are listed as follows:

When the number of levels is high enough, the harmonic content is low enough to avoid the need for filters. Inverter efficiency is high because all devices are switched at the fundamental frequency. The control method is simple.

Disadvantages of the diode clamped multilevel inverter can be listed as follows:

Excessive clamping diodes are required when the number of levels is high. It is difficult to control the real power flow of the individual converter.

2.4.2 Flying Capacitor Multilevel Inverter:

The structure of this inverter is like that of the diode clipped inverter. Rather than utilizing clipping diodes, the inverter utilizes capacitors in their put. The circuit topology of the flying capacitor multilevel inverter is appeared in Figure 2.6 [3]. This topology has a stepping stool structure of DC side capacitors. The voltage on every capacitor varies from that of the following capacitor. The voltage increase between two nearby capacitor legs gives the measure of the voltage ventures in the yield waveform. One favorable position of the flying capacitor based inverter is that it has redundancies for inward voltage levels. Not at all like the diode braced inverter, the flying capacitor inverter does not require the greater part of the switches that are ON (leading) in a continuous arrangement. In addition, the flying capacitor inverter has stage redundancies, though the diode cinched inverter has just line-line redundancies. These redundancies permit a decision of charging and releasing particular capacitors and can be fused in the control framework for adjusting the voltages over the different levels.

In addition to the (NL-1) DC link capacitors, the NL-level flying capacitor multilevel inverter will require (NL -1) × (NL -2)/2 auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches. One application proposed in the literature for the multilevel flying capacitor is static var generation.

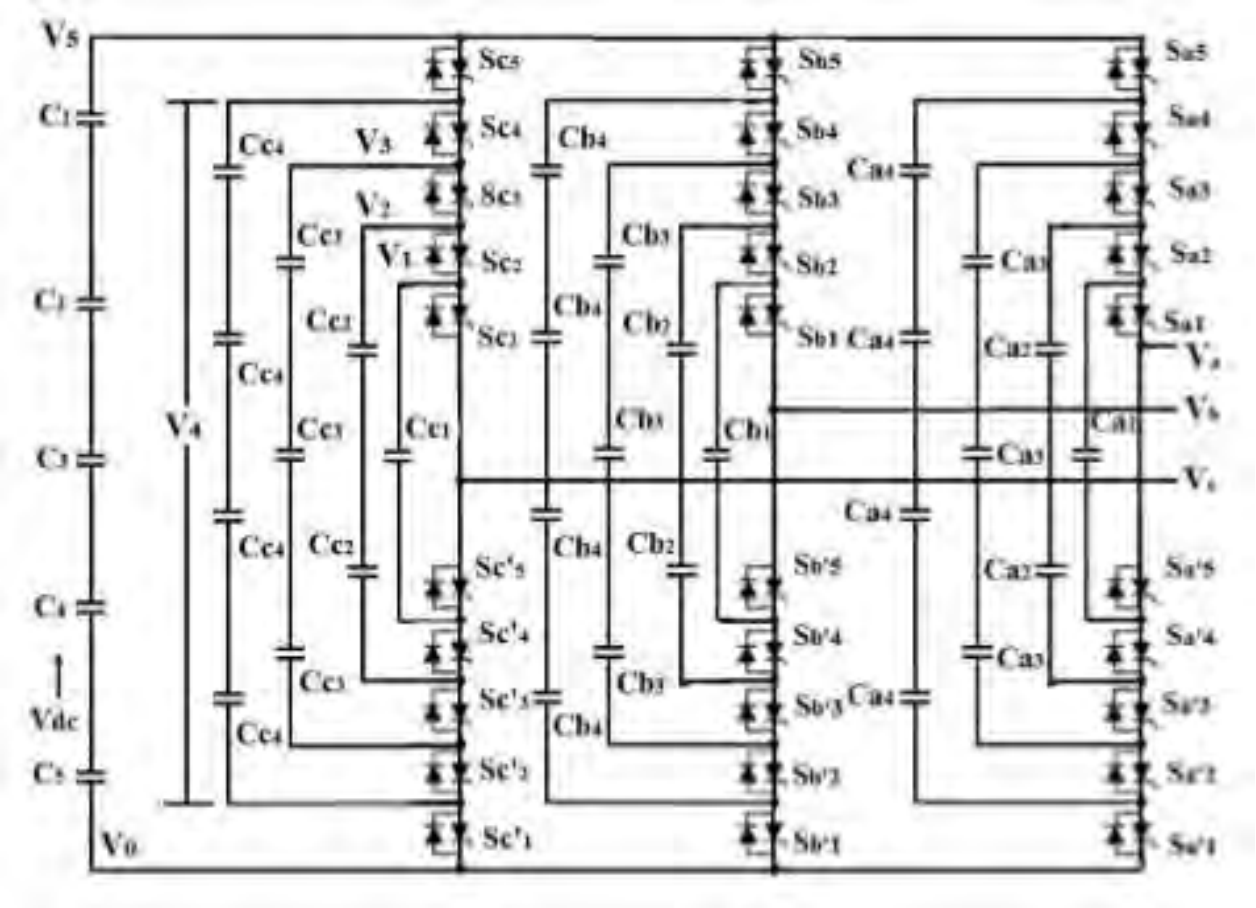

Figure 2.6: Three phase eleven level structure of a flying capacitor inverter, source: [3]

Advantages of the flying capacitor multilevel inverter are summarized as follows:

Provides switch combination redundancy for balancing different voltage levels. Real and reactive power flow can be controlled. The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

On the flip side, flying capacitor multilevel has some disadvantages. They are,

Control is complicated to track the voltage levels of all the capacitors. Also, pre-charging of all the capacitors to the same voltage level and startup are complex. Switching utilization and efficiency are poor for real power transmission. The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode clamped converters. Packaging is also more difficult in inverters with a large number of levels.

2.4.3 Cascaded H-bridge Multilevel Inverter:

Each Separate DC Source (SDCS) [4] is associated with a solitary stage full scaffold or H-connect inverter. A solitary stage structure of eleven level fell inverter is shown in Figure 2.7. Every inverter level can produce three distinctive voltage yields, +Vdc, 0 and – Vdc by interfacing the DC source to the AC yield by various mixes of the four switches, S1, S2, S3 and S4. To get +Vdc, switches S1 and S4 are turned ON, though – Vdc can be gotten by turning ON switches S2 and S3. By turning ON S1 and S2 or S3 and S4, the yield voltage of zero is gotten. The AC yields of various full scaffold inverter levels are associated in arrangement with the end goal that the combined voltage waveform is the aggregate of the inverter output. Phase voltage waveform for eleven level cascaded H-bridge inverter is shown in Figure 2.7. The number of output phase voltage levels (NL) [4] in a cascaded inverter is defined by NL = 2s+1, where s is the number of separate DC sources. Output phase voltage Van is given in Equation 1.

Van = va1 + va2 + va3 + va4 + va5 …… (1)

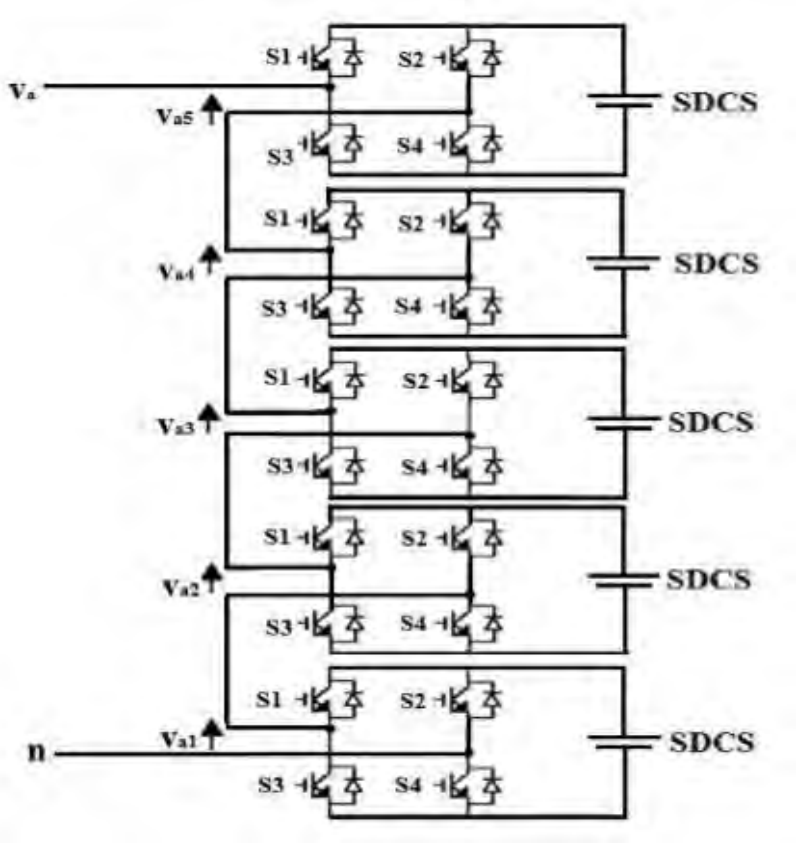

Figure2.7: Cascaded H-bridge eleven level inverter, source: [4]

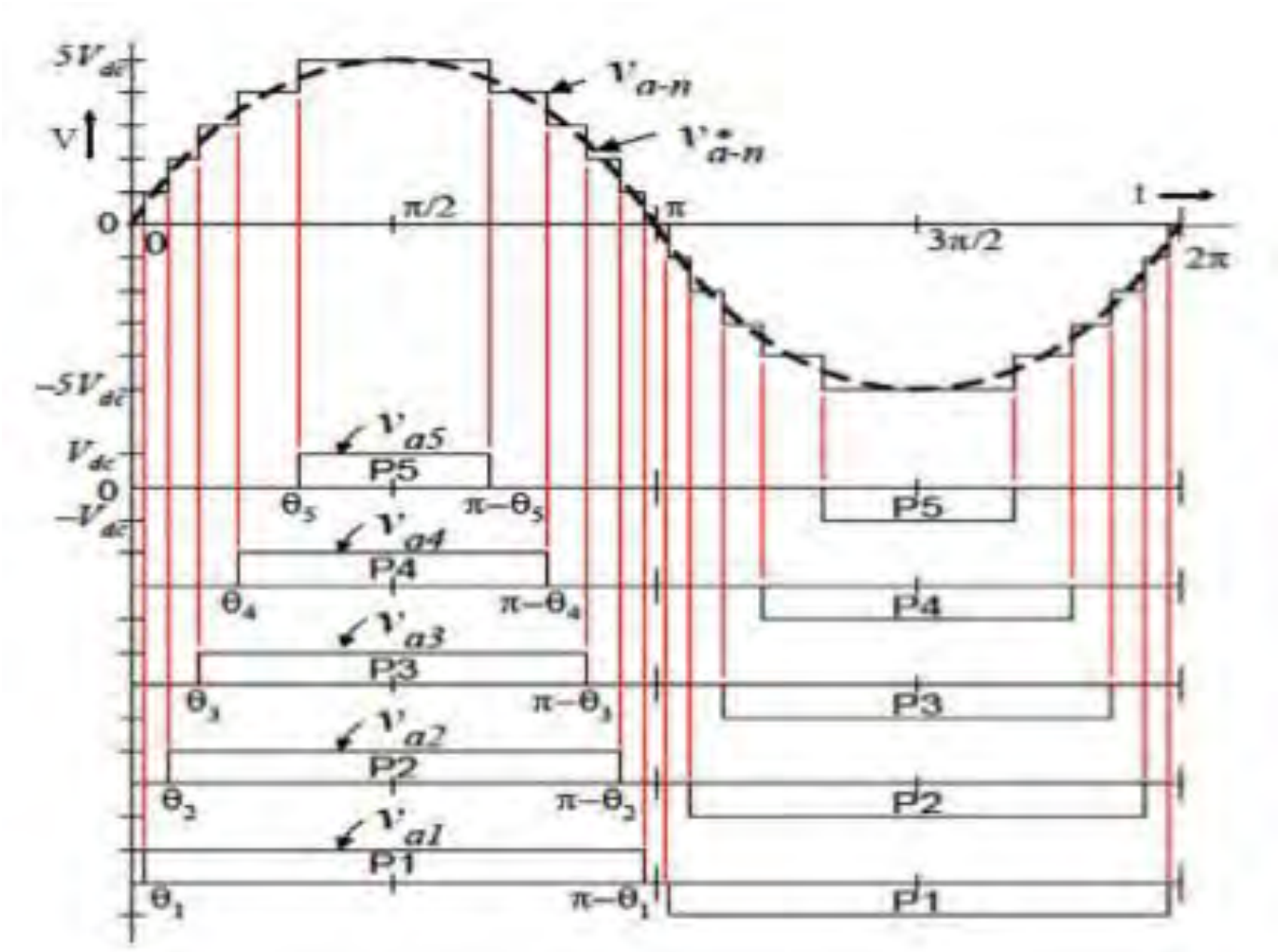

Figure 2.8: Output phase voltage waveform of eleven level cascaded inverter, source: [4]

Major advantages of the cascaded inverter can be summarized as follows:

The number of possible output voltage levels is more than twice the number of DC sources (NL = 2s + 1) [4]. The series of H-bridges makes for modularized layout and packaging. This will make the manufacturing process to be done more quick and cheap.

Major disadvantage of the cascaded inverter is given below:

It needs separate DC sources for real power conversions, thereby limiting its applications.

2.5 Component Requirements:

Component requirements of diode clamped, flying capacitor and cascaded H-bridge multilevel inverters for number of levels is given in Table 2.3. From the Table 2.3, cascaded inverter requires the least number of components and has the potential for utility interface applications because of its capabilities for applying modulation and soft-switching techniques.

Components	**Inverter Type**		
	Diode Clamped	**Flying Capacitors**	**Cascaded H-bridge**
Main Switching devices	(NL-1)*2	(NL-1)*2	(NL-1)*2
Main diodes	(NL-1)*2	(NL-1)*2	(NL-1)*2
Clamping Diodes	(NL-1)* (NL-2)	0	0
DC bus capacitors	(NL-1)	(NL-1)	(NL-1)/2
Balancing capacitors	0	(NL-1)* (NL-2)/2	0

Table 2.3: Components required for different MLI topologies, source: [4]

The switching devices do not encounter any voltage-sharing problems. Thus, multilevel inverters can without much of a stretch be connected for high control applications. The framework kV rating can be reached out past the breaking points of an individual gadget through the voltage clipping methods. In this way, diode lipped inverters are utilized more in high power engine drive applications. The interesting component of the multilevel inverter structures is their

capacity to scale up the kVA rating and furthermore to enhance the consonant execution in the yield voltage. By considering the cost of semiconductor switches and latent parts, converter misfortunes and effortlessness of regulation plans, fell H-connect inverter is likewise a best decision for medium and high power applications.

2.6 Conclusion:

All in all in this chapter we discussed about different inverter topologies and their construction. Different inverters have different advantages and disadvantages. From this chapter one can have an idea about different topologies of inverters.

CHAPTER 3

MODULATION TECHNIQUES

3.1 Modulation Techniques:

Balance is the way toward exchanging the power electronic gadget in a power converter starting with one state then onto the next. All balances are gone for producing a ventured waveform that best approximates a discretionary reference motion with flexible sufficiency, recurrence and stage crucial segment that is normally sinusoidal in enduring state. Every topology has diverse changing arrangement to accomplish summoned yield voltage. Tweak methodologies are in charge of combining reference control signals and for keeping all voltage sources adjusted. The prerequisites of multilevel adjustment calculation are as per the following. Voltage quality ought to be great Secluded outline Concurrent exchanging of different voltage levels isn't permitted. Exchanging recurrence of energy gadgets ought to be limited. Power modules should share the heap similarly. Control calculation ought to be straightforward. Usage cost ought to be low. In numerous modern applications, the yield voltage of inverters ought to be controlled to defeat the adjustments in input voltage and to meet the need of voltage/recurrence control.

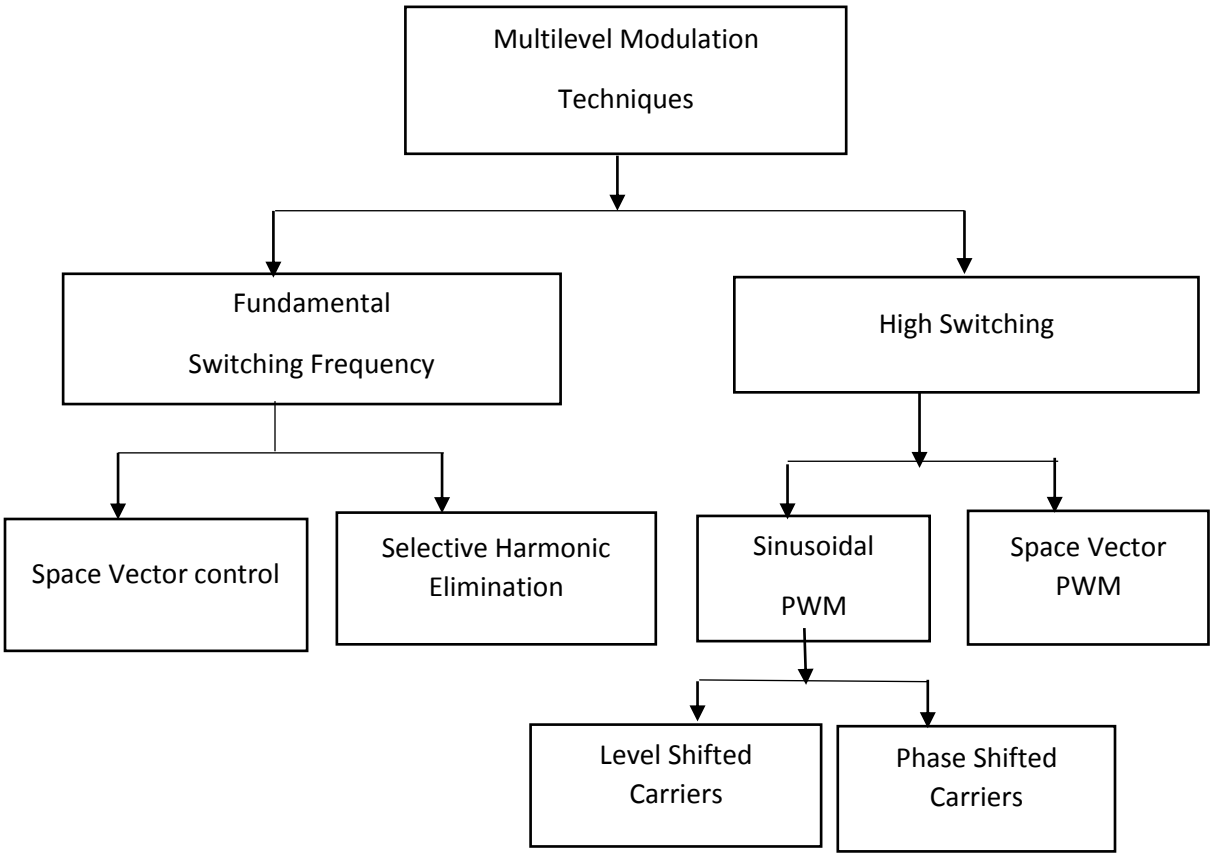

Figure 3.1: Classification of modulation techniques, source: [5]

Clearly sounds in the yield voltage rely upon the chose balance system. Utilizing more number of semiconductor gadgets and exchanging redundancies, bring a larger amount of unpredictability in multilevel topologies, when contrasted and a two level inverter.

In any case, this many-sided quality can be utilized to enhance the adjustment procedure, for example, limiting the exchanging recurrence, diminishing the basic mode voltage or adjusting the DC interface voltages. The adjustment techniques utilized as a part of multilevel inverters can be grouped as indicated by exchanging recurrence as appeared in Figure 3.1.Techniques that work with high exchanging frequencies have numerous recompenses for the power semiconductors in a single cycle of the key yield voltage. An extremely well known strategy in mechanical applications is the work of art transporter based Sinusoidal PWM that uses the stage moving system to lessen the music in the heap voltage. Another fascinating option is the SVM methodology [5], which has been used in three level inverters.

<table>
<tr><th rowspan="2">Switching Frequency</th><th colspan="2" rowspan="2">Modulation Techniques</th><th colspan="3">Multilevel Topology</th></tr>
<tr><th>NPC</th><th>FC</th><th>CHB</th></tr>
<tr><td rowspan="4">High Frequency</td><td colspan="2">SVM</td><td>Applicable</td><td>Applicable</td><td>Applicable but not recommended</td></tr>
<tr><td rowspan="2">SPWM</td><td rowspan="2">Level Shifted PWM</td><td rowspan="2">Not Applicable</td><td rowspan="2">Applicable</td><td rowspan="2">Applicable</td></tr>
<tr><td>Phase Shifted PWM</td></tr>
<tr><td rowspan="2">Fundamental Frequency</td><td colspan="2">SHE</td><td>Applicable</td><td>Applicable</td><td>Applicable</td></tr>
<tr><td colspan="2">SVC</td><td>Applicable but not recommended</td><td>Applicable</td><td>Applicable</td></tr>
</table>

Table 3.1: Applicability of modulation techniques for different multilevel inverter topologies, source: [5]

Strategies that work with low exchanging frequencies for the most part perform maybe a couple substitutions of the power semiconductors amid one cycle of the yield voltages, producing a staircase waveform. In view of the exchanging recurrence and adjustment procedures, their materialness for diverse kind of multilevel inverters are given in Table 4. It must be noticed that lower exchanging recurrence generally implies bring down exchanging misfortune and higher proficiency. Delegates of this family are the multilevel particular symphonious end and the Space Vector Control (SVC) [5]. It is discovered that SVM and SHE [5] are the most generally utilized regulation methods for every one of the sorts of multilevel inverters. In continuation of the work done in the previous couple of decades on exchanging recurrence connected to these multilevel inverters.

3.2 Space Vector PWM:

Each multilevel inverter has several switching states which generate different voltage vectors and can be used to modulate the reference. In SVM, the reference signal is generated from its closest signals. Some vectors have redundant switching states, meaning that they can be generated by more than one switching state. This feature is used to balance the capacitor voltages. Multilevel SVM must manage this behavior to optimize the search for the modulating vectors and apply an appropriate switching sequence. A conceptually different control method for multilevel converters, based on the space-vector theory, has been introduced, which is called space vector control.

3.3 Selective Harmonic Elimination:

The prevalent particular consonant disposal technique is additionally called central exchanging recurrence technique which depends on the consonant end hypothesis. The multilevel principal exchanging plan naturally gives the chance to dispose of certain lower arrange music by differing the circumstances at which certain switches are turned ON and killed. A staircase yield voltage waveform is produced by turning ON and OFF the exchanging gadgets in the multilevel inverters

once amid one major cycle. This decreases the exchanging misfortunes in the gadgets. In this strategy, each switch is turned ON and killed once in an exchanging cycle and exchanging points are normally picked in light of particular symphonious disposal or, then again minimization of THD in the yield voltage. Two approaches to take out lower order harmonics are;

i) By increasing the switching frequency of SPWM and SVM in case of two level inverters or in multicarrier based phase shift modulation for multilevel inverters.
ii) ii) By computing the switching angles using SHE techniques.
iii) The first strategy for disposing of low recurrence sounds is constrained by the exchanging misfortunes and the accessibility of the voltage steps. SHE techniques comprises the mathematical modelling of output waveform and solving them for switching angles based on the amplitude of the fundamental wave of the output voltage, the order and number of the eliminated harmonics. Thus, the lower order harmonics are either eliminated or minimized while the higher order harmonics are filtered out in selective harmonic elimination method. Multilevel inverter can deliver a quarter wave symmetric ventured voltage waveform integrated from a few DC voltages.

To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to h-1 harmonic contents can be removed from the voltage waveform. In general, the most significant low frequency harmonics are chosen for elimination by properly selecting the triggering or switching angles and high frequency harmonic components can be readily removed by using additional filter circuits.

The switching points of the inverter are figured by explaining the supernatural conditions mirroring every symphonious. An appropriate beginning estimation of regulation list and beginning theory is important to illuminate these conditions. Fathoming these supernatural conditions with n number of questions is a repetitive employment. In any case, the exchanging edges can be computed disconnected to wipe out the particular low request sounds and furthermore exchanging happens at the central recurrence and subsequently limits the

exchanging misfortunes. At the end of the day, just a couple of compensations occur in one cycle expanding proficiency and empowering air cooling. The calculation of the exchanging point increments with the expansion in the voltage levels. With a restriction for the changing points to be inside (pi/2), it gives a tight scope of adjustment file. This technique is constrained to open-circle applications what's more, low powerful execution requesting applications. The principle challenge related with SHE-PWM [5] strategy is to get the expository arrangement of the arrangement of nonlinear supernatural conditions that contain trigonometric terms which thus give different sets of arrangements.

This has been accounted for in various research papers. A few calculations have been accounted for in the specialized writing, concerning strategies for settling the resultant nonlinear supernatural conditions, which portray the SHE-PWM [5] issue. A consecutive homology based calculation and subterranean insect province calculation has been done to comprehend for the exchanging points. The hypothesis of symmetric polynomial, hypothesis of resultant polynomials and the resultant hypothesis have been proposed to comprehend the polynomial conditions acquired from the supernatural conditions. With an expansion in the quantity of H-spans associated in arrangement, the calculation increments as the request of the polynomials turn out to be high. In Newton Raphson strategy for settling these supernatural conditions, the exchanging edges can be processed with unimportant calculation exertion for any underlying theory. This technique is subordinate ward and may end in neighborhood optima. Further, a judicious choice of the initial values alone will guarantee convergence.

3.4 Sinusoidal Pulse Width Modulation:

Sinusoidal PWM method is also known as the triangulation, sub harmonic, sub oscillation method, Carrier Based Pulse Width Modulation (CB-PWM) is very popular in industrial applications. The SPWM scheme is illustrated in Figure 10.

In this, Vc is the peak value of the triangular carrier wave and Vr is the reference, or modulating signal. For realizing SPWM, a high frequency triangular carrier wave is compared with a sinusoidal reference of the desired frequency.

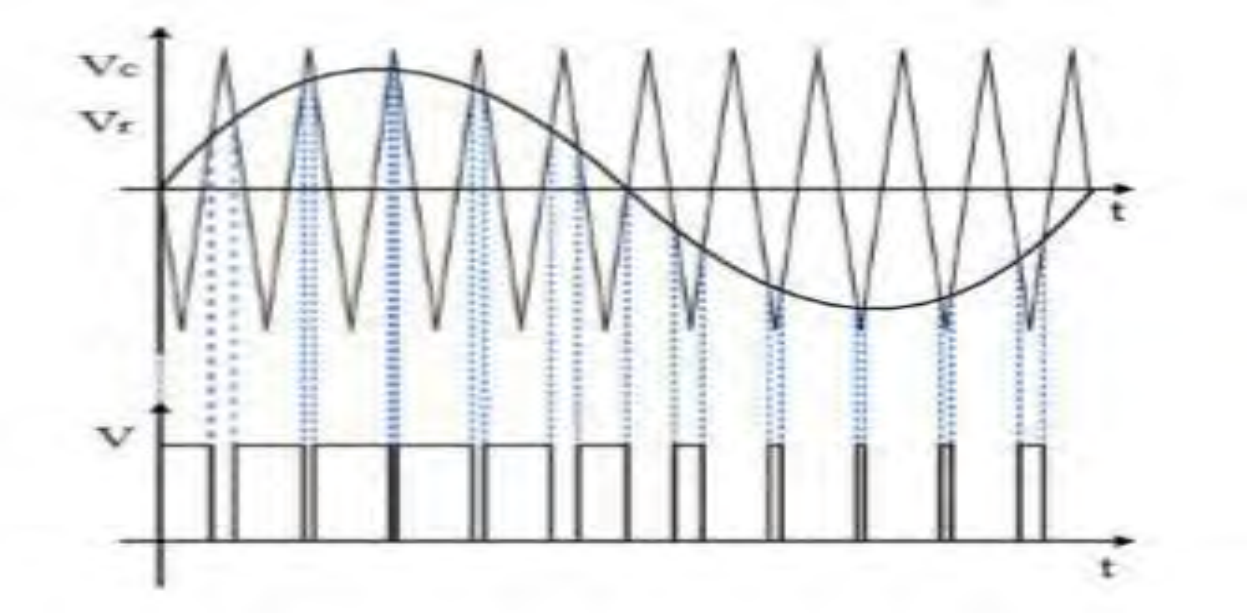

Figure 3.2: Sinusoidal pulse with modulation, source: [5]

The intersection of sinusoidal reference and triangular waves determines the switching instants and commutation of the modulated pulse. Operating with constant frequency of carrier signal concentrates on voltage harmonics around switching frequency (which is of double the carrier frequency) and multiples of switching frequency. Carrier based modulation for more than two level inverters require more carrier signals. For NL -level inverter, minimum (NL -1) carrier signals are needed.

Each carrier signal is responsible for a pair of switches. Every leg has two switches, one switch is controlled directly by the comparator signal and the other is controlled by its inverting signal. Multiple carrier signals in multilevel inverters create various possibilities of mutual locations of those signals. Typical combinations for multi-carrier systems are,

1. Phase Shifted Carriers (PSC)
2. Level Shifted Carriers (LSC)
3. Phase Disposition (PD)
4. Phase Opposite Disposition (POD)
5. Alternative Phase Opposite Disposition (APOD)

3.5 Phase Shifted Carriers:

This method of carrier signals placement is usually used in H-bridge and FLC converters. It can also be applied in all kinds of multilevel inverters. As in other types of sinusoidal modulation, PSC modulation requires (NL-1) carriers shifted in phase by 360°/ (NL -1), where NL is the number of levels. Each carrier is responsible for a pair of switches in all legs of the converter. In three phase system, two other phase voltages by comparison with the carriers are generating four more rectangular sequences for the remaining switches. Figure 3.3 presents carrier placement for three level inverter and one of the commanded voltages.

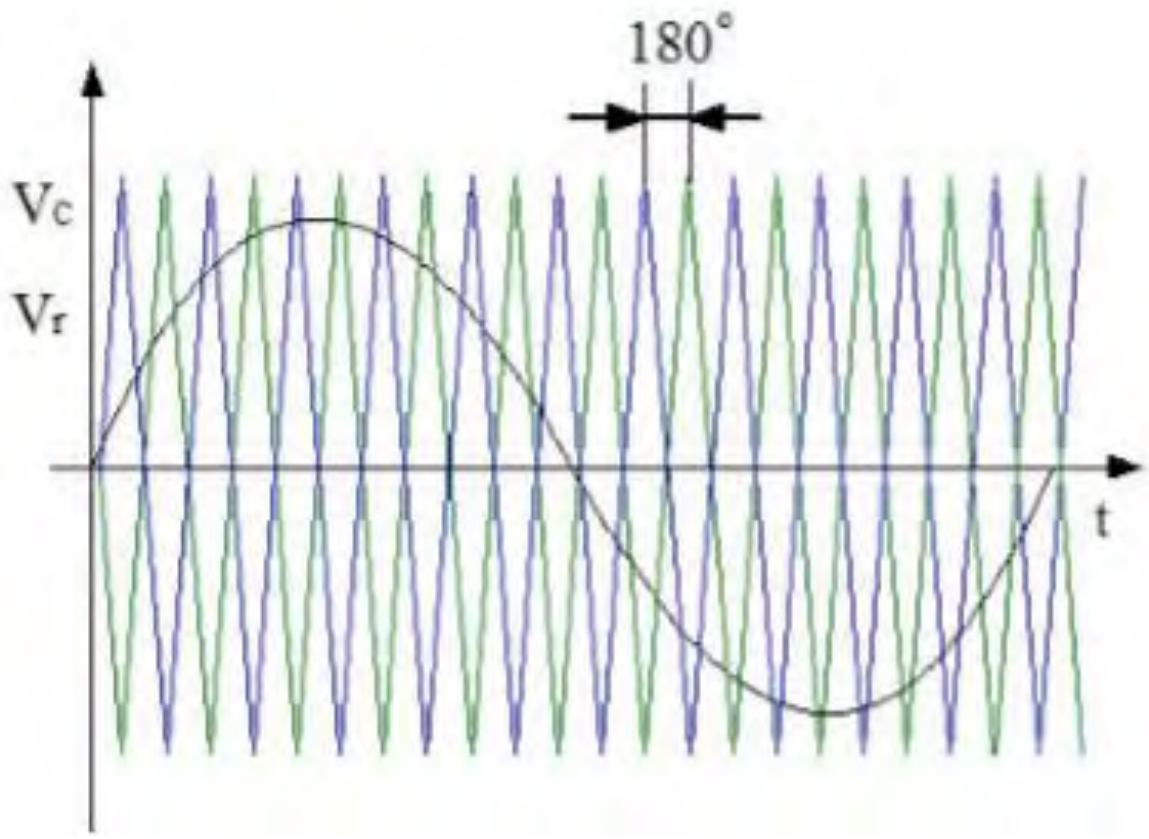

Figure 3.3: Phase shiftted carrier modulation, source: [5]

3.6 Level shifted carriers:

Second type of sinusoidal modulation is PWM with level shifted carriers. Difference between those methods is rather small and gathered around the output voltage spectrum. In PD-PWM

modulation technique, the major feature of the phase voltage spectrum is the significant first carrier harmonic. This carrier harmonic is a common-mode component across the phase voltages of a three phase inverter, and therefore gets cancelled in the output line voltage. This feature gives the PD-PWM to produce excellent line voltage performance. Consequently, with concentration of harmonics in the first carrier, the harmonic sidebands which of course do not fully get cancelled between the three phase legs have less energy. In POD-PWM control technique, the carrier signals which are above the zero level are in phase and the carrier signals which are below the zero level are in phase of each other and out of phase by 180 to the above signals.

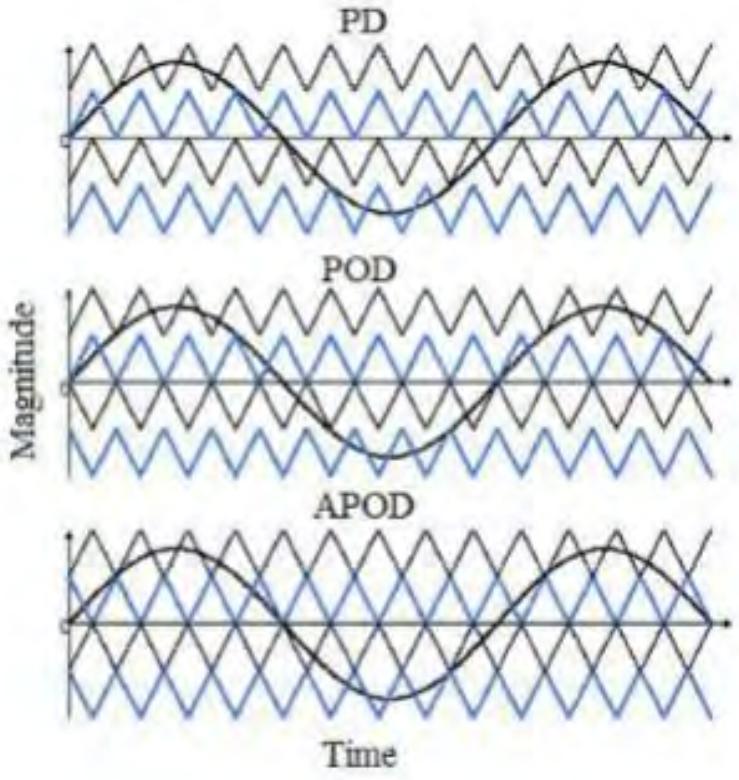

Figure 3.4: Level shifted PWM, source: [5]

For APOD, all carriers are in phase opposition by 180 from their respective adjacent carriers. Variants of this type of modulation take the names from mutual locations of the carrier signals as it is shown in Figure 3.4.

In this first chapter, operation of half bridge and full bridge inverters with their advantages and disadvantages are discussed. Detailed analysis of various multilevel inverters such as diode clamped, flying capacitor and cascaded H-bridge with their concepts are presented. Modulation techniques such as space vector PWM, selective harmonic elimination and sinusoidal PWM are presented. Investigation on their applicability for the different topologies is also discussed.

3.7 Conclusion:

The key aspect discussed here is the modulation techniques. To reduce harmonic distortion this technique can be applied. We discussed about PWM (Pulse Width Modulation) technique which includes space vector PWM, sinusoidal PWM. We also explained Level shifted PWM and phase shifted PWM.

CHAPTER 4

PROPOSED CASCADED MULTILEVEL INVERTER

4.1 Introduction:

An inverter or power inverter is a device which converts direct current (DC) to alternating current (AC). There are three types of inverters based on type of output waveform as: square wave, modified-sine wave and pure sine wave. A square wave is non sinusoidal waveform, most typically seen in electronics and signal processing. Square wave have two levels (positive and negative) and alternates regularly between these two levels. The output of a modified sine wave inverter is more like a square wave output except that it has one more level i. e, before switching positive or negative the output goes to zero volts. Though it is simple and low cost, most AC motors work on this power source or inverter reduces efficiency and the motors may also produce hissing sound while operating and due to which the life of equipment will reduce. A pure or true sine wave inverter changes or converts the DC supply into a near perfect sine wave. The sine wave has very little harmonic distortion which results in a very clean supply and makes it suitable for working electronic systems such as computers, motors and microwave ovens and other sensitive equipment without causing problems like noise. Things like mains battery chargers also run better on pure sine wave converters. Ideally the output waveforms of an inverter should be sinusoidal. However, the waveforms of practical inverters are non-sinusoidal and contains certain harmonics. Due to the availability of high speed power semiconductor devices, the harmonic contents present in the output voltage can be minimized significantly by using switching technique. BJTs, MOSFETs or IGBTs can be used as ideal switches.

4.2 Single Phase Bridge Inverter:

A single phase DC-AC inverter is shown in Figure below. The analysis of the single phase DC-AC inverters is done taking into account following assumptions and conventions.

1) The current entering between the first two MOSFETs node in Figure is considered to be positive.
2) The switches G1, G2, G3 and G4 are unidirectional, i.e. they conduct current in one direction.

When the switches G1 and G2 are turned on simultaneously for a duration $0 \leq t \leq T1$, the input voltage Vin appears across the load and the current flows from point a to b. Q1 – Q2 On, Q3 – Q4 Off ==>$v_o = V_s$

If the switches G3 and G4 turned on duration T1 ≤ t ≤ T2, the voltage across the load is reversed and the current through the load flows from point b to a.Q1 – Q2 OFF, Q3 – Q4 ON ==> ν o = - Vs

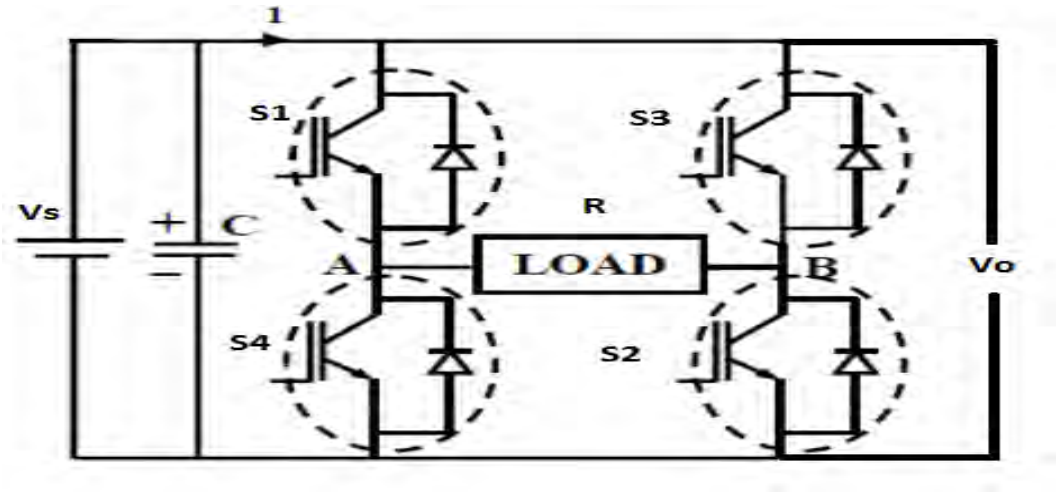

Figure 4.1: Single phase bridge inverter, source: [6]

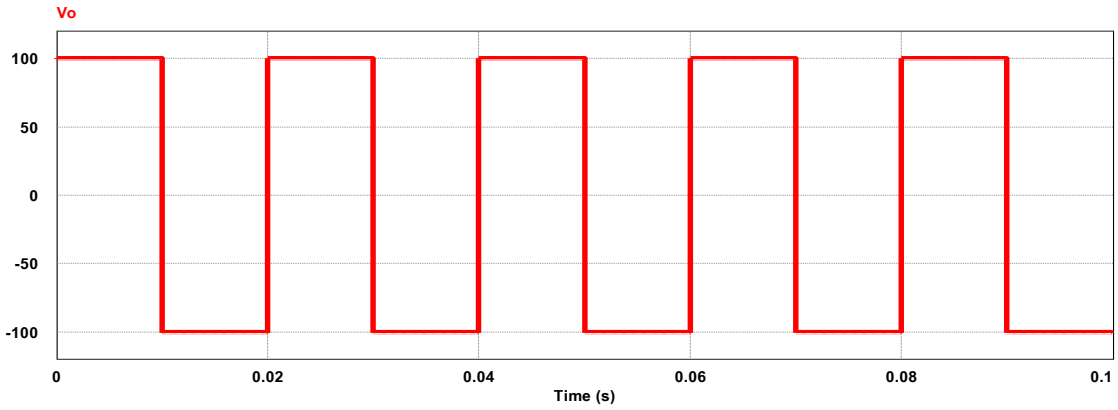

Figure 4.2: Output voltage (v0) of Figure 4.1

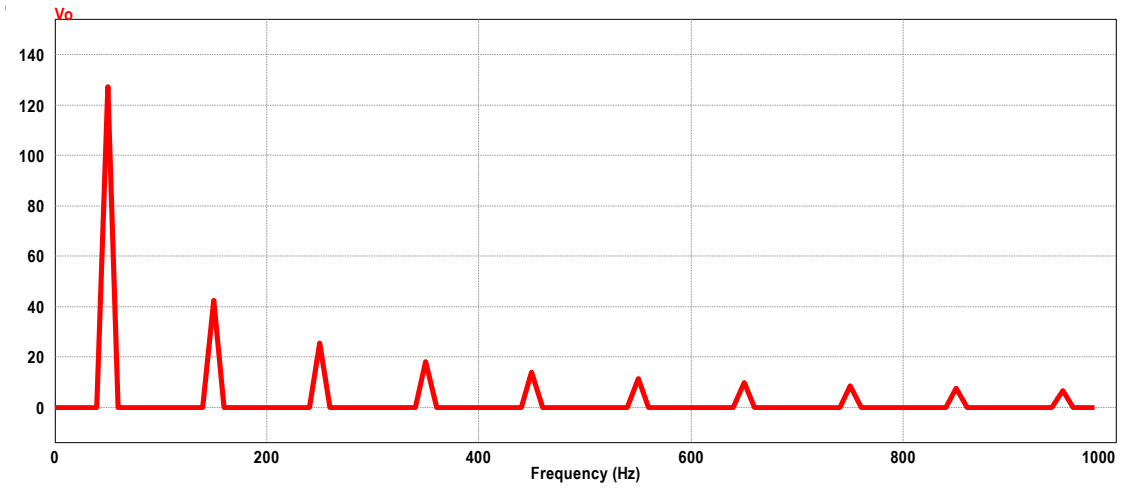

Figure 4.3: Fast Fourier Transform of Figure 4.1

Switching	Conduction mode	Conduction mode
	ON	OFF
S1	0-180	180-360
S2	0-180	180-360
S3	180-360	0-180
S4	180-360	0-180

Table 4.1: Switching sequences of figure 4.1 based of Conduction mode

Time step was 1E-005 for simulation control and total time was fix to 0.1 second. Here Fast Fourier Transform - FFT algorithm computes the discrete Fourier transform - DFT of the actual sequence. We wanted to convert out T vs Vo signal from its original domain to a representation in the frequency domain and vice versa. After Fast Fourier Transform we found a better analysis of the original voltage signal. It tells the relative amplitude of frequencies present in the signal. It can be defined for both discrete time and continuous time signal. Any signal can be represented as mixture of many harmonic frequencies.

4.3 Amplitude and Harmonic Control:

The amplitude of the fundamental frequency for a square wave output from of the inverter is determined by the dc input voltage. An integral multiple of the frequency of some reference signal or wave is called as harmonic [6]. The ratio of the frequency of such a signal to the frequency of the reference signal can also be referred as harmonic. Let the main or fundamental frequency of an alternating current signal is represent as f. This frequency f is expressed in hertz and most of the energy is contained at this frequency or the signal is defined to occur at this frequency. If harmonic signal is displayed on an oscilloscope the waveform will appear to repeat at a rate corresponding to f Hz. That is in the case of the square wave, the Fourier series contains the odd harmonics and can be represented as

$$v_o = \sum_{n_{odd}} \frac{4V_{de}}{n\pi} \sin n w_o t$$

A controlled output can be produced by modifying the switching scheme. An output voltage of the form shown below, has intervals when the output is zero as well as +Vdc and –Vdc. This output voltage can be controlled by adjusting the interval α on each side of the pulse where the output is zero. The rms value of the voltage waveform in figure 4 is, equation2

$$V_{rms} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi-\alpha} V_{dc}^2 \, d(\omega t)} = V_{dc}\sqrt{1 - \frac{2\alpha}{\pi}}$$

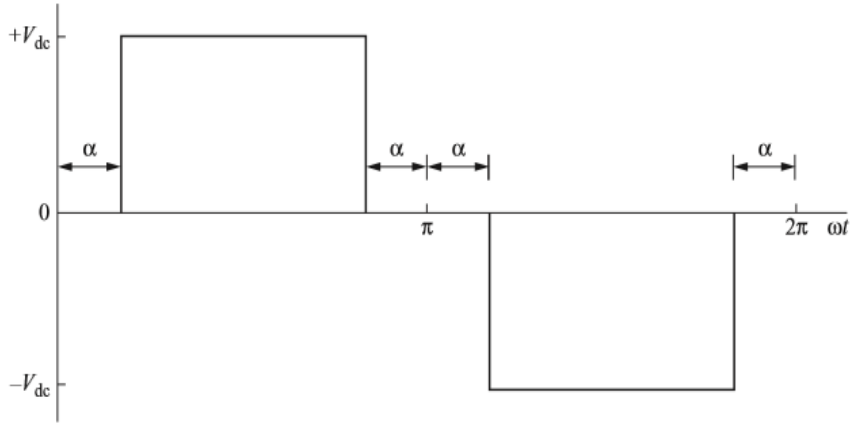

Figure 4.4: Inverter output for amplitude and harmonic control, source: [1]

The Fourier series of the waveform is expressed as,

$$v_0(t) = \sum_{n\,odd} V_n \sin(n\omega_0 t)$$

Taking advantage of half-wave symmetry, the amplitudes are

$$V_n = \frac{2}{\pi}\int_{\alpha}^{\pi-\alpha} V_{dc} \sin(n\omega_0 t)\, d(\omega_0 t) = \frac{4V_{dc}}{n\pi}\cos(n\alpha)$$

Where α is the angle of zero voltage on each end of the pulse. The amplitude of each frequency of the output is a function of α. In particular, the amplitude of the fundamental frequency (n =1) is controllable by adjusting α: equation5

$$V_1 = \left(\frac{4V_{dc}}{\pi}\right) cos\alpha$$

Harmonic content can also be controlled by adjusting α . If α=30°, for example, V3=0. This is significant because the third harmonic can be eliminated from the output voltage and current. Other harmonics can be eliminated by choosing a value of which makes the cosine term in equation4 to go to zero. Harmonic n is eliminated if,

$$\alpha = \frac{90^0}{n}$$

Amplitude control and harmonic reduction may not be compatible. Such as, establishing α at 30°to eliminate the third harmonic fixes the amplitude of the output fundamental frequency at V1=(4Vdc/pi) cos30° = 1.1Vdc and removes further controllability. To control both amplitude and harmonics using this switching scheme, it is necessary to be able to control the dc input voltage to the inverter.

Switching	Conduction mode	Conduction mode
	ON	OFF
S1	30-150	210-310
S2	240-330	60-120
S3	210-310	30-150
S4	60-120	240-330

Table 4.2: Switching sequences of figure 4.1 (at α=30°) based of Conduction mode

Figure 4.5 shows the output waveform for α = 30° and the sinusoid of $w=3w_o$. The product of these two waveforms has an area of zero, showing that the third harmonic is zero.

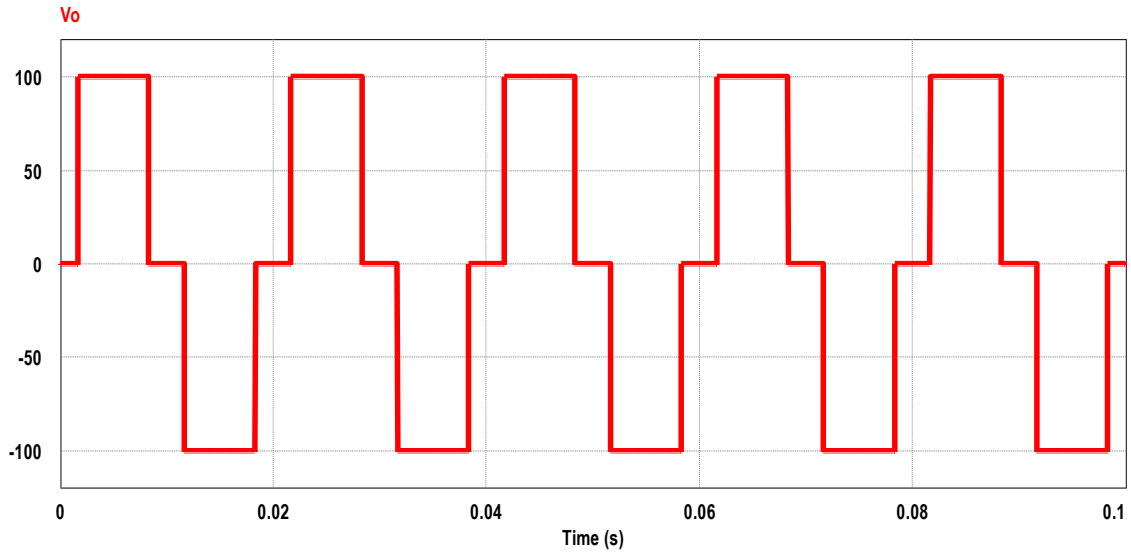

Figure 4.5: Output voltage (v0) waveform for α=30°

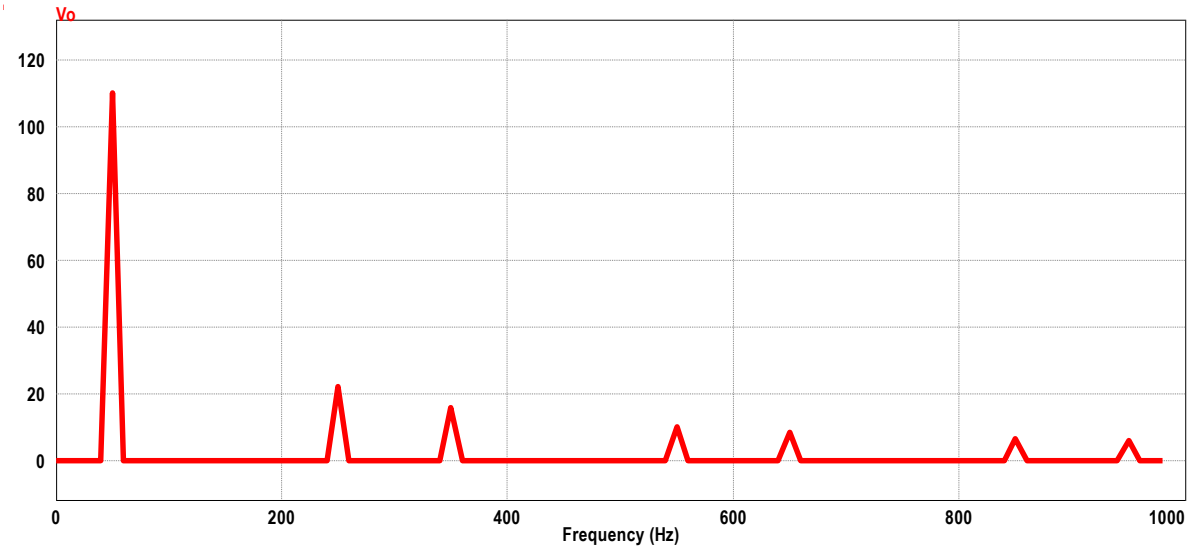

Figure 4.6: Fast Fourier Transform of Figure 4.4

Again for example α at 18°to eliminate the fifth harmonic fixes the amplitude of the output fundamental frequency at V1=(4Vdc/ pi) cos18° = 1.2Vdc and removes further controllability. And the sinusoid of $w=5w_o$, showing that the fifth harmonic is eliminated for this value of α.

4.4 Multilevel Inverter Design:

An electrical power inverter is basically a circuit that converts a DC signal into an AC signal. AC signal is more useful in our daily appliances and it travels easily. And it is easier to use multilevel inverters rather than using multiple power lines. Multilevel inverters give higher power .They are operated through multiple switches instead of one [7]. They can use environmental friendly energies like wind and solar energy and convert them to AC. To convert a DC signal into an AC signal we require fast switching of DC signal giving us multiple levels. This turns into a staircase wave that is quite close to a sine wave.

There are essentially three types of multilevel inverters: Cascaded H-Bridges: Using H-Bridge Cascaded multilevel inverters, we can invert up to three voltage levels. Different positions of switches, determine different voltage levels. The circuit consists of diodes and switches. This is the most common type of inverter and usually uses Separate DC sources (SDCs). However, due to recent advancements, single DC source H-Bridge Cascaded inverters can also be formed.

Diode Clamped: This type of inverter uses capacitors and diodes for inversion. The aim is to convert DC voltage into capacitor voltage. Proper precautionary measures should be taken in order to avoid over charging of capacitors. Flying Capacitor: This is a relatively complicated way of inversion, because the capacitors need to be pre charged, and is somewhat similar to diode clamped method. The difference is that clamping is done through capacitors instead of diodes. It is also known as imbricated cell multilevel inverter. A lot of research is still underway regarding multilevel converters, owing to their usefulness [7]. According to some researches the latter two of the above mentioned types are being combined. Numerous topologies have been presented to make most out of these.

The yield waveform can be of two sorts:

• Sine wave

• Modified sine wave while changing over from DC voltage to AC voltage, there are two strategies or modes:

• Either we change over the DC motion into Higher-Power DC flag and after that change over it into AC.

• OR we change over DC to AC at the lower level and afterward utilizing line recurrence we get the required yield voltage.

4.5 Two Level Inverter Design:

Psim simulation :

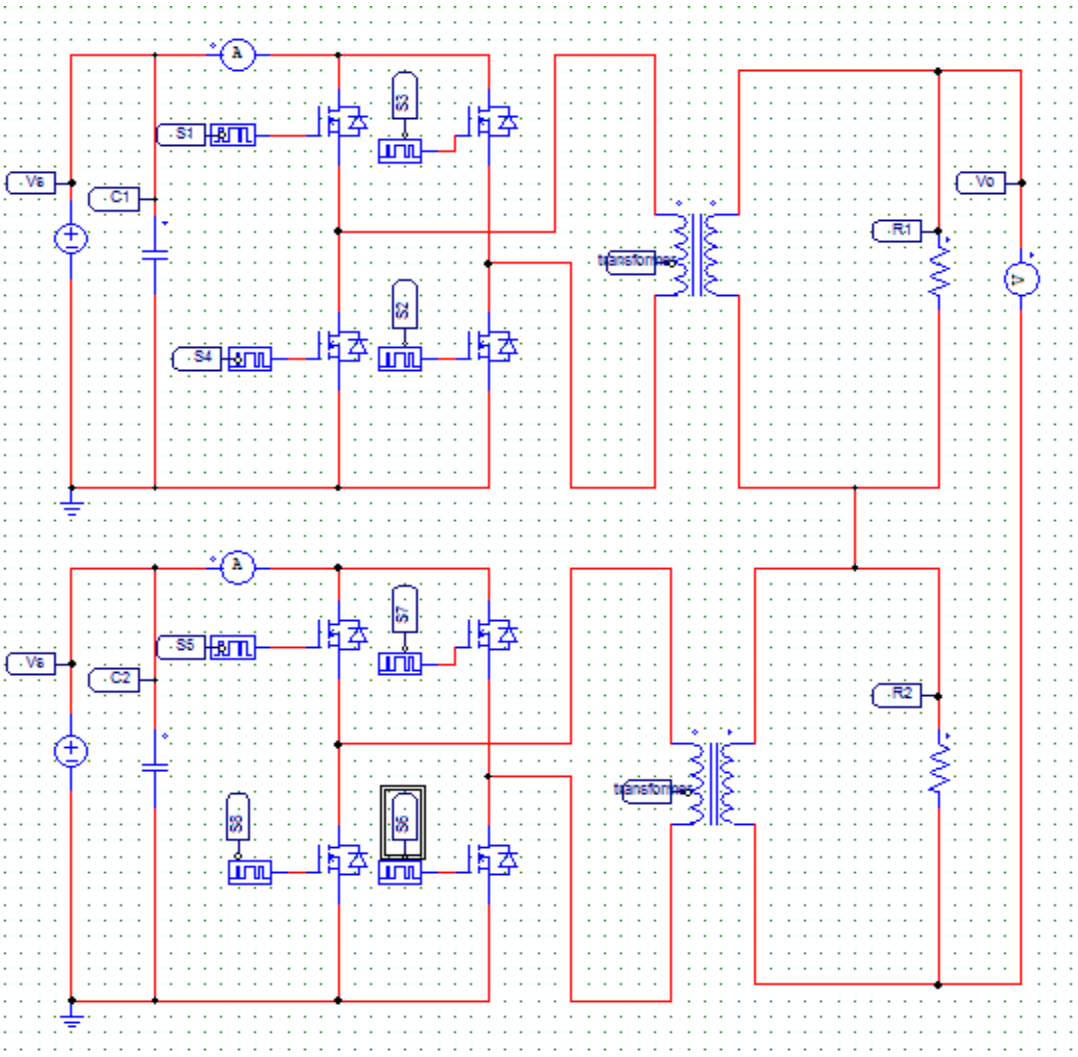

Figure 4.7: Two level inverterwith transformers

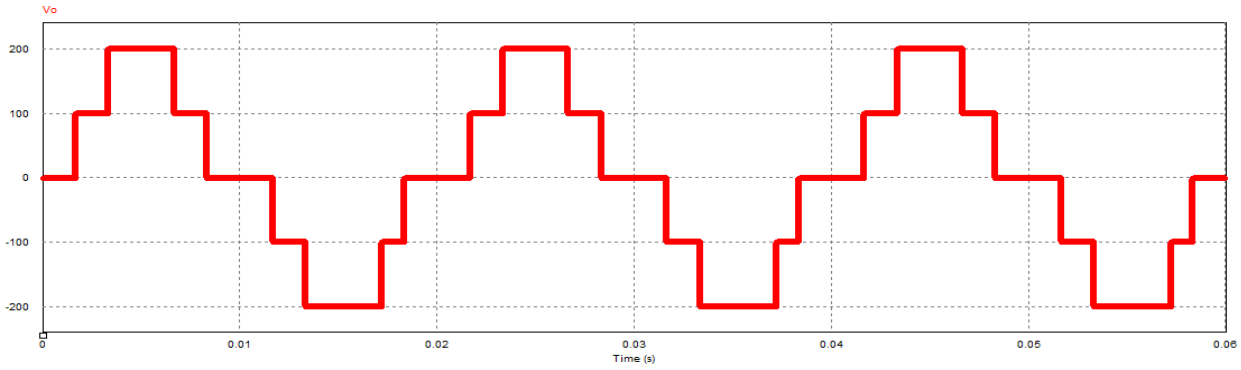

Figure 4.8: Output voltage (v0) waveform of Figure 4.7

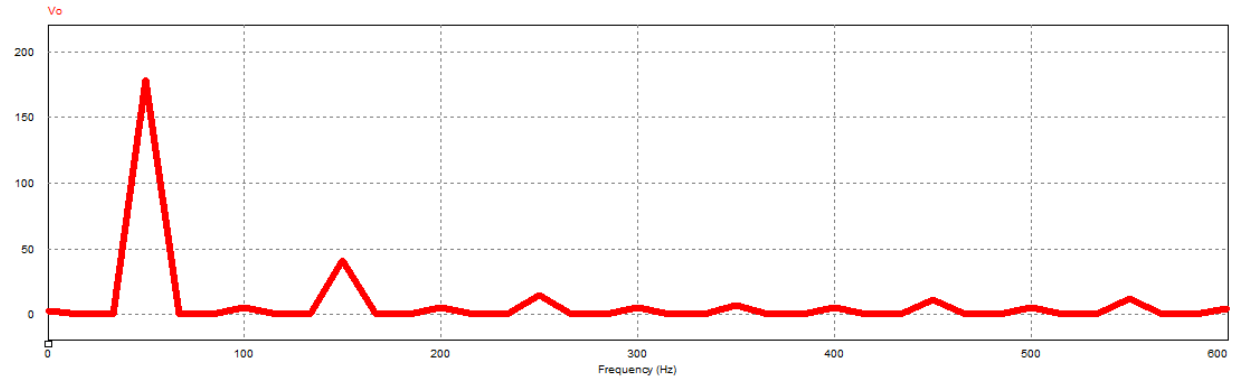

Figure 4.9: Fast Fourier Transform of Figure 4.8

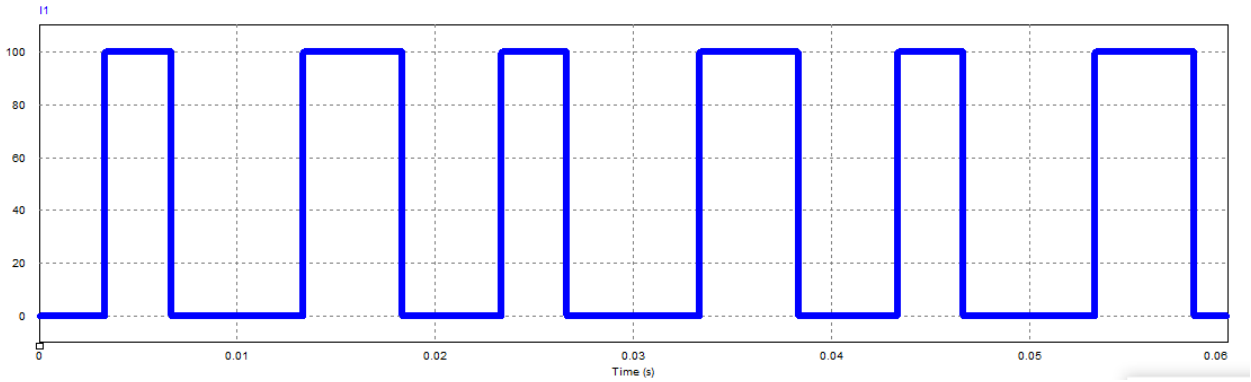

Figure 4.10: waveform of I1

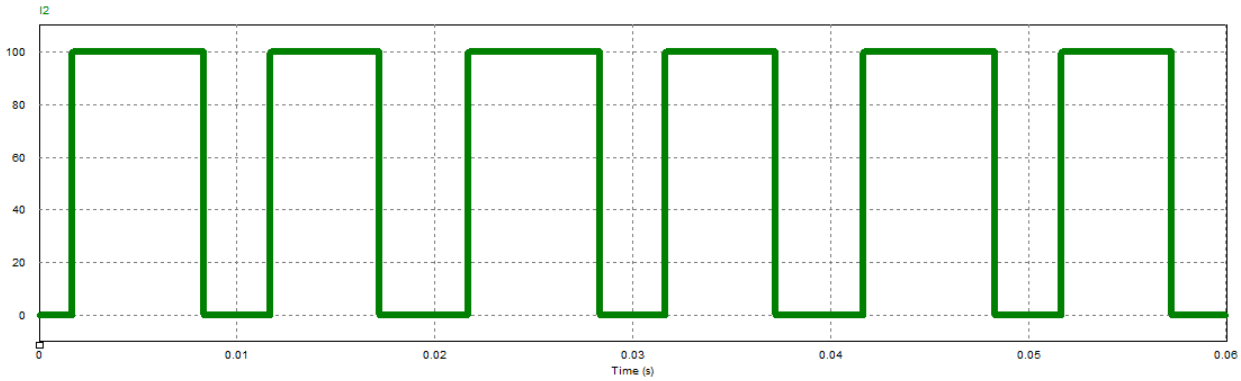

Figure 4.11: waveform of I1

Switching	Conduction mode	Conduction mode
	ON	OFF
S1	60-120	240-330
S2	60-120	240-330
S3	240-330	60-120
S4	240-330	60-120
S5	30-150	210-310
S6	30-150	210-310
S7	210-310	30-150
S8	210-310	30-150

Table 4.3: Switching sequences of figure 4.7 based on Conduction mode

Here we have used 8mosfets and connected switches sequence wise. The conduction mode was 120 degree. Two Ideal transformers are connected stage wise. Because it is a two level inverter so it operates accordingly the way switches are becoming On and Off. The capacitors are helping the circuit to work smoothly. The resistors are working finely to make the output flawlessly harmonic. Values of the resistors are 100 ohms.

4.6 Phase Disposition (PD):

The rules for phase disposition method for a two level inverter are

1) 2 carrier waveforms in phase are arranged.

2) The converter is switched to + Vdc / 2 when the sine wave is greater than both carrier waveform

3) The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier

4) The converter is switched to - Vdc / 2 when the sine wave is less than both carrier waveforms As can be seen from the figure in the PWM scheme there are two triangles,

The upper triangle ranges from 1 to 0 and the lower triangle ranges from 0 to –1. During the positive cycle of the modulation signal, when the modulation is greater than Triangle 1 and Triangle 2, then S1ap and S2ap are turned on and also during the positive cycle S2ap is completely turned on. When S1ap and S2ap are turned on the converter switches to the + Vdc / 2 and when S1an and S2ap are on, the converter switches to zero and hence during the positive cycle S2ap is completely turned on and S1ap and S1an will be turning on and off and hence the converter switches from + Vdc / 2 to 0. During the negative half cycle of the modulation signal the converter switches from 0 to -Vdc /2.

Here in the inverter we used ideal transformers to change a certain DC input voltage into a completely different AC output voltage either higher or lower.

A lot can be said about the potential applications of Multilevel Inverters. They are usually used in industrial applications. Multilevel inverters are inarguably important in the areas where we need high power. Some areas of usage are:

- Power conditioning
- Active Filters
- Industrial Motor Drives
- Power Grids
- Transportation.

4.7 Three Level Inverter Design:

The three level inverters produce common mode voltage, reducing the stress of the motor and don't damage the motor. It can draw input current with low distortion. The inverter can operate at both fundamental switching frequencies that are higher switching frequency and lower switching frequency. It should be noted that the lower switching frequency means lower switching loss and higher efficiency is achieved. Selective harmonic elimination technique along with the multi-level topology results the total harmonic distortion becomes low in the output waveform without using any filter circuit. The three level inverter offers several advantages over the more common two level inverter. Most often the NPC inverter is used for higher voltage inverters. Because the IGBTs are only subjected to half of the bus voltage, lower voltage IGBT modules can be used.

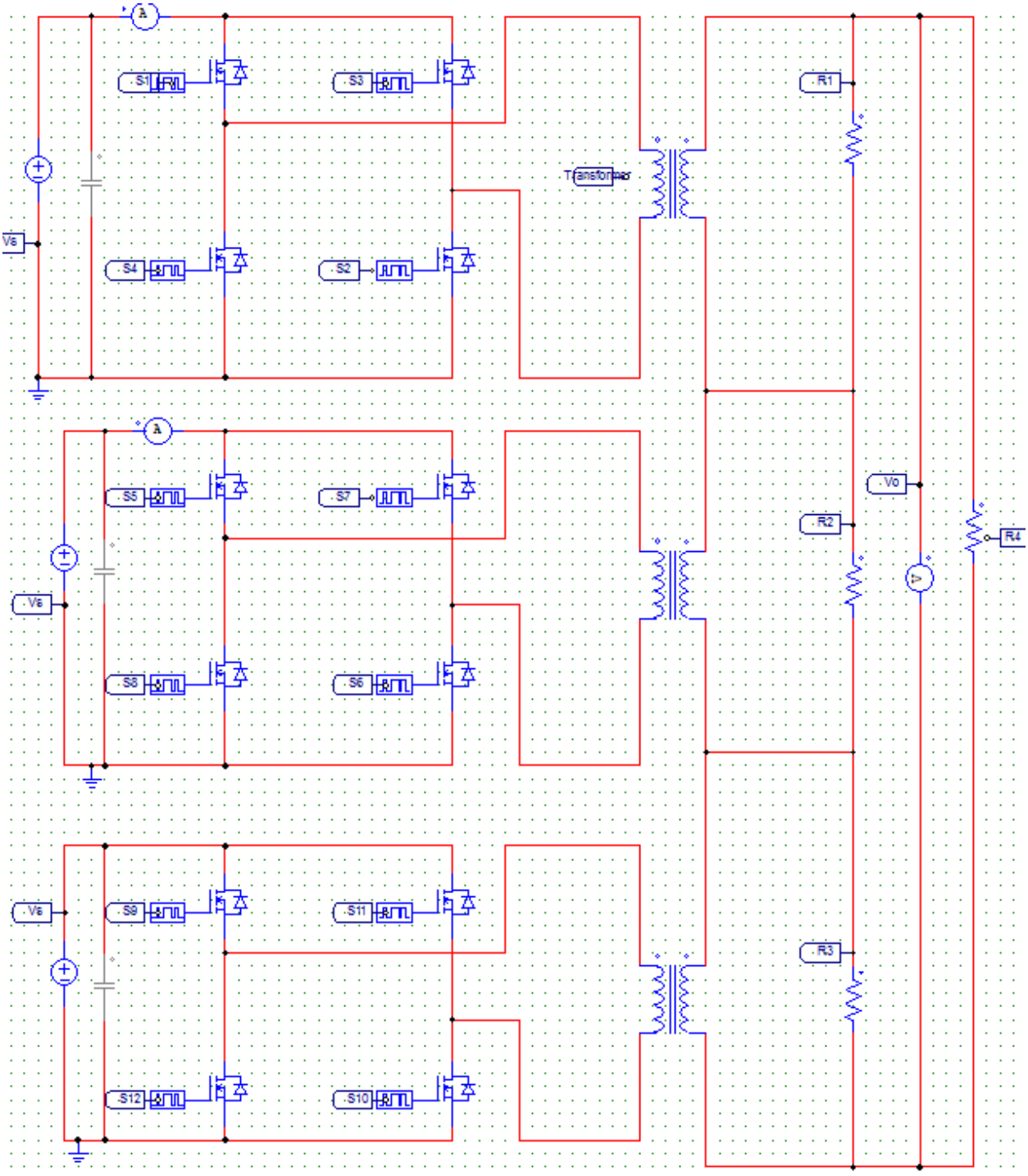

Figure 4.12: Three level inverter with transformers

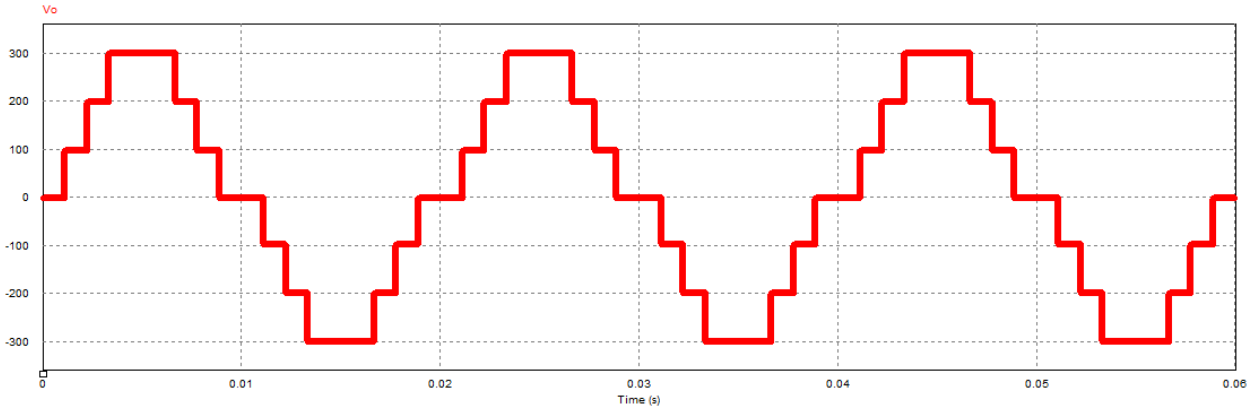

Figure 4.13: Output voltage (v0) waveform

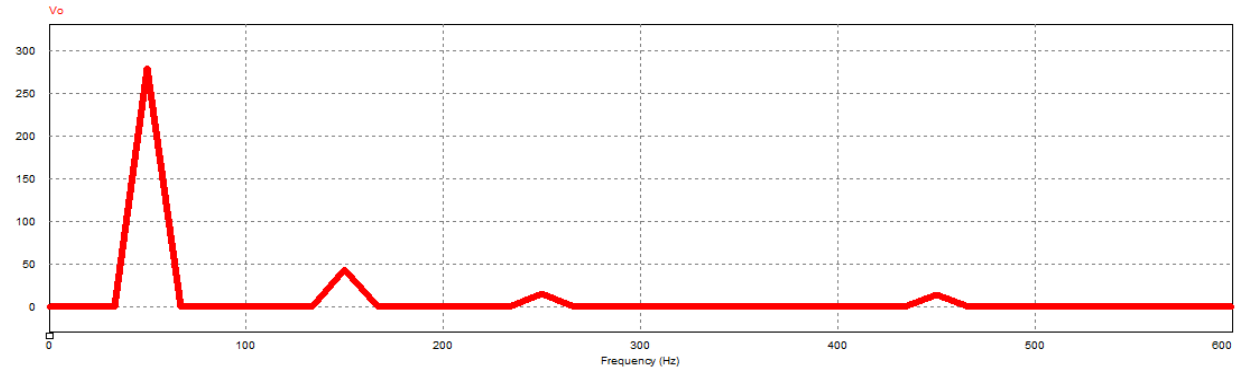

Figure 4.14: Fast Fourier Transform of Figure 4.13

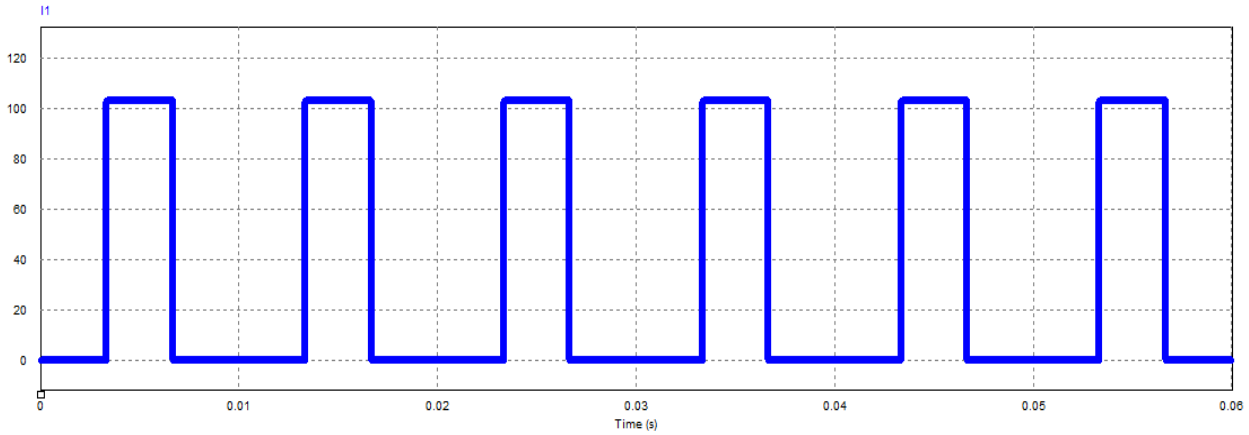

Figure 4.15: waveform of I1

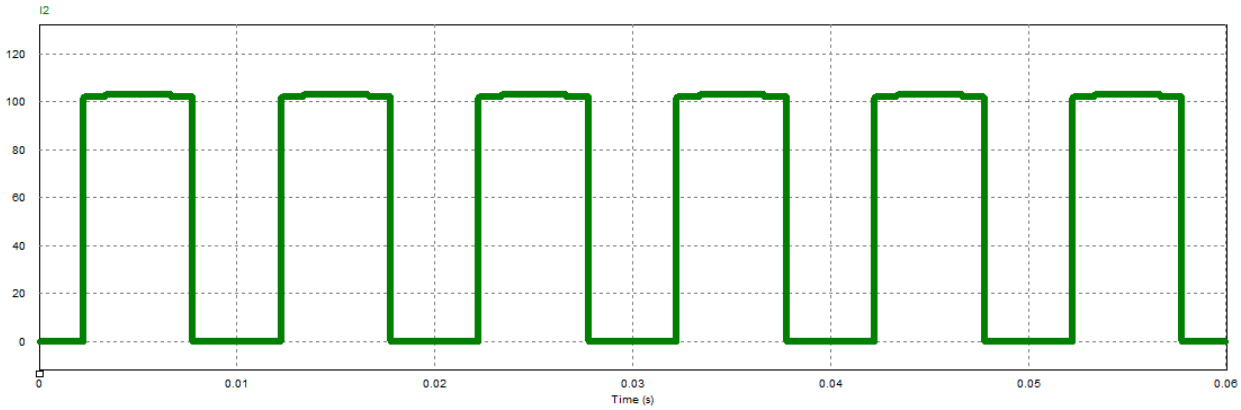

Figure 4.16: waveform of I1

Switching	Conduction mode	Conduction mode
	ON	OFF
S1	60-120	240-300
S2	60-120	240-300
S3	240-300	60-120
S4	240-300	60-120
S5	40-140	220-320
S6	40-140	220-320
S7	220-320	40-140
S8	220-320	40-140
S9	20-160	200-340
S10	20-160	200-340
S11	200-340	20-160
S12	200-340	20-160

Table 4.4: Switching sequences of figure 4.12 based on Conduction mode

Here we have used 12 MOSFET's and connected switches sequence wise. The conduction mode was 120 degree. Ideal transformers are connected stage wise. Because it is a three level inverter so it operates accordingly the way switches are becoming On and off. The capacitors are helping the circuit to work smoothly. The resistors are working finely to make the output flawlessly harmonic. Values of the resistors are 1ohms and 100 ohms.

Advantages:

1. Better waveform quality of output voltage (more sinusoidal).
2. Reduced dv/dt, leading to reduction in EMI.
3. Lower voltage rating devices can be used.

Disadvantages:

1. Higher component count
2. Some configurations need more than one isolated DC supply.

4.8 Conclusion:

Here in this part we discussed about our proposed cascaded circuit and their output wave shapes. Circuits output wave shapes FFT analysis have been discussed here and also about their harmonics.

CHAPTER 5:

CONCLUSION

&

FUTURE RESEARCH

5.1 Conclusion:

The elementary concept of a multilevel inverter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Loads, Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel inverter can be briefly summarized as follows.

● Staircase waveform quality: Multilevel inverters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) [1] problems can be reduced.

● Common-mode (CM) [3] voltage: Multilevel inverters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies such as that proposed in.

● Input current: Multilevel inverters can draw input current with low distortion.

● Switching frequency: Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM [3]. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. Unfortunately, multilevel inverters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated ~ 36 ~ switches can be utilized in a multilevel inverter, each switch requires a related gate drive circuit [3]. This may cause the overall system to be more expensive and complex. Plentiful multilevel inverter topologies have been proposed during the last two decades. Contemporary research has engaged novel converter topologies and unique modulation schemes. Moreover, three different major multilevel inverter structures have been reported in the literature: cascaded H-bridges inverters

with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped). Moreover, abundant modulation techniques and control paradigms have been developed for multilevel inverters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. In addition, many multilevel inverters applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, flexible AC transmission system (FACTS), and traction drive systems. In the thesis paper we have considered Square wave as outputs because this is one of the most straightforward waveforms an inverter configuration can deliver and is most appropriate to low-affectability applications, for example, lighting and warming. Square wave yield can create "murmuring" when associated with sound hardware and is by and large unacceptable for delicate gadgets.

5.2 Further Research Scope:

World energy requirement is almost completely dominated by fossil fuel even though fossil fuel are non-sustainable energy sources. Hence the world energy sector is continually in the look for greener and sustainable energy sources**.** For further research we want to work with different renewable sources. Particularly, in a solar power harvesting system, the photovoltaic inverter is considered as the most crucial component [8]. Inverter specifications and functions depend on the architecture chosen for the system. In further research we want to study and experience the cascaded inverters and its use in photovoltaics and their different architecture systems.

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