BRAC UNIVERSITY

SCHOOL OF ENGINEERING AND COMPUTER SCIENCE

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

GRAPHENE BASED NANO SCALE HEAT SPREADER IN FIELD EFFECT TRANSISTOR

BY

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IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE DEGREE OF BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

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In the name of Allah, the most gracious, most merciful.

Department of Electrical and Electronics Engineering,

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Declaration

We, hereby declare that this thesis is a work of research and self-study. All the information in this academic paper has been inferred from published work of others. Data, equations, images and all sources are properly cited. This work has not been partially or fully presented anywhere else.

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Preface:

After the invention of the MOSFET (Metal-Oxide Silicon Field Effect Transistor), in the late 50's the electronics industry changed dramatically. Use of conventional Vacuum Tubes were rapidly being replaced by cheaper, smaller and more efficient MOSFETs. The fundamental function of a MOSFET was to be used as a switch and/or an amplifier. However as time went by, and people needed faster processing powers for their computing needs, the MOSFET needed to be improved. Integrated circuits have continuously been miniaturized and the current trend toward nanoscale electronics have led to tremendous integration levels, with hundreds of millions of transistors implemented on a chip area no larger than a few square centimeters in accordance with Moore's Law [P1]. IC's are becoming smaller as well as more powerful. Technological advancement has to be in par with human needs. However the major roadblock in terms of IC technology advancement is the immense by-production of heat. Moore's Law has an end point and after a certain dimension transistors cannot be made any smaller. Higher chip temperatures will prevent the optimum performance of integrated circuits. As IC's are becoming much smaller heat generation is increasing, and chip temperatures are reaching levels that will prevent the reliable operation of integrated circuits. So rather than focusing on minimizing the size of transistors, we have proposed to minimize the heating effect. Power densities of Chip-level can reach up to 100 W/cm^2. If the rates of VLSI (Very Large Scale Integration) follow the guidelines presented by the International Technology Roadmap for Semiconductors (ITRS) the chip-level power density is likely to increase even further. Increasing power density levels will render many electronic systems unusable without significant advances in cooling technology, or without fundamental changes in design. The situation is compounded by millimeter-scale hot spots on the chip, i.e., localized regions of higher heat generation rate per unit area and hence higher temperatures

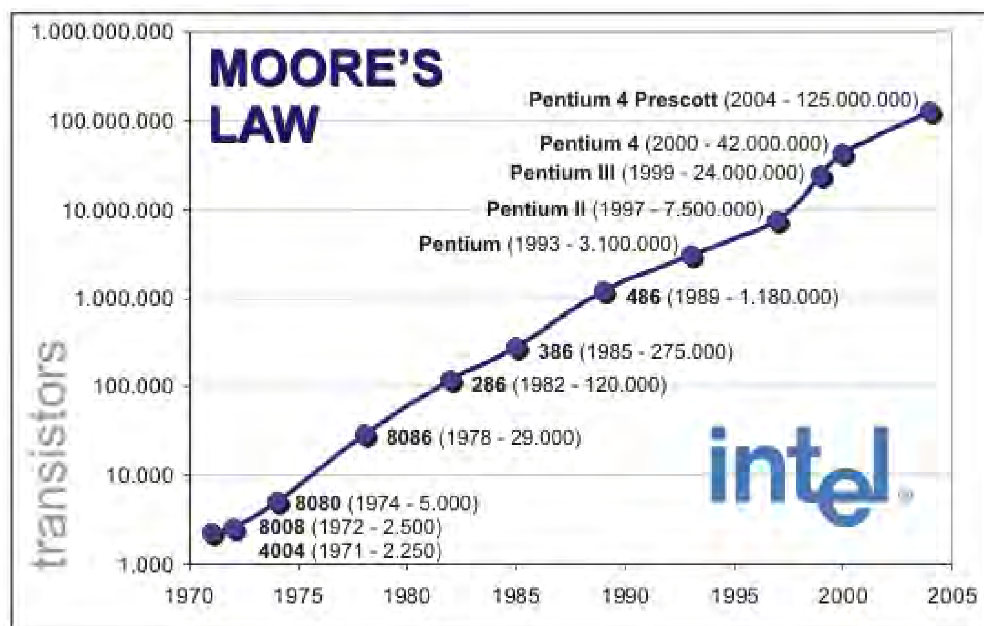

Fig: P1 Moore's Law

Thesis Abstract:

Currently the methods used to reduce the generation of heat in semiconductors are mainly Flip-chip bonding and the use of metal matrix composite. Both are not very efficient when it comes to dispersing the inert heat generated in a transistor. There is still little if not zero progress behind thermal management of a transistor in its core that is in the nanometer scale. Generally speaking, the electrical energy that is supplied to electronic devices is ultimately transformed into and dissipated as heat. This generation of heat is accompanied by a temperature rise at the heat source followed by the transport of heat to regions of lower temperature within and outside the electronics module or package. Within the package transport of heat occurs via a process of thermal conduction in the solid material making up the package. As the heat reaches the external surfaces of the package it is usually transferred to a cooling fluid (e.g., air) via a thermal convection process. In the case of lower power components thermal radiation may also play a role in transferring heat to the surrounding environment. The temperatures within the electronics package will continue to rise until the rate of heat removal from the package is equal to the rate of heat generation. It is worthwhile to note that, even if purposeful active measures were not taken to cool the package, the laws of nature or physics would prevail and limit the temperature rise. However, in most instances, the resulting temperatures would be too high. As shown in Fig: [T] based upon the results of a study conducted under a US Air Force Avionics Integrity Program, temperature was identified as the principal factor in 55% of electronic failures. In addition to the effect of temperature on electronic device reliability, it can also play an important role on CMOS circuit performance. Consequently, it is necessary to provide satisfactory cooling for electronic packages by design. Heat is generally produced inside a semiconductor, when high amounts of current is flowing. Although methods to dissipate the heat from the exterior of the packaging is available, little to no work has been done to minimize heating effect in the nanometer scale. Heat is produced by mostly Peltier conditions and other effects, which will be

discussed later. Our idea is to put in a Graphene based Nano sheet inside the transistor to be used a heat spreader, which will absorb the excess heat produced and dissipate it out. Thereby improving transistor functionality. Graphene is a highly thermal conductive material, consisting of a single layer, one atom thick hexagonal lattice of Carbon atoms. Graphene's (*pure, undoped*) thermal conductivity is as high as, 2000-4000 W m^{-1} K^{-1}. Silicon based semiconductors have thermal conductivity of 150 W m^{-1} K^{-1}. Diamond, a very popular material with excellent thermal properties has a thermal conductivity of 1000 m^{-1} K^{-1}. Graphene can be said to be a cousin of Diamond. Both have Carbon as their base element, both have similar properties. However Graphene beats the race of thermal management. We have also used different versions of Graphene such as Bi-Layer, Few Layer, N-Doped and Al-Doped. These test materials have been simulated in QuantimeWise^{TM}, and we have showed different Figure of Merit (ZT) for different types of graphene. Other parameters such as, Seebeck Coefficient, Phonon Thermal Conductivity and Electron Thermal Conductivity have also been evaluated.

All our calculated results are analyzed and presented in an organized manner.

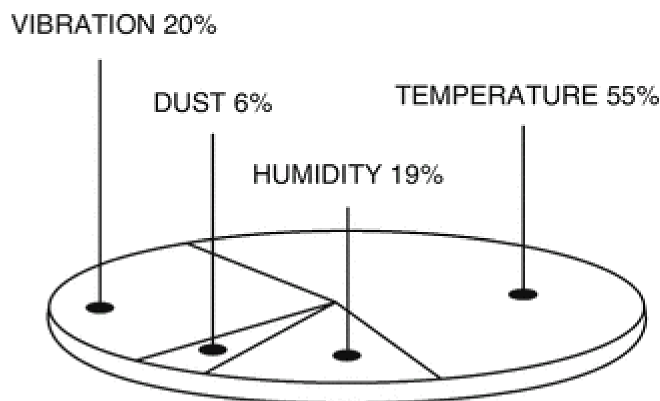

Fig: [T] Pie chart of the factors of Device Failure

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Abbreviations

MOSFET = Metal Oxide Silicon Field Effect Transistor

VLSI = Very Large Scale Integration

IC = Integrated Circuits

MMC = Metal Matrix Composite

DOS = Density of States

SLG = Single Layer Graphene

FLG = Few Layer Graphene

CVD = Chemical Vapor Deposition

Nomenclature

Constant:

K_B= Boltzmann constant, $1.38 \times 10^{-23} m^2 kg s^{-2}$

$\hbar$ = Reduced Planck constant, $1.055 \times 10^{-43} Js$

Symbols:

A= Cross-sectional Area, m^2

C= Spectral Volumetric Specific Heat, $m^{-3}Hz^{-1}K^{-1}$

D=Density of States per unit volume per unit frequency interval, $m^{-3}Hz^{-1}$ e= Charger Per Carrier

E_f = Fermi Level

E_g = Band Gap Energy

E_c = Conduction Band Energy

I= Electrical Current, A

J_e = Electrical Current Density, Am^{-2}

J_q= Heat Flux, Wm^{-2}

G_K= Thermal Conductance, $Wm^{-2}K^{-1}$

R= Electrical Resistance, Ω

S= Seebeck Co-efficient, VK^{-1}

T=Temperature, K

V= Velocity, ms^{-1}

Z= Figure of Merit, K^{-1}

B= Thomson Co-efficient, VK^{-1}

Π= Peltier Co-efficient

K= Thermal Conductivity, $Wm^{-1}K^{-1}$

ρ = Electrical Resistivity, Ωm

ω = Angular Frequency, rad. Hz

1.0

Introduction:

Our electronics industry has seen a rapid boom in growth since the invention and development of transistors on the 23rd of December, 1947 at Bell Laboratories. Since then in accordance with the Moore's Law, transistors have been greatly reduced in size, and have seen an increase in speed and performance. However as more chips are being assembled on a surface of area no more than a few square centimeters, transistors have to face an obstacle which is excessive heat generation. Due to which transistor performance cannot be optimum. Heating in a semiconductor is caused mainly due to Peltier Effects, Thomson Effects and Joule Heating. Conventional methods to minimize this heat has not been proven to be highly effective. We propose to implement a graphene Nano sheet inside the transistor, on top of the substrate. The heat produced in the transistor should be conducted away from the core, through the highly conductive graphene. Thermal conductivity of graphene is measured by the summation of Electron Thermal Conductivity and Phonon Thermal Conductivity.

$$Kph + Ke = Kt$$

Figure of Merit (ZT) is a useful tool to analyze the level of conductivity in a material. ZT is a function of Thermal Conductivity Kt.

$$ZT = S^2\sigma T/Kt$$

2.0

Conventional Thermal Management:

Heating in transistors are inherently a bad omen. But how heating in a transistor causes negative effects in its performances? We will be discussing it soon. Meanwhile let's look at ways in which excessive heating in transistors or ICs is curbed. Conventionally there are two popular methods to minimize heat production in a transistor device package. They are Flip-chip bonding and Composite Metal Matrix. Both of these will be discussed briefly.

i) Flip-chip bonding:

Flip-chip bonding also known as controlled collapse chip connection (C4) is a method for connecting semiconductor devices such as IC to external circuits, using solder bumps. Flip-chip mounting technology will be talked about in brief. To attach the flip chip into a circuit, the chip is inverted to bring the solder dots down so it can be connected to the underlying electronics. To create an electrical connection the solders are then re-melted. Most of the time an insulating adhesive is then "under filled" to provide a stronger mechanical connection and to provide a heat bridge.

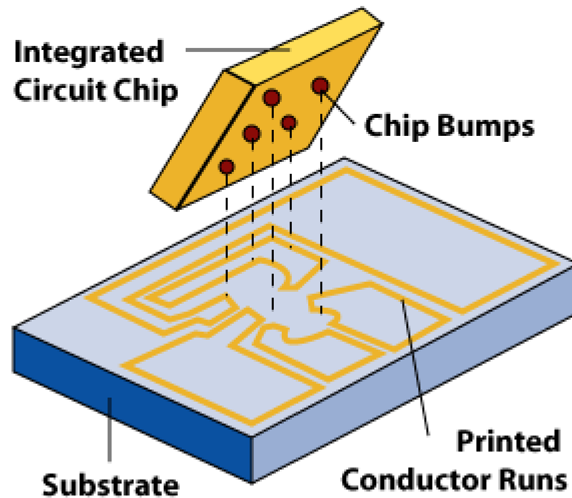


Fig: 2 (a) Flip Chip Bonding

Flip chips have several disadvantages. Flip chips require very flat and stable surfaces on which to mount it, which is difficult to maintain as the boards continuously heat and cool. The short connections are very rigid, so the thermal expansion of the chip must be matched to the on laying board or the connections can crack. Lack of carrier means it is not easy to replace, or install it manually. The material for the under fill or the bulk is moreover electrically insulating, which will provide high impedance adding nuisance to the thermal performance noticeably.

ii) Metal Matrix Composite (MMC):

A metal matrix composite is a composite material constituting of two materials, one being a metal and the other being a metal or an organic compound. MMC's are made by dispersing a reinforcing material into a metal matrix. For example, carbon fibers are seen to be used with Aluminum matrix to synthesize composites. The reinforcement material is embedded in the matrix, which means there is a path between the matrixes to any point in the material, unlike two materials sandwiched together. Two different thermal properties of the matrix and the

reinforcement material changes the overall thermal conductivity of the material. Hence MMC's are popular method for thermal management. Copper-silver alloy matrix containing 55% by volume diamond particles, known as Dymalloy, is used as a substrate for high-power, high-density multi-chip modules in electronics for its very high thermal conductivity.

Aluminum-Graphite composites are used in power electronic modules because of their high thermal conductivity, the adjustable coefficient of thermal expansion and the low density.

Regardless of its excellent thermal conductivity, it is not widely used in the field of Thermal Management. Thermal Conductivity of MMC's are high but cannot be varied. The higher price of MMC's prohibit the widespread use in semiconductors or IC's.

All of the above methods were applicable to IC level, however scientists are now faced with an even bigger challenge. Heating in a nanometer length scale, inside the packaging, within individual transistors.The next section talks about the causes of heating in a transistor.

3.0

Heat Generation in Si-Transistors

Higher packing densities mean higher power densities [Fig: 3.0] usually in the space of 100W/cm^2. Confined geometries such as those in FinFET$_s$ and in other Strained Silicon devices, poor thermal properties such of elements like Silicon (with which most transistors are built) and finally thermal resistance near the material boundaries cause excessive power dissipation. Heat is generated spatially (channel vs contacts) and spectrally (acoustic vs optical phonons).

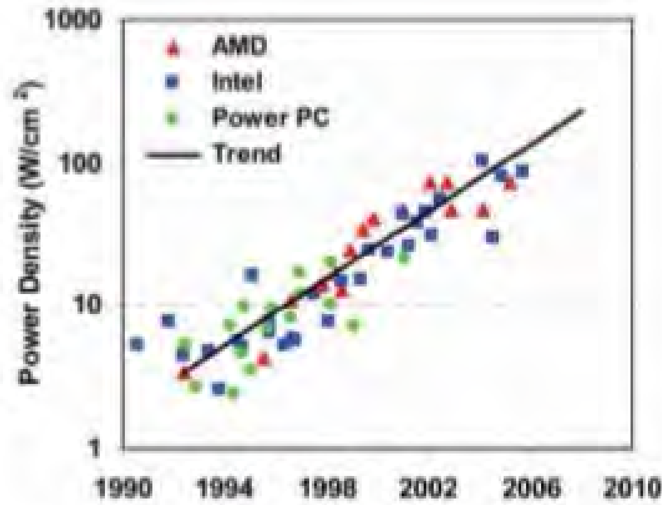


Fig: 3 (a) Power Density increases every year

Decreasing dimensions lead to nano-meter scale hotspot regions, which might increase the drain-source electrical resistance in devices such as SOI-FET, FinFET, CNT-FET, TMD-FET, and NW-FET.

The heating is mainly due the effect known as Joule Heating.

i) Joule Heating:

Joule Heating, to be put in simple words is the dot product of the electric field and current density.

$$H = \boldsymbol{J}.E$$

H = Heat dissipated/ Power Density (W/cm^3)

J = Current Density (A/cm^2)

E = Electric Field (V/cm)

The more complete fine-element model is:

$$H \approx \boldsymbol{J}.E + (R\text{-}G)\ (E_g + 3K_bT).$$

The second term is the heating rate due to the non-radiative generation (G) and recombination (R) of electron-hole pair.

In the perspective of a field-effect transistor (FET), the applied voltage leads to an electric field which is the highest near the drain of the device. This field speeds up the charge carriers (e.g., conduction band electrons in an n-type FET) which gain energy and heat up. Electrons can scatter with each other, with lattice vibrations known as phonons with material interfaces, imperfections or impurity atoms. Of these, the electron density only loses net energy by scattering with phonons, as a result heating up the lattice through the mechanism known as Joule heating. The lattice absorbs the extra electron energy, warms to a higher temperature and in return affects the electronic transport properties of the material. Electrons with energies greater than 50 meV scatter mainly with optical phonons in silicon, while those with lower energy scatter strongly with the acoustic modes. The optical phonon modes have lower group velocities (on the order of 1000 m/s) and their occupation is comparatively low as well, hence they contribute very little to heat transport. The main heat carriers in silicon are the faster acoustic phonon modes, which are significantly denser and have group velocities ranging from 5000 m/s to 9000 m/s. Optical phonons decay into acoustic modes, but over relatively long time scales, such as in the order of picoseconds, while the electron-optical phonon scattering time is on the

order of tenths of picoseconds. Under high field conditions, this can make way for the creation of a phonon energy bottleneck which can cause the density of optical phonon modes to build up over time, leading to more scattering events and obstructing electron movement. These processes are symbolically illustrated in the figure below:

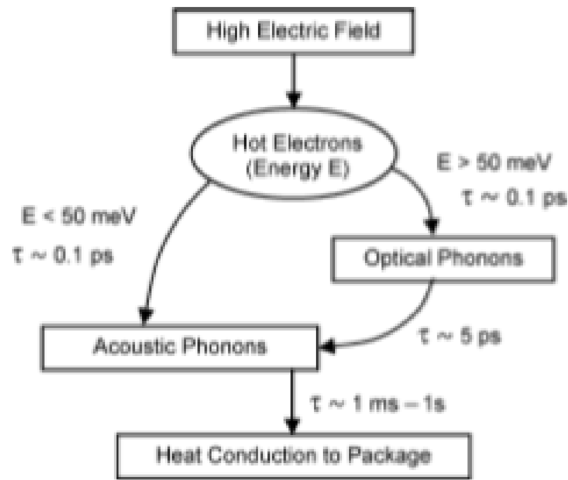


Fig: 3 (b) Joule Heating in Si based transistors

ii) Drawbacks due to excessive heating:

1. Thermal Runaway:

Silicon shows a strange behavior, in that it's electrical resistance increases with temperature up to about 150-160 °C, then starts falling, and drops further when the melting point is reached. This can lead to thermal runaway phenomena within internal regions of the semiconductor junction; the resistance decreases in the regions which are heated above this threshold, allowing

more current to flow through these regions, in turn causing yet more heating in comparison with the surrounding regions, which leads to further temperature increase and resistance decrease, and turns into a cycle.This leads to the phenomenon of current crowding (similar to current hogging, but within a single device), and is one of the underlying causes of many semiconductor junction failures. Power MOSFETs usually increase their on-resistance with temperature. Under some circumstances, power dissipated in this resistance causes more heating of the junction, which further increases the junction temperature, in a positive feedback loop. As a consequence, power MOSFETs have stable and unstable regions of operation. If a MOSFET transistor produces more heat than the heatsink can dissipate, then thermal runaway can still destroy the transistors. This problem can be alleviated to a degree by lowering the thermal resistance between the transistor die and the heatsink.

2. **Lower Threshold Voltage**:

During operation if the temperature rises, it can significantly reduce the threshold voltage V_T, (because thermionic emission over the barrier at the source side of the channel, becomes easier.) This increases the current, however higher current will lead to even more heat production, leading to thermal runaway.

3. **Lower Mobility**:

High heating in the device can lower the mobility, due to the increased phonon scattering. Which in turn reduces the current, thereby impeding the performance.

4. Thermal Overstress:

Excess heat can cause semiconductors to fail. Excess heat melts materials, chars plastics, warps and breaks semiconductor dies, and causes other types of damages. Three main problems due to Thermal overstressing are:

i. Encapsulation failure:

   These failures occur when the encapsulation used to package a device develops a fault as in a crack. Thermal stress and differences in the coefficient of thermal expansion between the encapsulation material and metal used for leads can cause the cracks to form. Moisture can enter the package during high humidity through these opening, and hinder the performance.

ii. Die-attach failure. Improper contact between the die and substrate decreases thermal conductivity between the two. As a result, the die can overheat, which leads to stressing and cracking, and thus device failure.

iii. Wire-bond failure. Thermal overstress due to high current flow, mechanical stress in the bond wire due to improper bonding, cracks at the interface between bond wire and die, electro migration of silicon, and excessive bonding pressure can each cause wire-bond failures. When a bond fails, so does the device, because one of its conductors no longer exists.

4.0

Using Graphene as a heat sink

i) What is Graphene:

Scientists have talked about graphene for a long time. We have unintentionally created small bits of it every time we write with a pencil on a piece of paper. Graphene has been first spotted under electron microscopes in the year 1962 by Hans-Peter Boehm. The material was later rediscovered, characterized and isolated by Andre Geim and Konstantin Novoselov in 2004 at the University of Manchester.

Graphene is a single layer, one atom thick lattice of carbon atoms. It can be identified as a single layer of a stack of Graphite, but has astonishing properties in comparison to its predecessor.

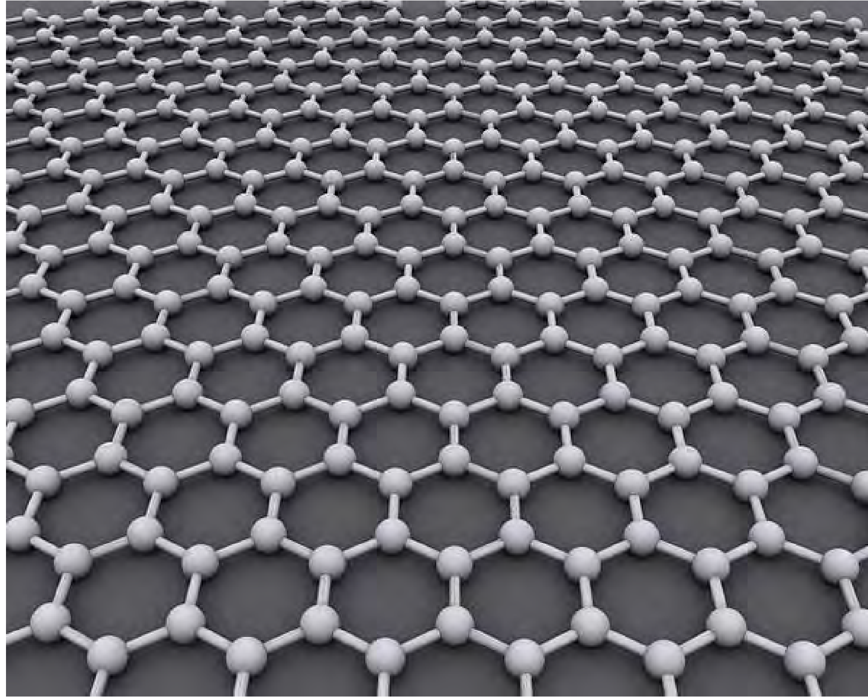


Fig: 4 (a) Single Layer, Hexagonal Lattice of Carbon Atoms (Graphene)

The resistivity of graphene sheets are near about, 10^{-6} Ω·cm. Lower than Silver, the lowest otherwise known at room temperature. The Thermal Conductivity is as high as 5300 $W \cdot m^{-1} \cdot K^{-1}$.

The conductivity of Pyrolytic Graphite is 2000 $W \cdot m^{-1} \cdot K^{-1}$

Below are a few pictures found from the video of a Youtuber showing how ice can be cut with the warmth of his hands just by using a graphene strip.

Fig: 4 (b) Using a graphene strip to cut through ice

Fig: 4 (c) Mid-way

Fig: (d) Fully cut through

Fig: (e) Using a steel knife to show the difference

Fig: 4 (f) Again with a graphene strip.

The high thermal conductivity of graphene can be used to create a heat sink embedded in the transistor, to reduce the heat inside, thereby increasing transistor performances. Graphene has a melting point of 5000K. At about 6000K (The Sun's surface temperature is 5,777K), the graphene starts to melt into a loosely coupled double bonded chain, before turning into a gas. Below is a list of the thermal conductivities of different materials, the list shows the thermal conductivity of Diamond the highest otherwise known.

Material	Thermal conductivity (cal/sec)/(cm^2 C/cm)	Thermal conductivity (W/m K)*
Diamond	...	1000
Silver	1.01	406.0
Copper	0.99	385.0
Gold	...	314
Brass	...	109.0
Aluminum	0.50	205.0
Iron	0.163	79.5
Steel	...	50.2
Lead	0.083	34.7
Mercury	...	8.3
Ice	0.005	1.6
Glass,ordinary	0.0025	0.8
Concrete	0.002	0.8
Water at 20° C	0.0014	0.6

Fig: 4 (g) Thermal Conductivities of different materials.

5.0

Theoretical Data for Thermal Conductivity of Graphene:

Self-heating is a big problem in optoelectronics and photonics. These facts gave way to recent interest to thermal properties of materials. Acoustic phonons (quanta of the crystal lattice vibrations) are the main heat carriers in a variety of material systems. The phonon and thermal

properties of nanostructures are different from those of bulk crystals. Semiconductor nanowires do not conduct heat as well as bulk crystals due to increased phonon - boundary scattering or changes in the density of states (DOS) and phonon dispersion. The thermal conductivity K of thin films and nanowires is usually lower than that of the corresponding bulk materials owing to the extrinsic effects such as phonon – boundary scattering. This may sound contradictory to our research, however theoretical studies suggested that phonon transport in strictly two-dimensional (2D) and one-dimensional (1D) systems can bring out exotic behavior, leading to theoretically infinitely large intrinsic thermal conductivity.

The first experimentation of heat conduction in graphene were carried out in 2007 at UC Riverside [Fig]. The investigation of the phonon transport was made possible with development of the optothermal Raman measurement technique. The experiments were performed with the suspended graphene layers exfoliated from the high-quality Kish (a scum of impure graphite) and highly ordered pyrolytic graphite. It was found that the thermal conductivity varies and can exceed that of the bulk graphite, which is ~2000 W/mK at room temperature (RT).

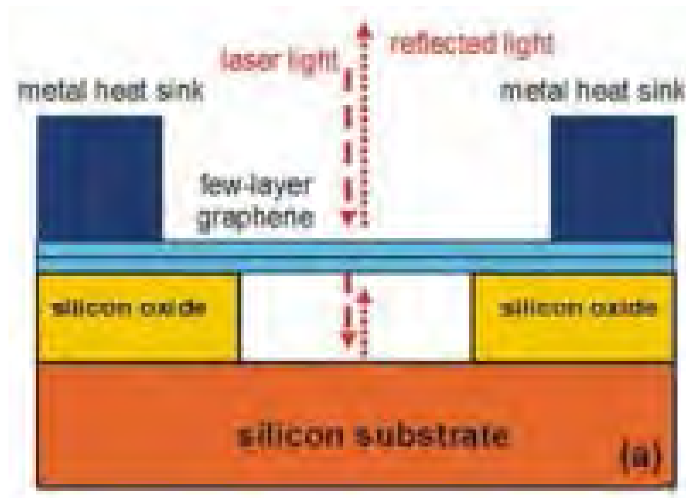


Fig:5 (a) Schematic of the thermal conductivity measurement showing suspended FLG flakes and excitation laser light

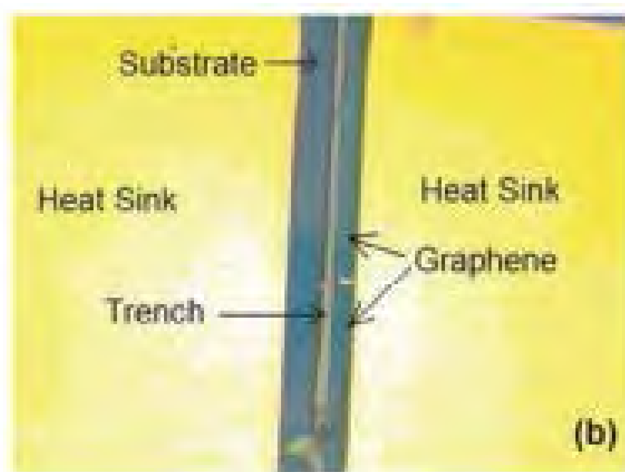


Fig: 5 (b) Optical microscopy images of FLG attached to metal heat sinks.

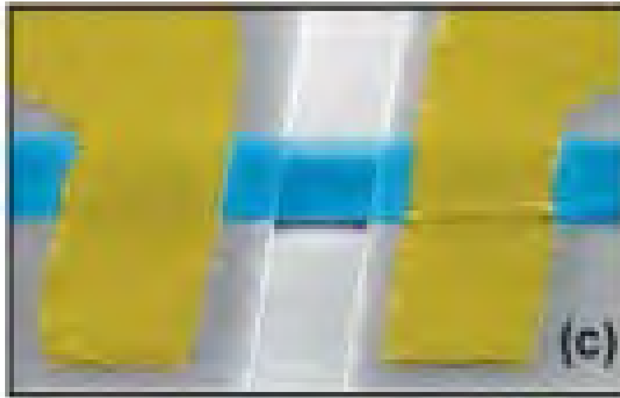


Fig: 5 (c) Colored scanning electron microscopy image of the suspended graphene flake to clarify a typical structure geometry

The first experimental study of the isotopic effects on the thermal properties of graphene was carried not too long ago from now. The isotopically modified graphene containing various percentages of 13C were synthesized by CVD technique. The thermal conductivity of the isotopically pure 12C (0.01% 13C) graphene, determined by the optothermal Raman technique was higher than 4000 W/mK at the temperature T~320 K, and more than a factor of two higher than the value of K in a graphene sheet composed of a 50%-50% mixture of 12C and 13C.

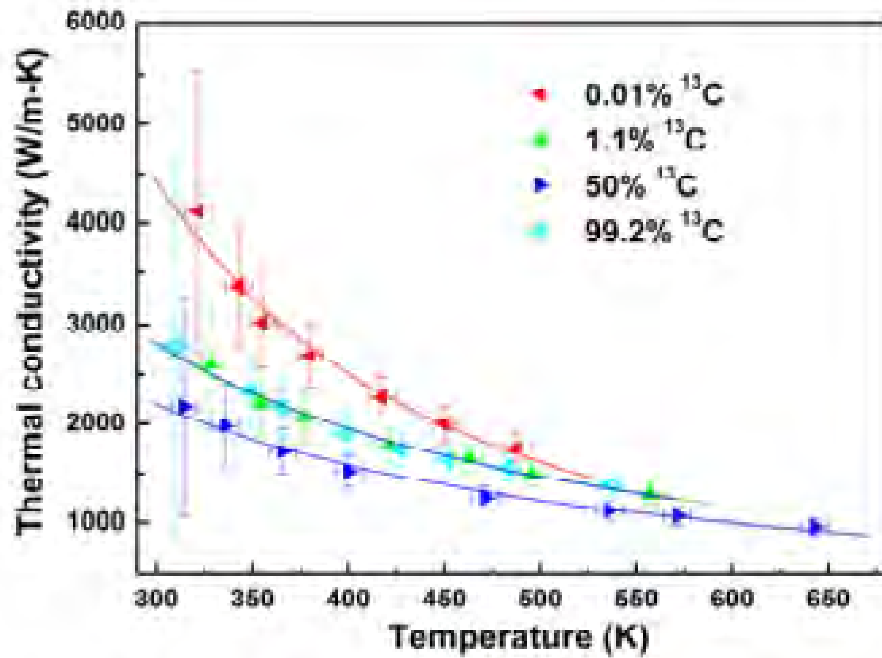


Fig: 5 (d) Thermal conductivity of graphene with 13C isotope concentrations of 0.01%, 1.1% (natural abundance), 50% and 99.2%, respectively, as a function of the temperature. The graph shows strong dependence of the thermal conductivity on the isotope concentration.

The thermal conductivity of graphene also depends substantially on its lateral size. Single Layer Graphene (SLG), Few Layer Graphene (FLG) etc. all reach different maximum temperatures at increasing thermal conductivities.

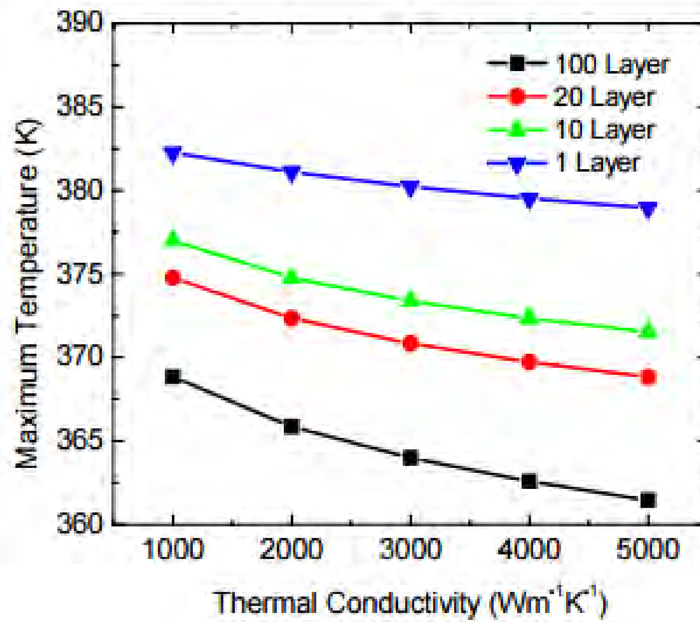


Fig: 5(e) Graph of Maximum Temperature Vs Thermal Conductivity

6.0

Heat Spreader:

Our idea is to use graphene heat spreaders inside a transistor, in the nanometer scale. We have used the paper, "*Graphene Heat Spreaders for Thermal Management of Nano electronic Circuits",* by SamiaSubrina and others (Reference cited below) to advance our research. The author talks about implementing a graphene heat spreader between the substrate and the SiO_2 layer. The schematic is shown below.

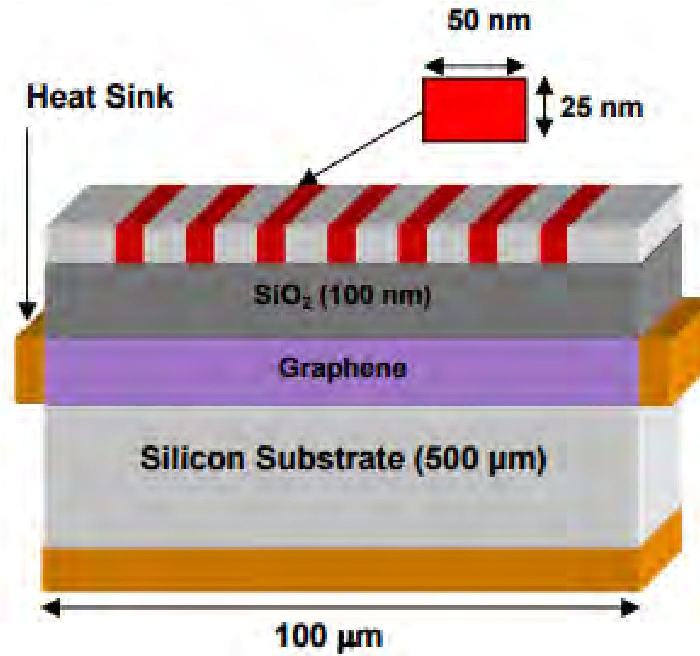


Fig: 6 (a) Schematic of SOI based circuit, with the graphene heat spreader attached to the side heat sinks.

The temperature profile has been shown in the paper. Without graphene heat spreader, the temperature of the device is higher, on the other hand with the use of graphene the device temperature falls drastically.

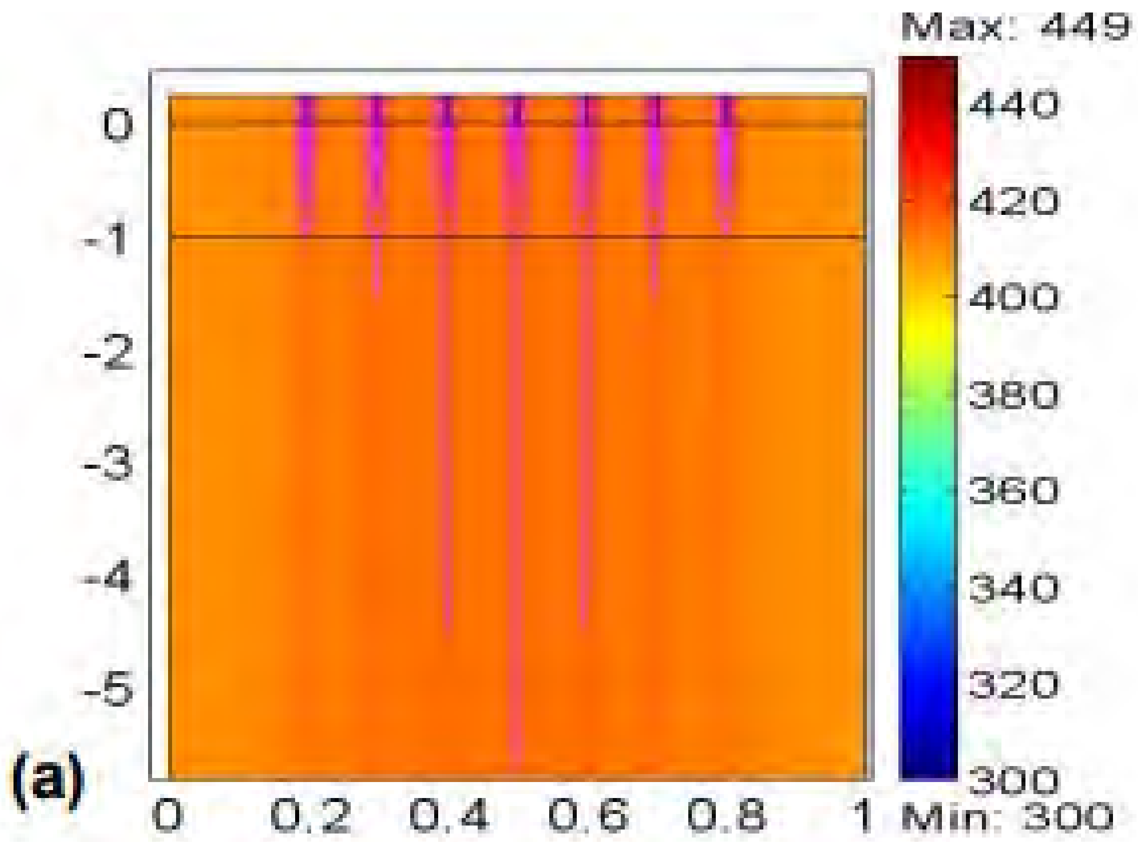


Fig: 6 (b) Temperature distribution across SOI-based circuit without graphene heat spreaders attached to the heat sink.

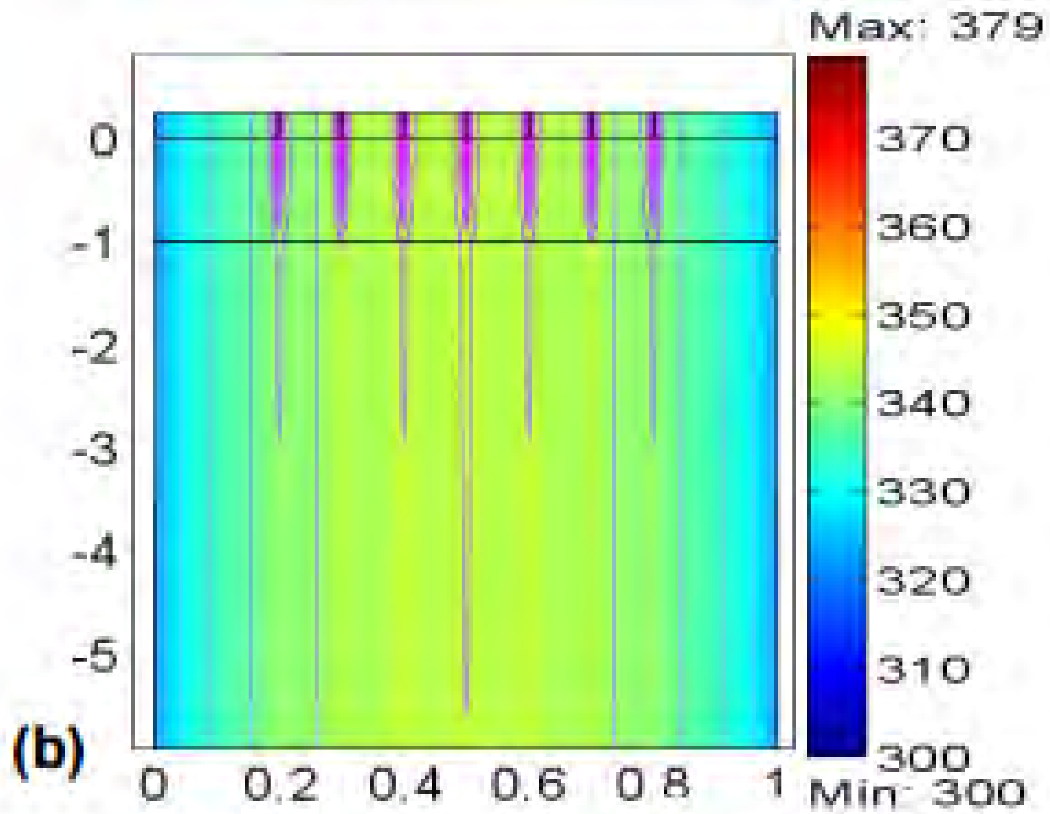


Fig: 6 (c) Temperature distribution across SOI-based circuit with graphene heat spreaders attached to the heat sink.

7.0

Figure of Merit

The efficiency of a thermoelectric device for electricity generation is given by η, defined as

$$\eta = \frac{\textbf{\textit{Energy Provided}}}{\textbf{\textit{Heat Energy absorbed at hot junction}}}$$

The ability of a given material to efficiently produce thermoelectric power is related to its dimensionless figure of merit given by:

$$ZT = \frac{S^2 \sigma T}{K}$$

Where,

S = Seebeck Coefficient

K = Thermal Conductivity

σ = Electrical Conductivity

T = Temperature

The equations shows us that Figure of merit is inversely proportional to the thermal conductivity.

i)

Thermal Conductivity (K):

Thermal conductivity is an intrinsic property of a material that measures the rate of heat conduction of a material. It is measured in watt per meter. Kelvin (W/m.K). Thermal conductivity (often denoted k or λ) is the property of a material to conduct heat.
Heat transfer occurs at a lower rate across materials of low thermal conductivity than across materials of high thermal conductivity. Correspondingly, materials of high thermal conductivity are widely used in heat sink/heat spreader applications and materials of low thermal conductivity are used as thermal insulation. The thermal conductivity of a material may depend on temperature. The reciprocal of thermal conductivity is called thermal resistivity.

ii)

Electrical Conductivity(σ):

Electrical conductivity is an intrinsic property of a material that measures the rate of flow of electrical charges through a material. It is measured in Siemens per meter (S/m).

Electrical conductivity (σ) is the reciprocal of electrical resistivity (ρ),

$$\sigma = 1/\rho$$

Where, resistivity ρ is proportional to resistance R of the material.

$$\rho = RA/L$$

A = cross-sectional area

L=length of the material

iii)

Thermoelectric Effects:

Seebeck effect is the phenomenon where a temperature difference at the junctions of two different materials produces voltage and thus electric current flows in the closed circuit

The voltage produced is proportional to the temperature difference between the two junctions and the proportionality constant (S) is the Seebeck coefficient

$$V=S\ (Th-Tc)$$

The voltage induced by Seebeck effect is found to be in microvolts per kelvin which is insignificant. However it increases with rise in the temperature difference in the junctions.

On the other hand, flow of electrical current would create or remove heat at the junction of two different metals. This is known as **Peltier Effect**. The heat absorbed or created at the junction is proportional to the electrical current and the proportionality constant Π is the Peltier coefficient.

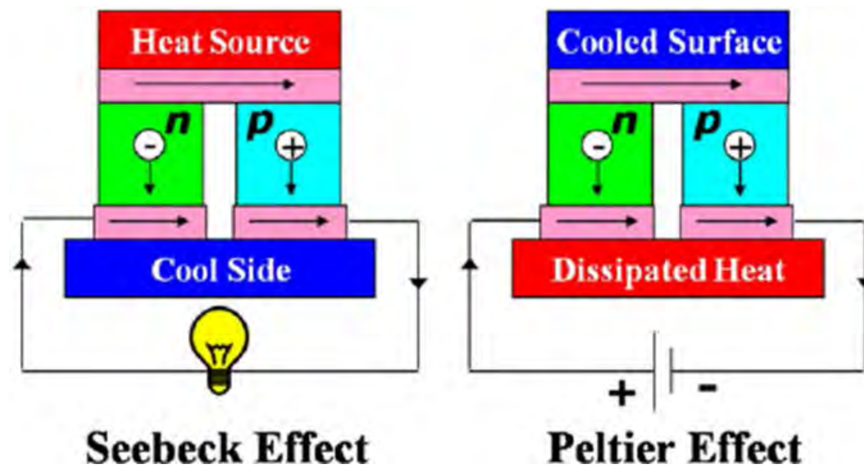


Fig:7 Seebeck and Peltier Effect

Thomson effect is described as the interrelationship between Seebeck effect and Peltier effect which states that heat is absorbed or produced when current flows in a material with a temperature gradient. The heat produced or removed in a material is proportional to the electric current and the temperature gradient and the proportionality constant is the Thomson coefficient.

8.0

Analysis using QuantumWise^{TM}

QuantumWise is a self-funded, privately owned company headquartered in Copenhagen, Denmark.QuantumWise develops commercial software for fast and reliable atomic-scale modeling of nanostructures, fully supported and delivered in a user friendly interface. Virtual NanoLab^{TM}(VNL) is an atomic scale modelling software for nanotechnology.

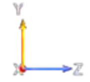
All our modelling, simulations and collection of data have been done using VNL-ATK Version 2016.4 (64-bit).

Using this software we modelled firstly a pure single layer of graphene nanosheet. Our main purpose is to design a suitable heat spreader for the nanoscale technology and for this we have chosen to use Graphene for its excellent thermal properties. We have calculated the values for σ, Π, S, k and thus ZT to study the characteristics of graphene with doped material and Bi/Multi layers. Simulation of the nanostructures include a device which contains a central region and two electrodes on each sides. In figure 1 all the designed nanostructures are shown. All the single layer graphene is measured as 0.2174 nm in length and 0.1914 nm in width. Then we have doped the structure with p-type (Boron and Aluminum) and n-type (Nitrogen and Sulfur) materials to study the impacts of impurity atoms in graphene properties. Furthermore, we designed bilayer and multilayer (n=4) graphene with the same measurements for each layer to compare the data.

Using transmission spectrum analysis, we have analyzed data for both Phonon and Electron Transmission Spectrum. We have then calculated values of electrical conductivity (σ), Peltier coefficient (Π), Seebeck coefficient(S), thermal conductivity (k) and lastly the Figure of Merit (ZT). The models of graphene layers (SLG,FLG) doped/undoped are shown below.

i)

Modelling:



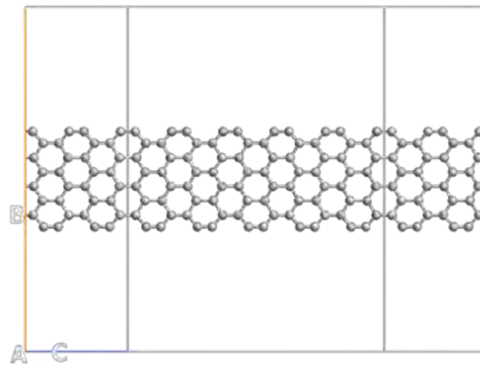
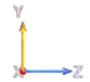


Figure 8.a Single Layer Graphene



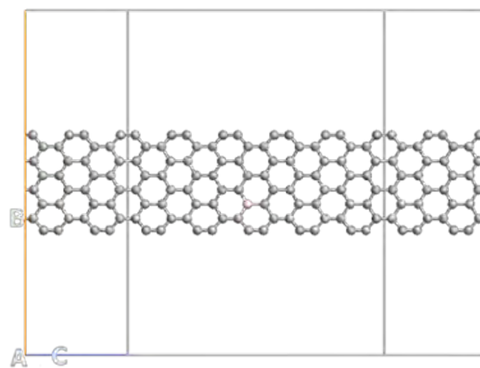
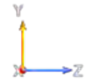


Figure 8.b. Boron doped Single Layer Graphene



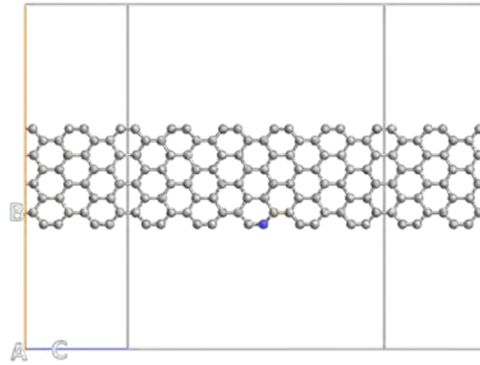
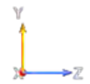


Figure 8.c. Nitrogen doped Single Layer Graphene



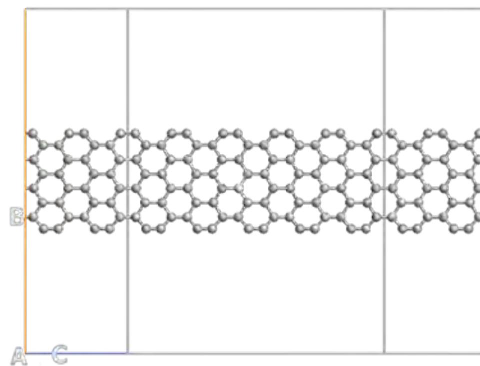
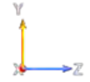


Figure 8.d. Aluminum doped Single Layer Graphene



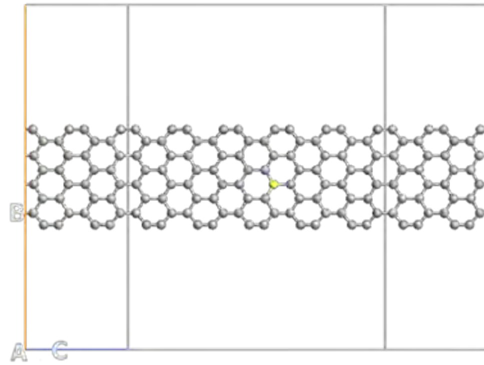


Figure 8.e. Sulfur doped Single Layer Graphene

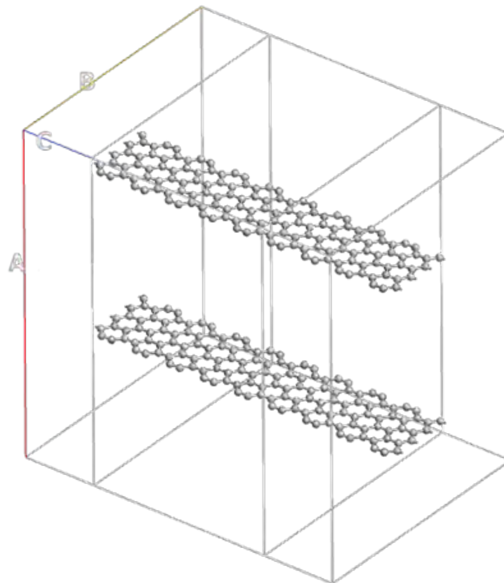


Figure 8.f. Bi Layer Graphene

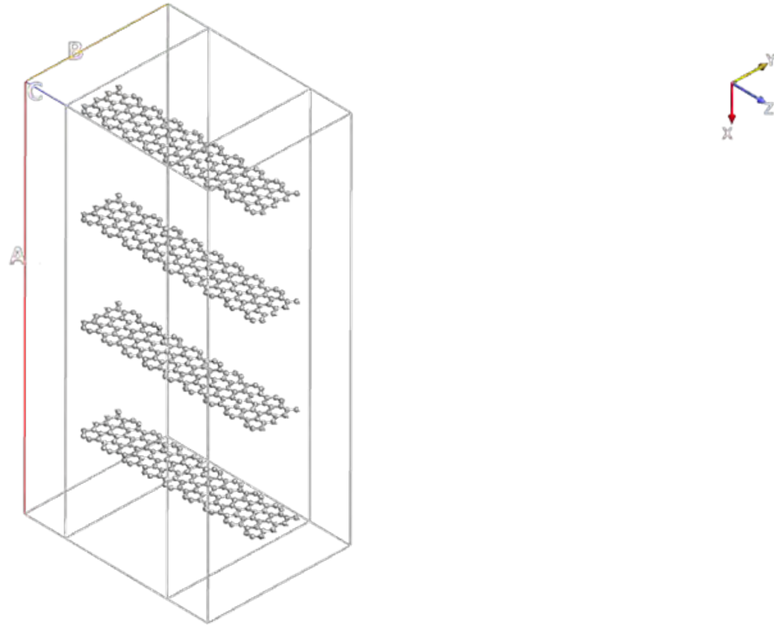


Figure 8.g. Multi Layer Graphene

ii)

Thermoelectric Properties with Change in Temperature:

We calculated the thermoelectric properties of Single-layer Graphene with/without doped material, and Bi/Multi-layer graphene with Temperature variation from 100K to 800K. The data are shown in Tables 1-7 which includes the electrical conductivity (σ*)*, Peltier coefficient (Π), Seebeck coefficient(S), thermal conductivity (k) and Figure of Merit (ZT).

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	6.274e-12	8.026e-07	8.026e-09	3.996e-10	1.011e-16
200	3.705e-08	3.319e-07	1.659e-09	8.259e-10	2.471e-14
300	6.228e-07	3.05e-07	1.017e-09	1.284e-09	1.504e-13
400	2.488e-06	2.801e-07	7.003e-10	1.772e-09	2.754e-13
500	5.606e-06	2.581e-07	5.162e-10	2.249e-09	3.32e-13
600	9.491e-06	2.385e-07	3.975e-10	2.689e-09	3.346e-13
700	1.366e-05	2.182e-07	3.118e-10	3.087e-09	3.012e-13
800	1.78e-05	1.692e-07	2.115e-10	3.446e-09	1.848e-13

Table 1: Single layer Graphene

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	3.435e-06	-0.0404	-0.000404	2.212e-10	0.2534
200	1.653e-05	-0.04505	-0.0002252	4.417e-10	0.3798
300	2.383e-05	-0.05316	-0.0001772	6.726e-10	0.3337
400	2.789e-05	-0.06049	-0.0001512	9.335e-10	0.2734
500	3.088e-05	-0.06466	-0.0001293	1.232e-09	0.2095
600	3.351e-05	-0.06551	-0.0001092	1.557e-09	0.1539
700	3.599e-05	-0.06393	-9.133e-05	1.888e-09	0.1113
800	3.836e-05	-0.06094	-7.617e-05	2.213e-09	0.08048

Table 2: boron doped (p type) single layer graphene (Fermi level shifted at 0.08eV)

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	3.377e-06	-0.0404	-0.000404	2.248e-10	0.2452
200	1.626e-05	-0.04506	-0.0002253	4.837e-10	0.3411
300	2.344e-05	-0.05317	-0.0001772	7.642e-10	0.289
400	2.744e-05	-0.06049	-0.0001512	1.07e-09	0.2346
500	3.038e-05	-0.06463	-0.0001293	1.409e-09	0.1802
600	3.297e-05	-0.06544	-0.0001091	1.766e-09	0.1332
700	3.541e-05	-0.0638	-9.114e-05	2.126e-09	0.09687
800	3.775e-05	-0.06074	-7.593e-05	2.473e-09	0.0704

Table 3: nitrogen doped (n type) single layer graphene (Fermi level shifted at 0.08eV)

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	3.77e-05	-0.001895	-1.895e-05	1.441e-10	0.009393
200	2.66e-05	-0.01477	-7.383e-05	2.31e-10	0.1255
300	2.482e-05	-0.02753	-9.177e-05	3.015e-10	0.208
400	2.463e-05	-0.0376	-9.4e-05	4.031e-10	0.216
500	2.514e-05	-0.04513	-9.026e-05	5.261e-10	0.1947
600	2.597e-05	-0.05126	-8.543e-05	6.532e-10	0.1741
700	2.689e-05	-0.05708	-8.154e-05	7.745e-10	0.1616
800	2.78e-05	-0.06321	-7.901e-05	8.875e-10	0.1564

Table 4.a: aluminum doped (p type) single layer graphene (Fermi level shifted at 0.08eV)

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	4.952e-05	-0.000524	-5.244e-06	1.707e-10	0.000798
200	3.859e-05	-0.005317	-2.659e-05	3.111e-10	0.01754
300	3.647e-05	-0.01357	-4.525e-05	3.839e-10	0.05835
400	3.49e-05	-0.02334	-5.834e-05	4.635e-10	0.1025
500	3.391e-05	-0.03293	-6.586e-05	5.612e-10	0.1311
600	3.344e-05	-0.04174	-6.957e-05	6.703e-10	0.1449
700	3.332e-05	-0.04986	-7.123e-05	7.828e-10	0.1512
800	3.343e-05	-0.05759	-7.199e-05	8.935e-10	0.1551

Table 4.b: aluminum doped (p type) single layer graphene (Fermi level shifted at 0.12eV)

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	5.589e-05	-0.000287	-2.874e-06	1.805e-10	0.0002558
200	4.462e-05	-0.002663	-1.331e-05	3.582e-10	0.004416
300	4.343e-05	-0.007321	-2.44e-05	4.6e-10	0.01687
400	4.223e-05	-0.01427	-3.569e-05	5.468e-10	0.03934
500	4.108e-05	-0.02255	-4.51e-05	6.37e-10	0.06557
600	4.015e-05	-0.03126	-5.21e-05	7.337e-10	0.08913
700	3.948e-05	-0.03995	-5.707e-05	8.347e-10	0.1079
800	3.905e-05	-0.04847	-6.059e-05	9.372e-10	0.1224

Table 4.c: aluminum doped (p type) single layer graphene (Fermi level shifted at 0.16eV)

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	6.057e-05	-0.000207	-2.073e-06	1.866e-10	0.0001395
200	4.864e-05	-0.001783	-8.915e-06	3.849e-10	0.002009
300	4.793e-05	-0.004658	-1.553e-05	5.134e-10	0.006751
400	4.725e-05	-0.009365	-2.341e-05	6.207e-10	0.01669
500	4.64e-05	-0.01571	-3.141e-05	7.193e-10	0.03183
600	4.554e-05	-0.02313	-3.856e-05	8.154e-10	0.04982
700	4.477e-05	-0.03115	-4.45e-05	9.113e-10	0.0681
800	4.412e-05	-0.03944	-4.93e-05	1.008e-09	0.08515

Table 4.d: aluminum doped (p type) single layer graphene (Fermi level shifted at 0.20eV)

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	1.699e-06	-0.04045	-0.0004045	7.414e-11	0.3749
200	8.299e-06	-0.04568	-0.0002284	1.581e-10	0.5477
300	1.224e-05	-0.05419	-0.0001806	2.297e-10	0.5213
400	1.463e-05	-0.06042	-0.0001511	3.204e-10	0.4169
500	1.651e-05	-0.06133	-0.0001227	4.479e-10	0.2773
600	1.822e-05	-0.05692	-9.487e-05	6.035e-10	0.1631
700	1.986e-05	-0.04857	-6.939e-05	7.698e-10	0.08695
800	2.142e-05	-0.03777	-4.722e-05	9.33e-10	0.04096

Table 5.a: sulfur doped (n type) single layer graphene (Fermi level shifted at 0.08eV)

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	4.634e-05	-0.001693	-1.693e-05	1.045e-10	0.01271
200	3.155e-05	-0.01335	-6.674e-05	2.245e-10	0.1252
300	2.822e-05	-0.0254	-8.467e-05	2.884e-10	0.2104
400	2.663e-05	-0.03599	-8.997e-05	3.467e-10	0.2487
500	2.577e-05	-0.04385	-8.771e-05	4.243e-10	0.2336
600	2.538e-05	-0.0478	-7.967e-05	5.288e-10	0.1828
700	2.534e-05	-0.04743	-6.776e-05	6.556e-10	0.1242
800	2.555e-05	-0.0431	-5.388e-05	7.947e-10	0.07465

Table 5.b: sulfur doped (n type) single layer graphene (Fermi level shifted at 0.12eV)

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	5.446e-05	-0.000215	-2.149e-06	1.328e-10	0.0001893
200	4.2e-05	-0.0031	-1.55e-05	3.071e-10	0.006569
300	3.882e-05	-0.009356	-3.119e-05	3.769e-10	0.03005
400	3.6e-05	-0.01725	-4.313e-05	4.196e-10	0.06384
500	3.369e-05	-0.02496	-4.992e-05	4.656e-10	0.09017
600	3.192e-05	-0.03099	-5.165e-05	5.283e-10	0.0967
700	3.063e-05	-0.03429	-4.898e-05	6.114e-10	0.08412
800	2.973e-05	-0.03435	-4.294e-05	7.126e-10	0.06154

Table 5.c: sulfur doped (n type) single layer graphene (Fermi level shifted at 0.16eV)

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	5.497e-05	4.761e-05	4.761e-07	1.365e-10	9.129e-06
200	4.365e-05	-5.673e-05	-2.836e-07	3.394e-10	2.069e-06
300	4.201e-05	-0.001959	-6.531e-06	4.375e-10	0.001229
400	4.009e-05	-0.005886	-1.472e-05	4.88e-10	0.007116
500	3.8e-05	-0.01087	-2.174e-05	5.232e-10	0.01717
600	3.601e-05	-0.01569	-2.615e-05	5.613e-10	0.02632
700	3.427e-05	-0.01926	-2.751e-05	6.12e-10	0.02966
800	3.282e-05	-0.0208	-2.599e-05	6.789e-10	0.02613

Table 5.d: sulfur doped (n type) single layer graphene (Fermi level shifted at 0.20eV)

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	1.255e-11	8.026e-07	8.026e-09	7.993e-10	1.011e-16
200	7.411e-08	3.319e-07	1.659e-09	1.652e-09	2.471e-14
300	1.246e-06	3.05e-07	1.017e-09	2.568e-09	1.504e-13
400	4.976e-06	2.801e-07	7.003e-10	3.545e-09	2.754e-13
500	1.121e-05	2.581e-07	5.162e-10	4.498e-09	3.32e-13
600	1.898e-05	2.385e-07	3.975e-10	5.379e-09	3.346e-13
700	2.733e-05	2.182e-07	3.118e-10	6.175e-09	3.012e-13
800	3.561e-05	1.692e-07	2.115e-10	6.893e-09	1.848e-13

Table 6: Bi Layer Graphene

T (K)	σ (S)	Π (V)	S (V/K)	k (W/K)	ZT
100	2.51e-11	3.531e-07	3.531e-09	1.599e-09	1.957e-17
200	1.482e-07	3.314e-07	1.657e-09	3.304e-09	2.464e-14
300	2.491e-06	3.05e-07	1.017e-09	5.136e-09	1.504e-13
400	9.952e-06	2.801e-07	7.003e-10	7.089e-09	2.754e-13
500	2.242e-05	2.581e-07	5.162e-10	8.996e-09	3.32e-13
600	3.796e-05	2.385e-07	3.975e-10	1.076e-08	3.346e-13
700	5.466e-05	2.182e-07	3.118e-10	1.235e-08	3.012e-13
800	7.122e-05	1.692e-07	2.115e-10	1.379e-08	1.848e-13

Table 7: Multi Layer Graphene

The tabular data has then been fed to Matlab, to bring out a graphical analysis as a summary of all our findings. The graphs have been shown below.

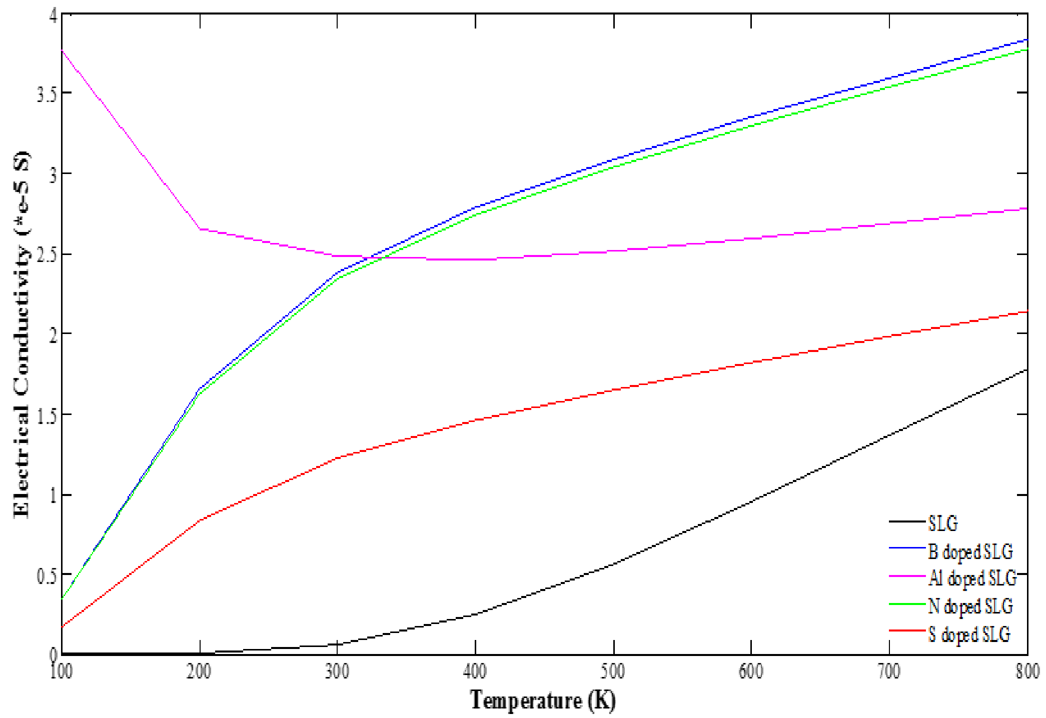


Figure 3.a. Electrical Conductivity vs Temperature for SLG/doped SLG

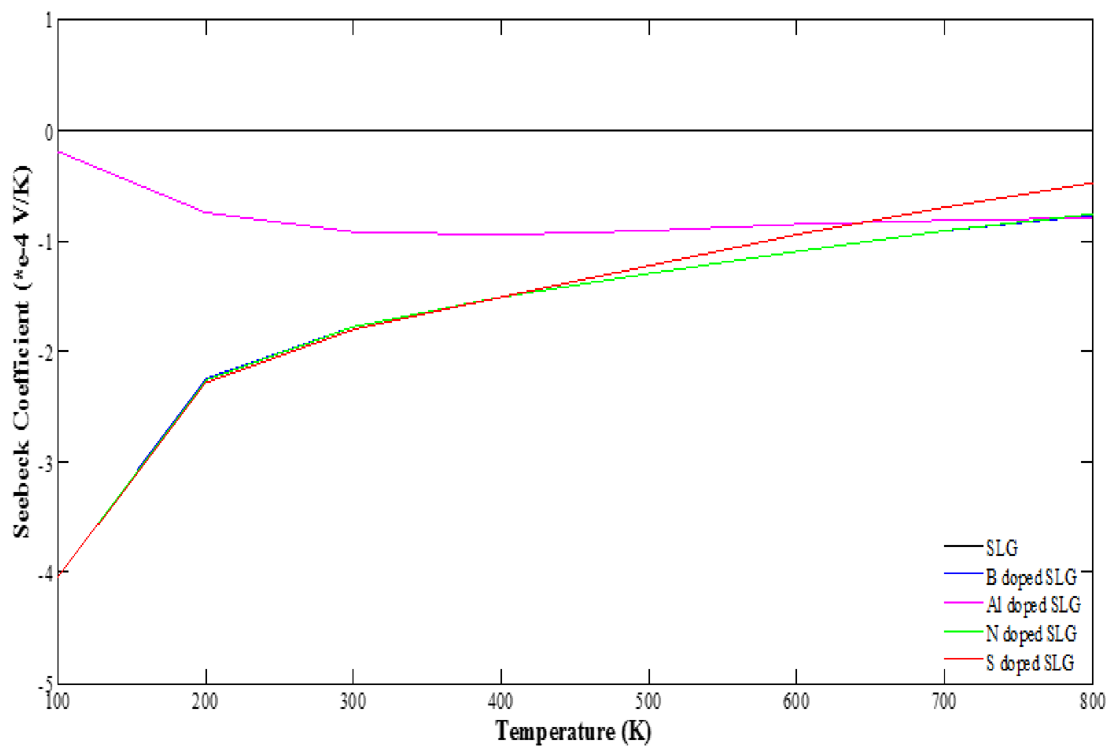


Figure 3.b. Seebeck Coefficient vs Temperature for SLG/doped SLG

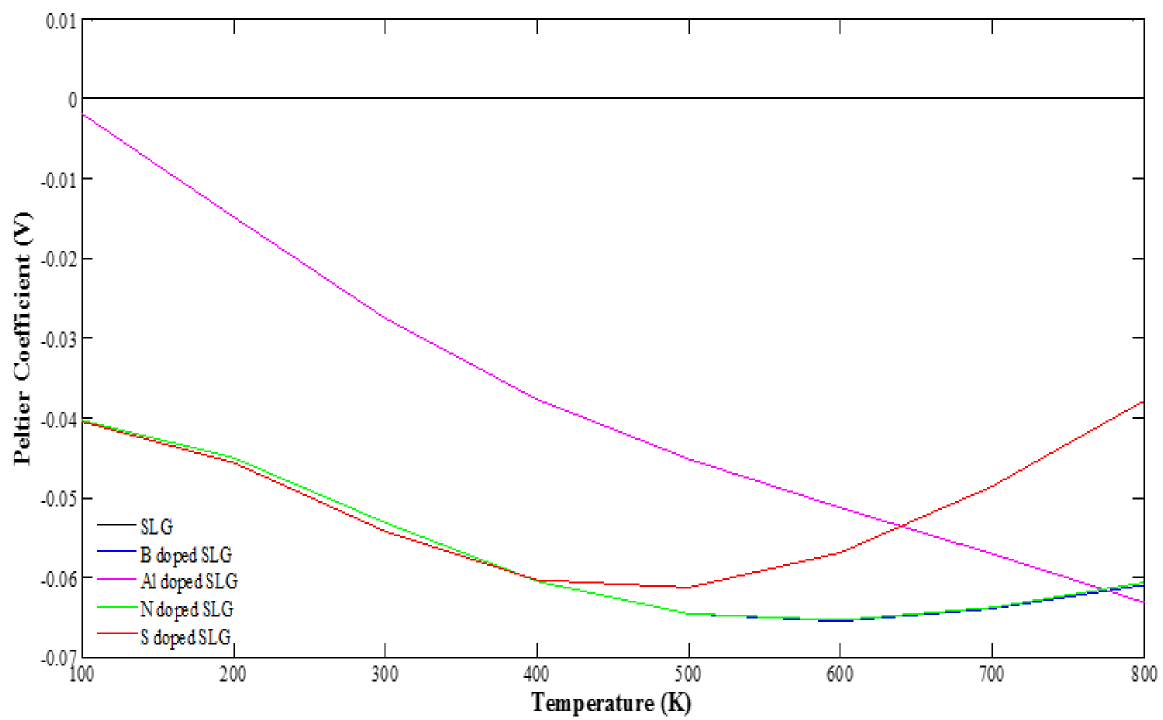


Figure 3.c. Peltier Coefficient vs Temperature for SLG/doped SLG

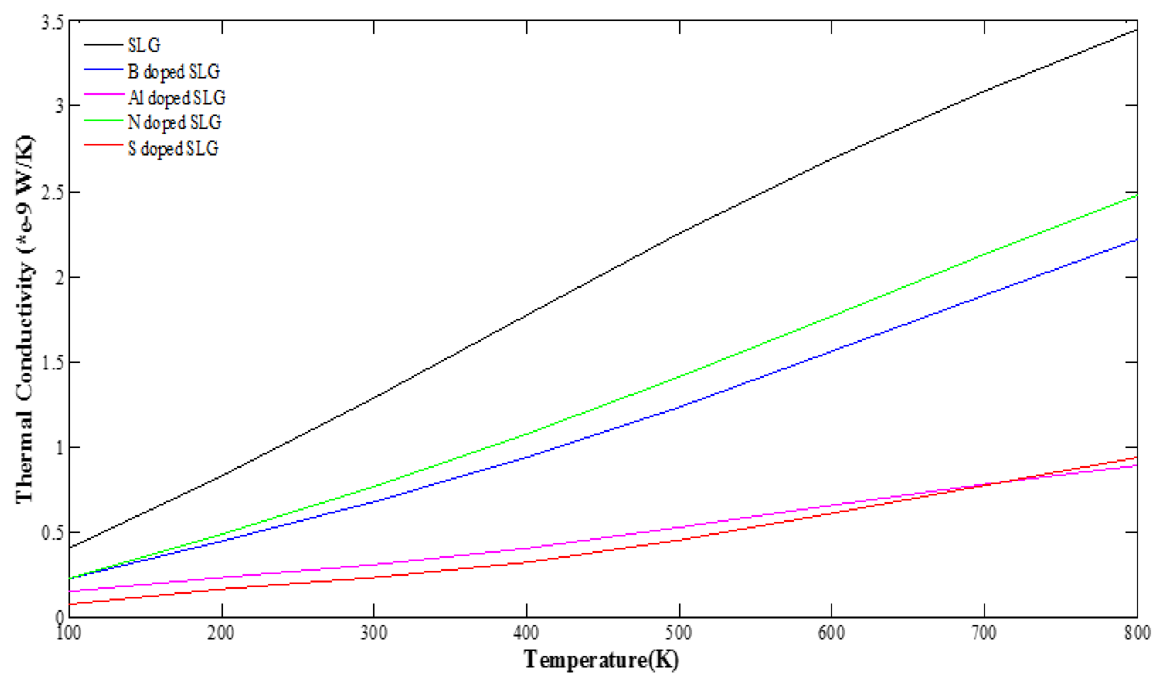


Figure 3.d. Thermal Conductivity vs Temperature for SLG/doped SLG

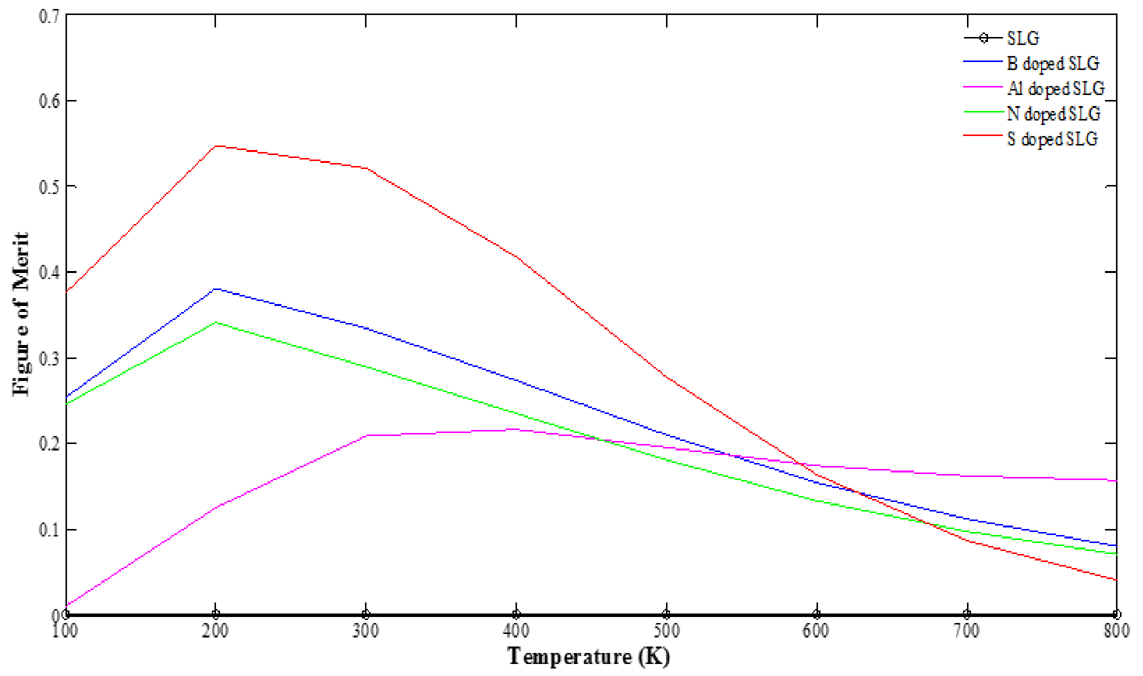


Figure 3.e. Figure of Merit vs Temperature for SLG/doped SLG

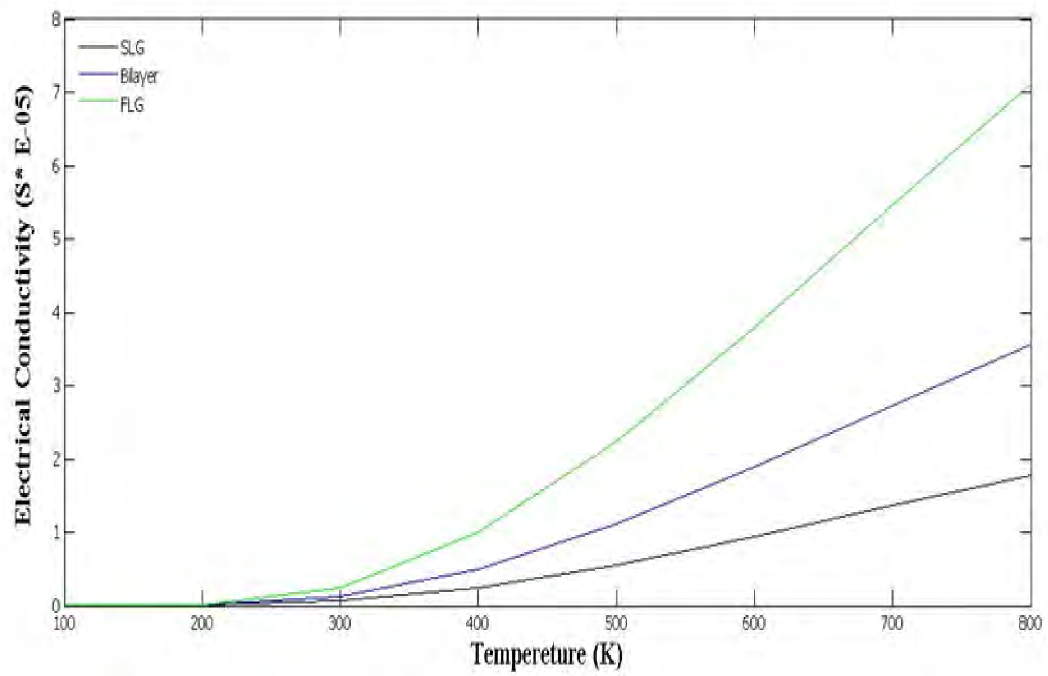


Figure 4.a. Electrical conductivity vs Temperature for SLG/BLG/FLG

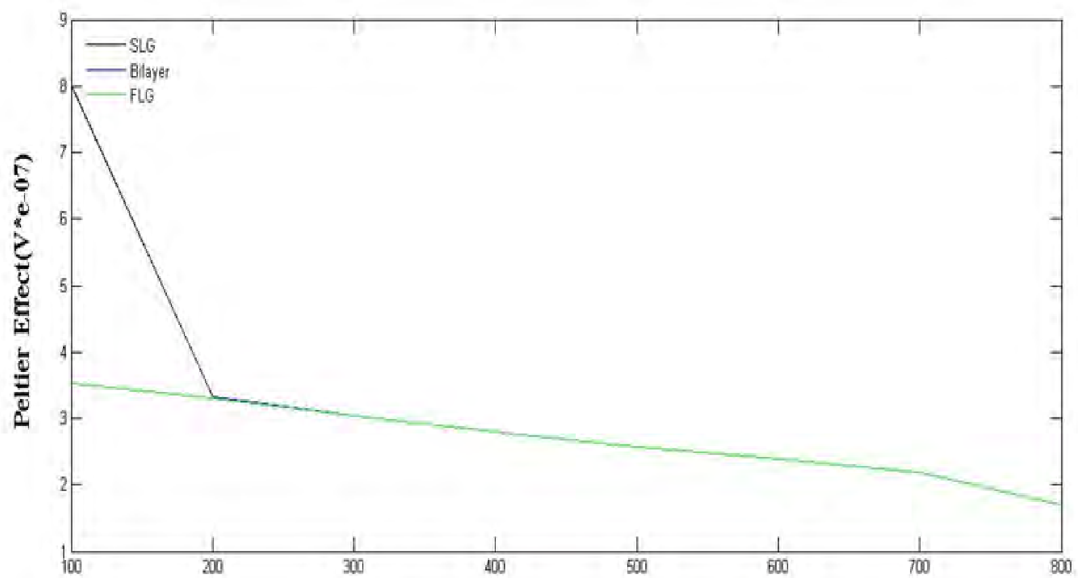


Figure 4.b. Peltier Coefficient vs Temperature for SLG/BLG/FLG

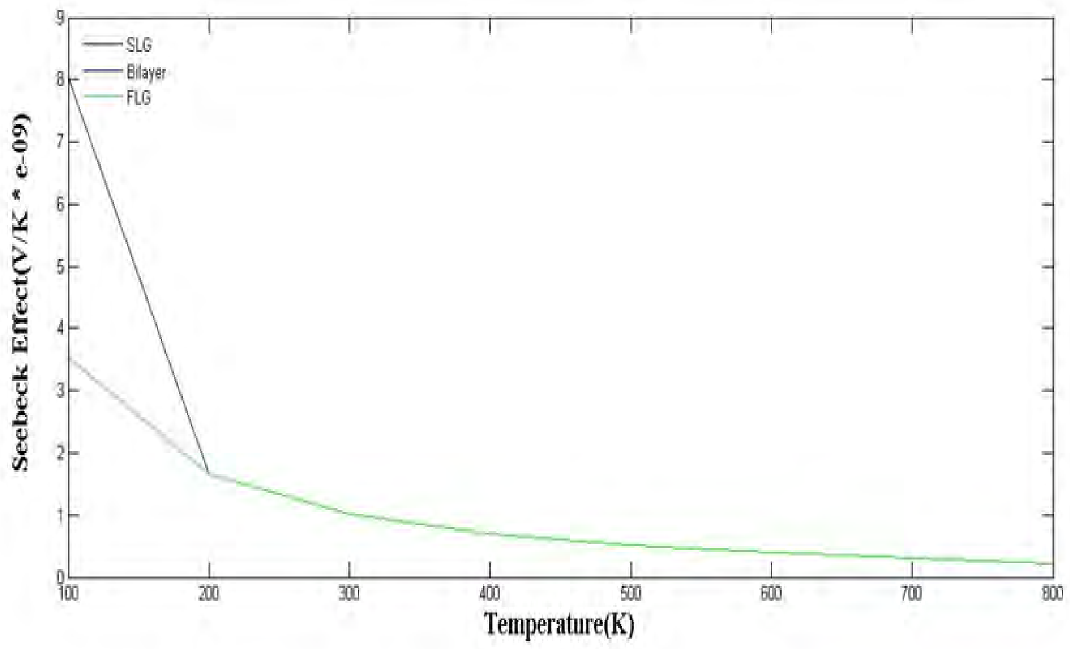


Figure 4.c. Seebeck Coefficient vs Temperature for SLG/BLG/FLG

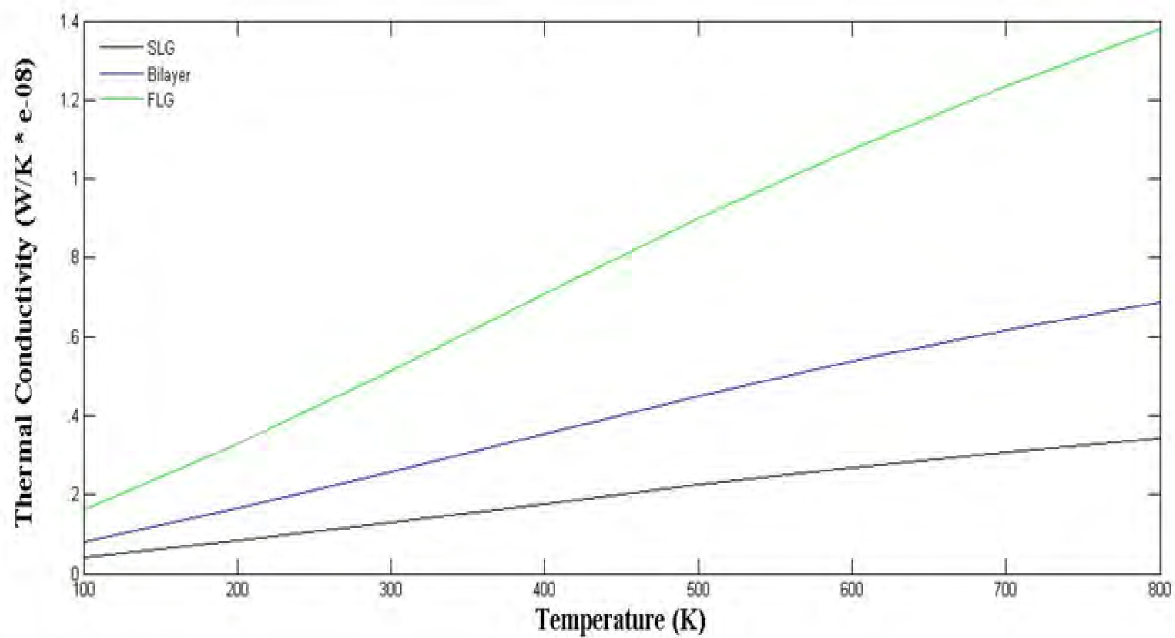


Figure 4.d. Thermal Conductivity vs Temperature for SLG/BLG/FLG

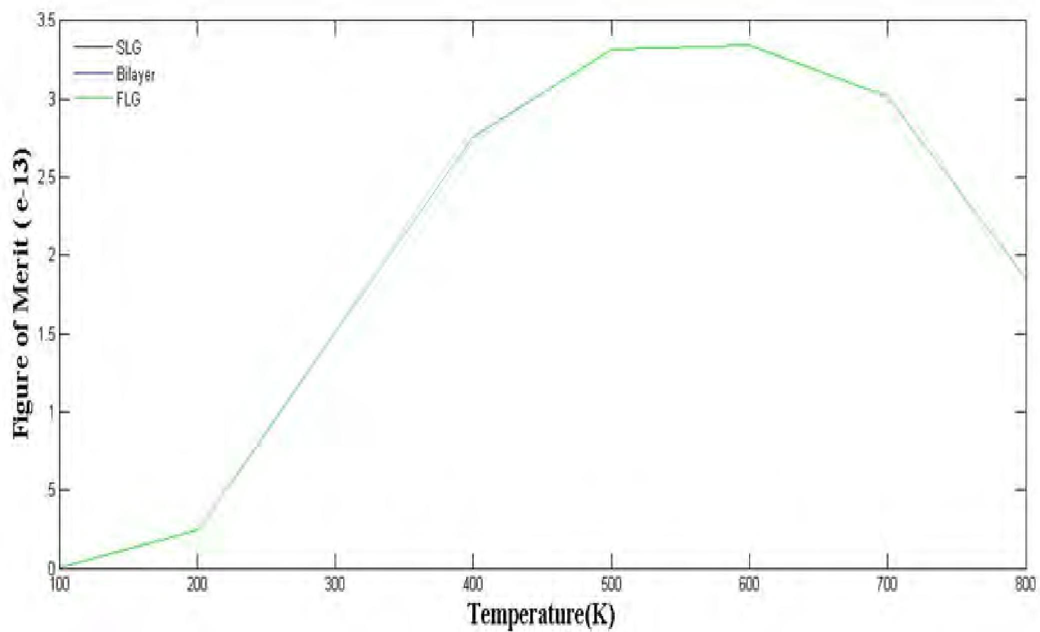


Figure 4.e. Figure of Merit vs Temperature for SLG/BLG/FLG

9.0

Conclusion:

From figures 3-4 it can be seen that electrical conductivity of doped SLG is much higher than pure SLG which increases the performance of the device. It is also seen to be increased with rise

in temperature, where boron doped and nitrogen doped SLG represents similarities and sulfur doped SLG has lower values of electrical conductivity for the doped SLG. An exception is seen in the behavior of aluminum doped SLG which decreases with temperature and then increases above 400K. The peltier coefficient and thus, seebeck coefficient is lowered with negative values for both p-type and n-type doped SLG. However, thermal conductivity is higher for pure graphene which further increases with temperature. As a result, figure of merit is significantly lower for SLG which can be increased much higher with impurity atoms. It is illustrated in figure 3.e where ZT of SLG is found to be 10^{-12}~10^{-15} times lower than doped SLG. Therefore, pure graphene thus holds the best stance as a heat spreader.

Moreover, with increase in layer graphene shows higher electrical conductivity than single layer graphene, which is illustrated in figure 3. It is seen that for temperatures from 100~400K electrical conductivity has insignificant change which increases drastically with more number of layers. It is also found that peltier effect and seebeck effects does not change with the number of layer for temperatures above 200K. The thermal conductivity also increases further more with more number of layers (which is highest at 800K for multi-layer graphene found to be 1.379e-08 W/K). Therefore, if we design the heat spreader with bi/multi-layer graphene instead of SLG it would dissipate heat from the device more efficiently. Also, we see that the device performance is increased with much higher electrical conductivity with rise in the layers (even higher than doped SLG with increased temperature which is highest at 800K for multi-layer graphene found to be 7.122e-05 Siemens). However, the figure of merit remains unchanged in this case.

We further changed the impurity concentrations of the doped materials to study the impact in the characteristics which is illustrated in tables 4.a-d for aluminum and 5.a-d for sulfur. We increased the impurity concentrations at shifted fermi level from 0.08eV to 0.12eV, 0.16eV and 0.20eV.

From table 4.a-d, it is seen that for p-type (Al doped) material of graphene electrical conductivity increases, peltier and thus seebeck effect decreases negligibly, thermal conductivity also increases insignificantly and thus figure of merit decreases with temperature for higher impurity concentration.

From table 5.a-d, a similar behavior with increase in impurity concentration for n-type (S doped) material of graphene is found in increase in electrical conductivity, decrease in peltier and

seebeck effect, increase in thermal conductivity and thus, decrease in figure of merit with temperature.

However, the impact of the impurity atoms is not of that much of significance in terms of heat spreader, as even though it increases with rise in concentration it is much lower than pure graphene. Performance of the device can also be increased with increase in number of layer more effectively than higher impurity concentration for graphene.

The first experimental demonstration of graphene heat spreaders on high-power electronic device was achieved by transferring mechanical exfoliated FLG on GaN transistors. However, this method cannot be applied in semiconductor industry due to the limited graphene flake size, varied flake shape and thickness. The practical applications of graphene heat spreaders will rely on a method that can produce high quality, large sized graphene flakes, but not be compromised for price to be economical.There are numerous ways graphene can be produced. Among many Chemical Vapour Deposition (CVD) is a popular choice.However there is a trade-off.The reported thermal conductivity of CVD grown graphene is lower than that of exfoliated graphene flakes, but still larger than conventional semiconductors or metals used in electronic devices. In a recent work, CVD grown graphene of different number of layers was fabricated and it was demonstrated as heat spreader in thermal packaging. A platinum microheater embedded chips were used to evaluate the performance of the graphene heat spreaders. The Pt microheater made of titanium/platinum/gold (Ti/Pt/Au) provided heating source and temperature sensor. CVD grown single-layer and multilayer graphene were synthesized on copper substrate and then transferred onto the thermal evaluation chips as heat spreaders. Pt microheater was driven by electric current as hot spot, in which the temperature rise can be calculated by measuring the electric resistance. Thermal performance of the graphene heat spreaders was evaluated by the temperature drop after graphene transfer. It was found that the temperature of hotspot driven at a heat flux up to 430 Wcm-2 was decreased from 121 ^{o}C to 108°C ($\Delta T = 13^{o}$C) after introduction of SLG heat spreader. These results prove the potential of CVD grown graphene as a promising heat spreader material for hot spot cooling in electronic devices.

CVD on a Nickel substrate is a popular and established method of graphene extraction.

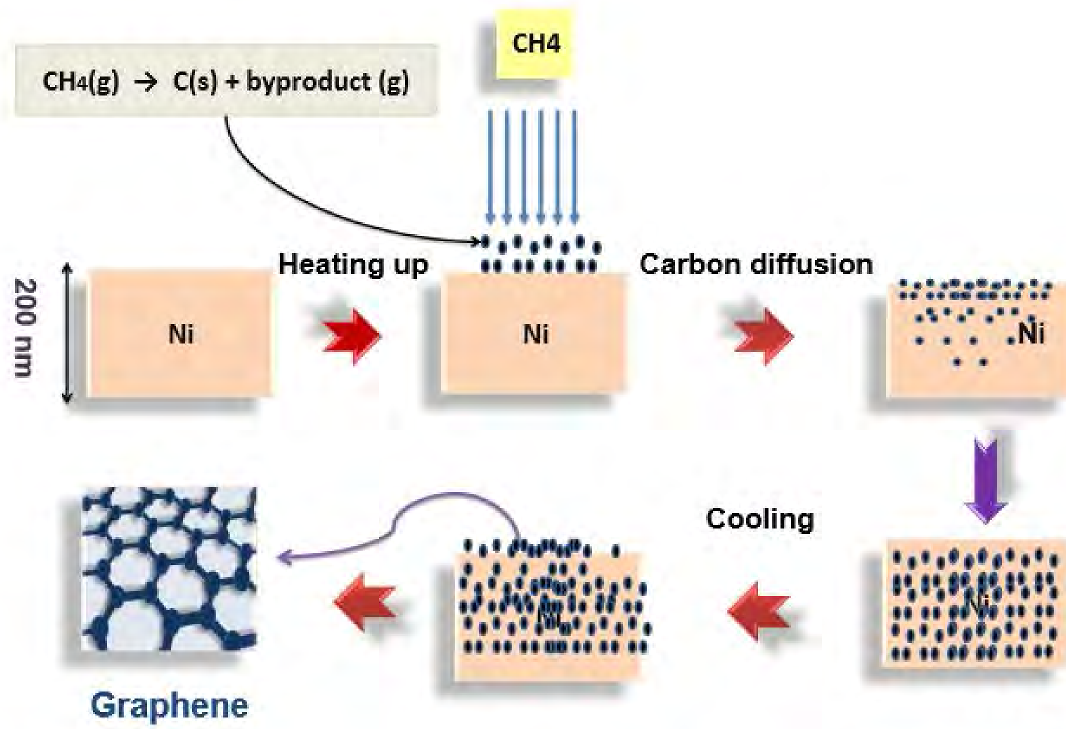


Fig: 9 CVD on Ni substrate

10.0

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