Simulation based electrostatic study of different multigate QuantumWell Field Effect Transistors by changing the gate oxide thickness and metal work function.

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ABSTRACT

This paper analyses the C-V characteristics by altering the gate oxide thickness and metal workfunction used in the gate of non-planer, multi-gate InGaAs channel Quantum Well Field-Effect Transistor (QWFET). In this paper, we tried to distinguish the different aspects of modern day transistors which lead us to the conclusion about the upcoming worldwide uses of QWFET in many electronic devices. Simulations were carried out using COMSOL Multiphysics linked with MATLAB simulator by incorporating various electrostatic parameters of different semiconductor materials in suitable domains with suitable boundary conditions. Poisson solver coupled with Schrodinger equation is used to obtain charge density in each point of the channel region of QWFET, and integrating the overall charge density we obtain total charge. In this way, charge accumulated in the channel region is obtained by altering gate voltage and a graph of charge versus gate voltage is obtained, which is further differentiated with respect to gate voltage to obtain graphs of gate capacitance versus gate voltage by changing the above mentioned parameters.

DATA SHEET

1. Electrostatic properties for 3 different compound semiconductor materials

Properties	InP	InAlAs	InGaAs
Number of states in 1cm3	3.96E22	4.34E22	3.79E22
Density	4.81g/cm3	4.5868g/cm3	5.47g/cm3
Electron affinity	4.38ev	3.5742eV	3.21eV
lattice constant	5.8687A	5.66A	5.3678A
Energy Gap	1.344ev	1.99eV	0.74eV
Nc	5.7E17/cm3	1.96E19/cm3	2.1E17/cm3
Nv	1.1E19/cm3	1.24E19/cm3	6.80E19/cm3
Intrinsic Carrier concentration	1.37E7/cm3	2.5E2/cm3	6.7E11/cm3
Electron Mobility	5200cm2/V/s	231.1cm2/V/s	10225cm2/V/s
Hole mobility	200cm2/V/s	77.57cm2/V/s	275cm2/V/s
Melting point	1333K	1362.64K	1373K
Speci c heat capacity	0.31J/g/K	0.3864J/g/K	0.34J/g/K
Thermal conductivity	0.68W/cm/K	0.10W/cm/K	0.23W/cm/K
Electron Thermal velocity	3.9E5m/s	2.3E5m/s	8.21E7m/s
Hole Thermal velocity	1.7E5m/s	1.565E5m/s	3.49E6m/s
Dielectric constant	11.926	11.5652	13.65

2. EFFECTIVE MASSES OF SOME COMPOUND SEMICONDUCTORS

1. GaAs → 0.067 Mo (electron effective mass)
   0.45Mo (hole effective mass)
2. InP → 0.077 Mo (electron)
   0.56Mo (hole)
3. InAs → 0.027 Mo (electron)
   0.41Mo (hole)
4. InGaAs → 0.047 Mo (electron)
   0.051 Mo (hole)
5. InAlAs → 0.067 Mo (electron)
   0.81 Mo (hole)

Where Mo = 9.11*10^-31 kg

3 Work function of some compound semi-conductor devices

- InP→ 4.05 eV
- InAlAs→ 4.10 eV
- InGaAs→ 4.08 eV

INTRODUCTION

1.1 History of emergence of Transistor

Living as we do in the 21st century, we are bounded by lots of electronic devices without which our life would have been very much complicated and difficult. One of the most importantfeatures in most electronic devices is switching, which to a large extent depends upon transistors. One of the switching element, known as triode, basically a vacuum was first invented by Lee De Forest in 1906. It consists of a cathode and a plate, separated by a control grid, suspended in a glass vacuum tube. The cathode is heated by a red-hot electric filament, which causes it to emit electrons that are attracted to the plate. But the tube was inefficient as a switch. It consumed a great deal of electrical power and gave off enormous heat. Few years later after triode was invented, a new era was created in the history of electronics as the first ever Field Effect Transistor (FET) was invented. The first FET was invented in 1947 by Bell Labs , supervised by John Bardeen, William Shockley and Walter Brattain. A FET has three terminalsnamely the gate, source and drain. A FET uses an electric field to control the shape and hence the electrical conductivity of a channel and hence controlling the amount of current flowing in a semiconductor material . A small change in gate voltage can cause a large variation in the current from the source to the drain. In 1952, after realizing that the point-contact structure had serious limitations, Shockley worked alone to conceive a more reliable and reproducible device and introduced Shockley's bipolar junction transistor. It was made from a solid piece of semiconductor material and no point contacts, dominated the industry for the next 30 years. The first ever commercially produced FET was Junction FET (JFET) which controls the channel conductance by altering the gate voltage. Soon after, Metal Oxide Semiconductor Field Effect Transistor (MOSFET) was invented that works by electronically varying the width of a channel along which charge carriers (electron s or hole s) flow. The MOSFET has certain advantages over the conventional junction FET, or JFET. Because the gate is insulated electrically from the

channel, no current flows between the gate and the channel, no matter what the gate voltage. Due to its high sensitivity on electrostatic charge, MOSFET can easily be destroyed when one touches the pin of MOSFET and so MOSFET was more reliable FET was introduced. HEMT is one such FET. High Electron Mobility Transistor, also known as hetero-structure FET (HFET) or modulation-doped FET (MODFET) is a field-effect transistor incorporating a junction between two materials with different band gaps. HEMTs have attracted attention due to their high-power performance. And gradually after HEMT was introduced, another type of FET was invented which is known as Quantum Well Field Effect Transistor (QWFET).

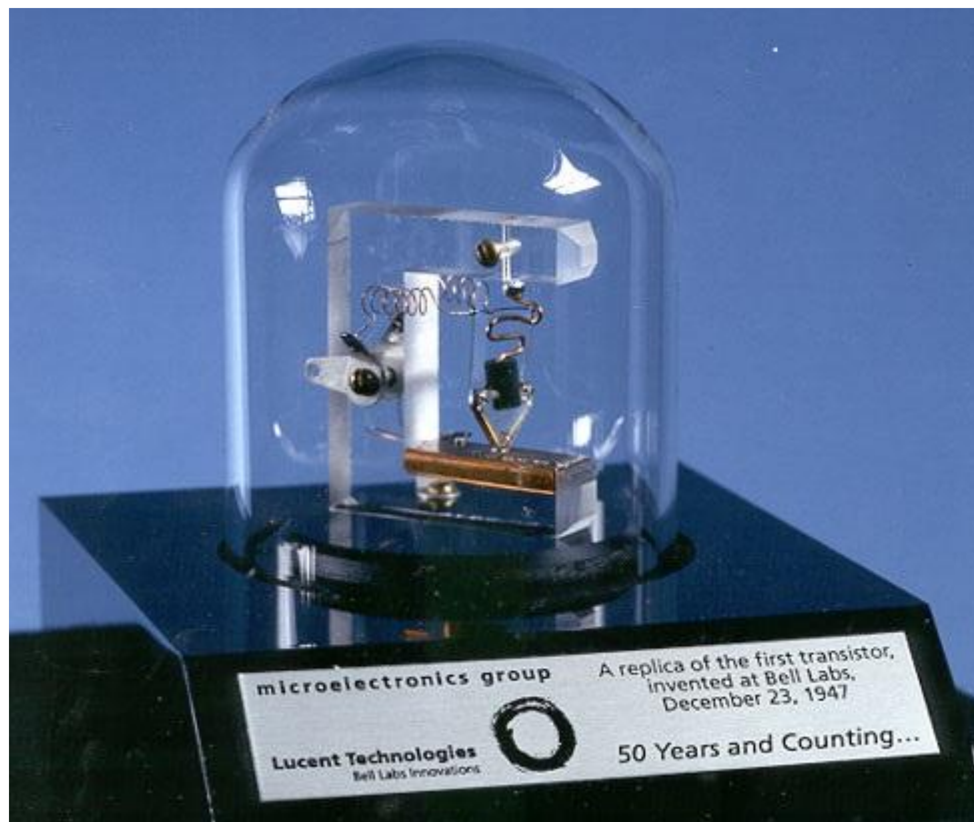

Fig: 1.1: First ever transistor

1.2 Bipolar Junction Transistor (BJT)

A bipolar junction transistor (bipolar transistor or BJT) is a type of transistor that uses both electron and holecharge carriers. For their operation, BJTs use two junctions between two semiconductor types, n-type and p-type. BJTs are manufactured in two types, NPN and PNP NPN based on the doping types of the three main terminal regions, and are available as individual components, or fabricated in integrated circuits, often in large numbers. An NPN transistor comprises two semiconductor junctions that share a thin p doped anode region, and a PNP transistor comprises two semiconductor junctions that share a thin n-doped cathode region. The basic function of a BJT is to amplify current. This allows BJTs to be used as amplifiers or switches, giving them wide applicability in electronic equipment.BJT consist of three differently doped semiconductor regions: the emitter region, the base region and the collector region. These regions are, respectively, p type, n type and p-type in a PNP transistor, and n type, p type and n type in an NPN transistor. Each semiconductor region is connected to a terminal, appropriately labeled: emitter (E), base(B) and collector (C).The emitter is heavily doped i.e number of electrons is very high and the base is lightly doped. The collector is normally doped. The emitter emits electrons into the base in case of npn BJT and holes in case of pnp BJT. The collector collects electron and holes emitted by the emitter and the base controls the flow of electrons and holes from the emitter and collector.

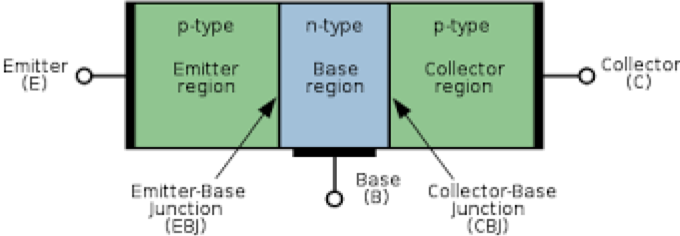

Fig:1.2:pnp BJT showing base, emitter and collector

1.3 JUNCTION FIELD EFFECT TRANSISTOR (JFET)

The junction gate field-effect transistor (JFET or JUGFET) is the simplest type of field-effect transistor. They are three-terminal semiconductor devices that can be used as electronically-controlled switches, amplifiers, or voltage-controlled resistors. Unlike bipolar transistors, JFETs are exclusively voltage-controlled in that they do not need a biasing current. Electric charge flows through a semiconducting channel between source and drain terminals. A JFET is usually on when there is no potential difference between its gate and source terminals. If a potential difference of the proper polarity is applied between its gate and source terminals, the JFET will be more resistive to current flow, which means less current would flow in the channel between the source and drain terminals. Thus, JFETs are sometimes referred to as depletion-mode devices.JFETs can have an n-type or p-type channel. In the n-type, if the voltage applied to the gate is less than that applied to the source, the current will be reduced. The p-type, JFET occurs when the voltage applied to the gate is greater than that applied to the source.

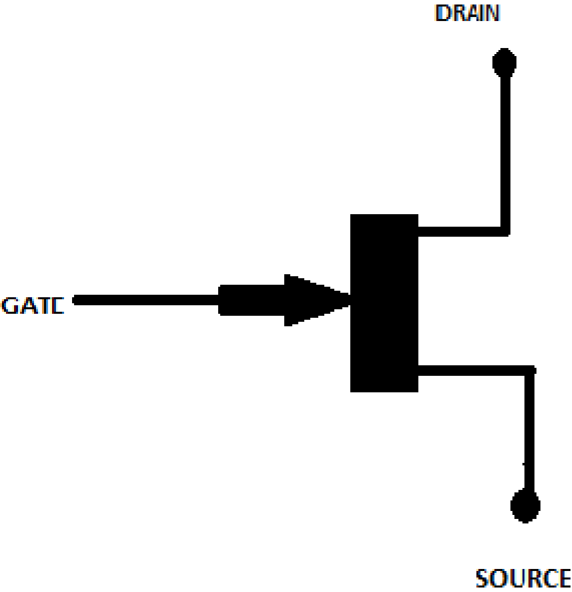

Fig : 1.3.1 : N-type JFET

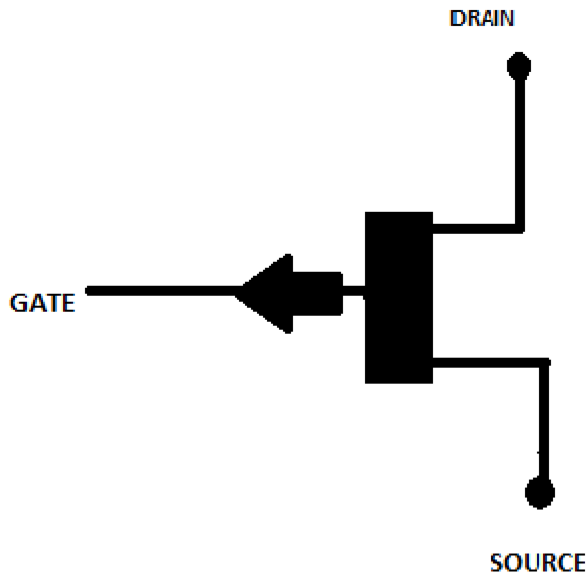

Fig: 1.3.2 : P-type JFET

1.4 METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

The metal–oxide–semiconductor field-effect transistor (MOSFET) is a type of transistor used for amplifying or switching electronic signals. Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals, the body (or substrate) of the MOSFET is often connected to the source terminal, making it a three-terminal device like other field-effect transistors. Because these two terminals are normally connected to each other (short-circuited) internally, only three terminals appear in electrical diagrams. The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common. The traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO_2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon (the latter is commonly used). As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor. When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. Considering a NMOS, if

both source and gate is grounded and drain is provided with a positive voltage, no current will flow through because electron cannot pass the two P-N-P junctions. For current to flow there should exist a channel of electrons between source and drain for the MOSFET to turn it on. In order for the channel to be created, the gate should be given a positive voltage and negative charges will accumulate beneath the Si02 layer. For current to flow, both gate and drain must be provided with a positive voltage. No current flows through the gate due to the silicon dioxide insulator. For the channel to be formed between drain and source, there must exists a minimum gate to source voltage which is known as threshold voltage. Below threshold voltage the MOSFET will remain off. When the voltage between transistor gate and source (Vgs) exceeds the threshold voltage (Vt), it is known as overdrive voltage. A metal–oxide–semiconductor field-effect transistor (MOSFET) is based on the modulation of charge concentration by a MOS capacitance between a body electrode and a gate electrode located above the body and insulated from all other device regions by a gate dielectric layer which in the case of a MOSFET is an oxide, such as silicon dioxide. If dielectrics other than an oxide such as silicon dioxide (often referred to as oxide) are employed the device may be referred to as a metal–insulator–semiconductor FET (MISFET). Compared to the MOS capacitor, the MOSFET includes two additional terminals (source and drain), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type, but they must both be of the same type, and of opposite type to the body region. If the MOSFET is an n-channel or NMOS, then the source and drain are "n+" regions and the body is a "p" region. If the MOSFET is a p-channel or PMOS, then the source and drain are "p+" regions and the body is a "n" region

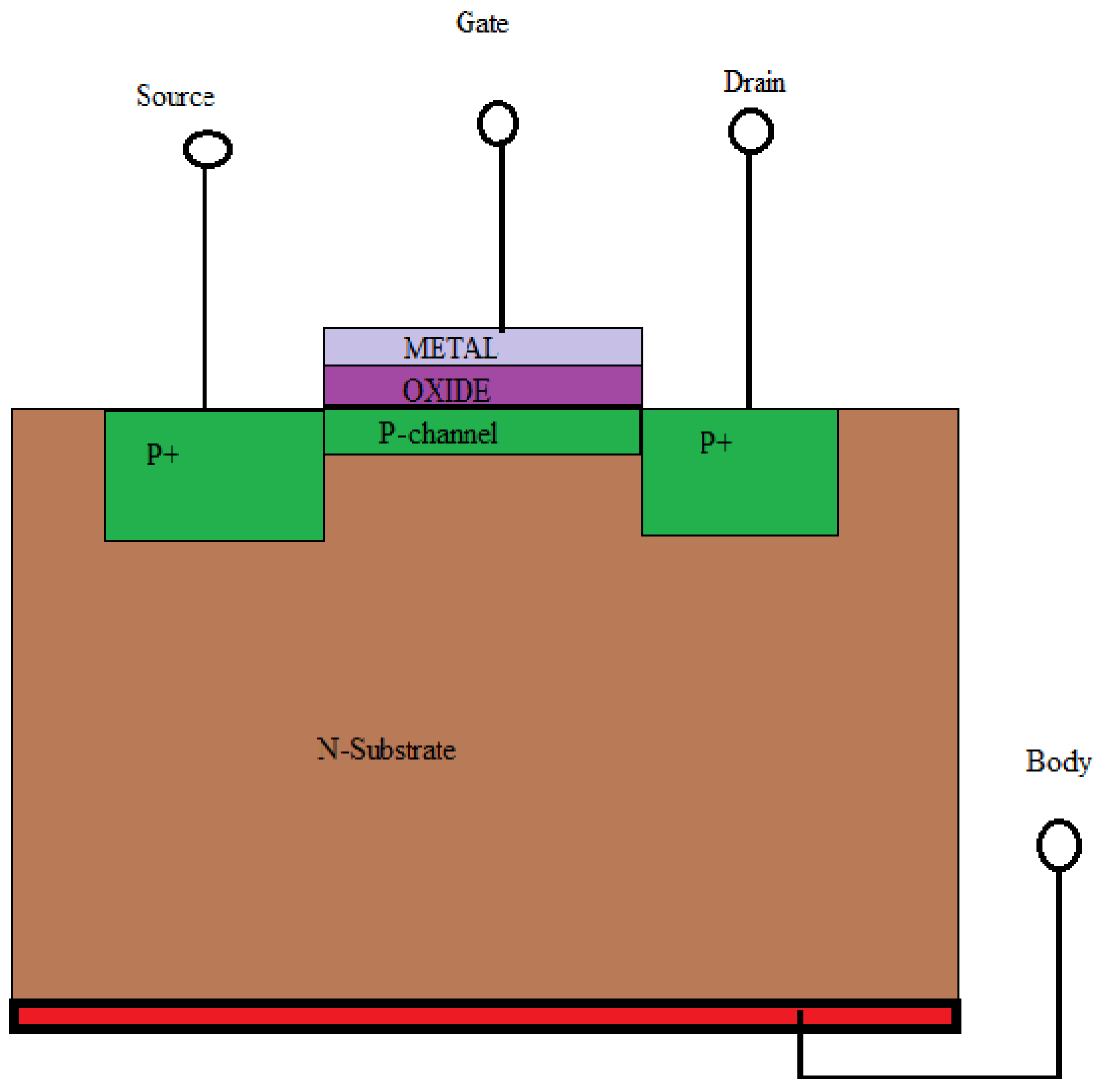

Fig: 1.4.1: A n-typeMOSFET showing Gate, Drain, Source and Body when Vgs>Vt

MOSFETS exists in mainly two forms: N MOSFET and P MOSFET. There exists another cascaded type of MOSFET known as Complimentary MOSFET or CMOS, which is a combination of both N-MOS and P-MOS.

NMOS

NMOS is built with n-type source and drain and a p-type substrate. In a NMOS, electrons are the carriers. When a high voltage is applied to the gate, NMOS will conduct and will not conduct when a low voltage is applied at the gate. This is why N-MOS is said to give good zeros. NMOS are usually much smaller than PMOS and provide half the impedance than that of PMOS. NMOS are considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as holes.

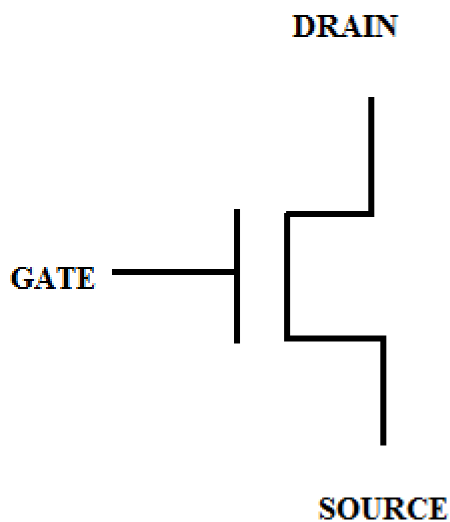

Fig: 1.4.2: NMOS Transistor

PMOS

PMOS is built with p-type source and drain and an n-type substrate and the carriers are holes. When a low voltage is applied in the gate, PMOS will conduct, exactly opposite to that of NMOS. PMOS devices are more immune to noise than NMOS devices.

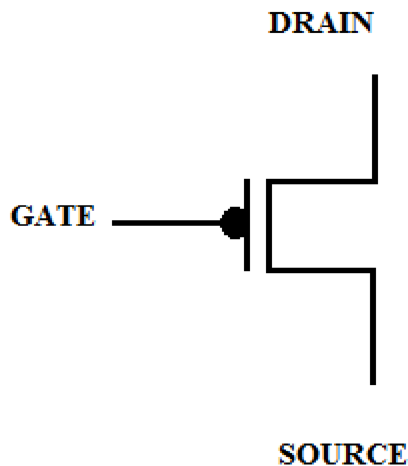

Fig: 1.4.3: PMOS Transistor

1.5 HIGH ELECTRON MOBILITY TRANSISTOR (HEMT)

A High-electron-mobility transistor (HEMT), also known as hetero structure FET (HFET) is a field-effect transistor incorporating a junction between two materials with different band gaps (i.e. a hetero junction) as the channel instead of a doped region. Ideally, the two different materials used for a hetero-junction would have the same lattice constant (spacing between the atoms).A commonly used material combination is GaAs with AlGaAs, though there is wide variation, dependent on the application of the device. Devices incorporating more indium generally show better high-frequency performance. In HEMT, a high band gap material (AlGaAS) is joined with a lower band gap material (GaAs). Since the two doped materials have different band gaps, there exists a junction where electron gets trapped. When a hetero-junction is formed, the conduction band and valence bandthroughout the material must bend in order to form a continuous level. Thus the electron tends to diffuse from higher band gap material towards the lower band gap material through the continuous level junction. This diffusion of carriers leads to the accumulation of electrons along the boundary of the two regions inside the

lower band gap material. The accumulation of electrons leads to a very high current in these devices. The accumulated electrons are also known as 2DEG or two-dimensional electron gas. HEMT usually has two distinct forms: pHEMT and mHEMT. In pHEMT, an extremely thin layer of one of the materials is used so that the crystal lattice simply stretches to fit the other material. By this a hetero-junction is created for the diffusion of electrons among the different band gaps materials. In mHEMT a buffer layer between the two different lattice constant materials. The buffer layer is made of InAlAs, with the indium concentration graded so that it can match the lattice constant of both the GaAs substrate and the AlGaAschannel.

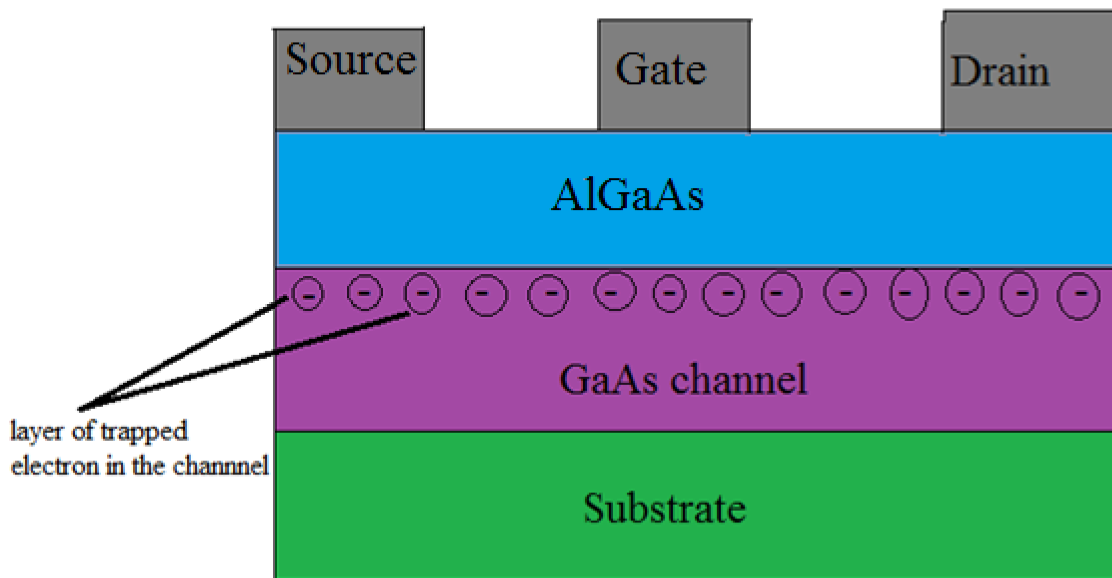

Fig: 1.5.1: A GaAs HEMT

1.6 QUANTUM WELL FIELD EFFECT TRANSISTOR (QWFET)

Quantum well FET are formed in semiconductors by having a material of lower band gap like GaAs, sandwiched between two layers of a material with a higher band gap, like InAlAs. Unlike HEMT, where there exists a single hetero-junction between two different band gap materials, in QWFET, due to the presence of a sandwiched material, there exist two hetero-junctions as hence it is referred to as bi-hetero-junction. The sandwiched material is chosen in such a way that the width of the material is very much smaller (in micro range) than the materials surrounding it, so that maximum number of electrons can reside inside the sandwiched material. If more number of electrons can accumulate within sandwiched material, then electron concentration will increase and hence there will be more discrete energy levels of the electrons. If more discrete number of energy levels exists, then the electron probability function will be more accurate.

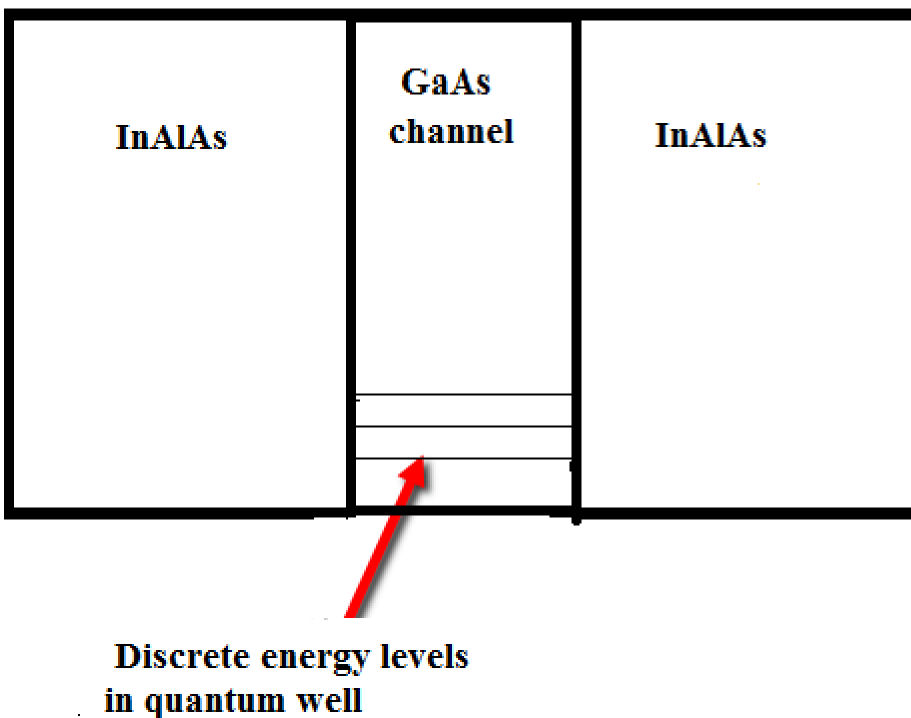

Fig: 1.6.1: Diagram showing quantum well in quantum well FET

2 SCHRODINGER EQUATION

The Schrödinger equation is the fundamental equation of physics for describing quantum mechanical behavior. It is also often called the Schrödinger wave equation, and is a partial differential equation that describes how the wave function of a physical system evolves over time. The general form of Schrödinger equation is as follows:

$$E\psi = H\psi$$

Where, H = Hamiltonian operator

ψ = electron probability density

E = total energy.

To apply the Schrödinger equation, the Hamiltonian operator is set up for the system, accounting for the kinetic and potential energy of the particles constituting the system, then inserted into the Schrödinger equation. The resulting partial differential equation is solved for the wave function, which contains information about the system. The effective mass Hamiltonian simple relation is

$H(k) = Ec + \hbar^2 k^2/2mc$

Where, Ec = potential energy

K = wave number

$\hbar^2$(h cut) = Planck constant/2π

Hence putting the value of Hamiltonian operator in the general Schrodinger equation we get the Schrodinger equation for a single non-relativistic particle.

$$E\psi(s) = -\frac{\hbar^2}{2m}\nabla^2\psi(s) + V(s)\psi(s)$$

m= Effective mass of an electron

∇^2 = Laplacian operator

$V(s)$= Potential energy

Schrodinger wave equation is mainly used to determine the probability density function for a nano-scale device. In a bulk material where the number of atoms is in huge quantities. More atoms means more number of electrons which leads to more number of overlapping of electron orbitals among themselves when the electrons come close to each other overcoming coulombs electrostatic force of repulsion. As a result there will be more band splitting of electron orbitals and hence the energy profile tends to become continuous. This procedure can be explained using classical mechanics. But in case when the materials tends to be in the nanometer range as for example in quantum well, there exists discrete energy levels. So this scenario cannot predict accurately to find the electron probability density function. In this case we use the Schrodinger wave equation to predict the electron density probability functions at different energy levels at different points. Then integrating the total surface over different energy states, we get the total electron probability density function.

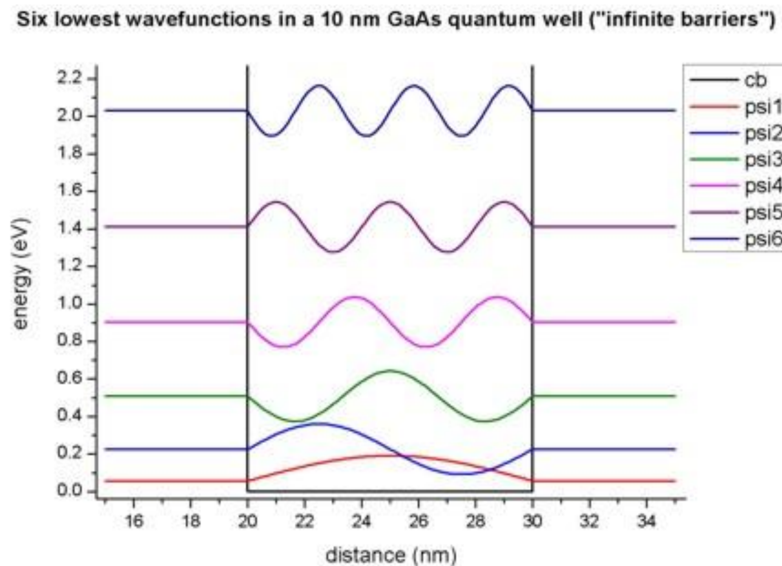

Fig:2: Diagram showing discrete energy states in a GaAs quantum well FET

3 POISSON'S EQUATION

The Poisson's equation is normally used to determine the electric potential of a material when a specific charge density is applied to it. The general Poisson's wave equation is

$$\nabla^2\phi = -(\rho / \varepsilon)$$

where ρ = charge density
ε = absolute permittivity of the material
ϕ = electric potential

The charge density obtained from the Poisson's equation is then exported into the Schrodinger equation to find the electron probability density function.

4 THEORITICAL MODELLING OF QWFET STRUCTURE

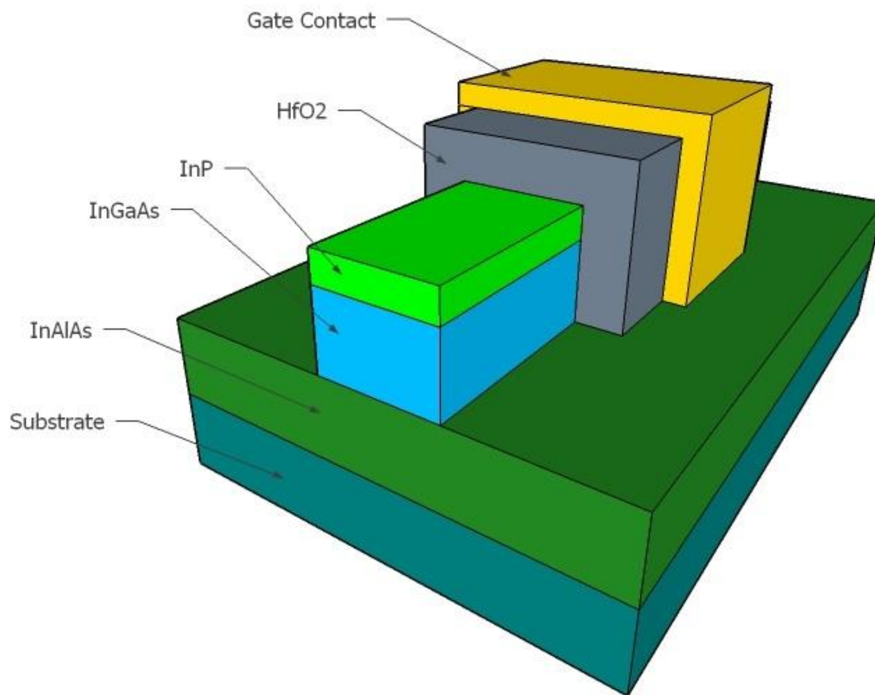

Fig: 4.1: 3-D cross section of QWFET device

The above figure shows the 3D cross sectional model of InGaAs QWFET. The substrate used is usually silicon and the bottom barrier is made of InAlAs. The gate surrounds the device on all the sides except the bottom followed by the oxide layer consisting of HfO_2. Here HfO_2 (hafnium oxide) is used ahead of silicon dioxide which is mainly used as the oxide layer in most

cases.Thereason behind choosing HfO_2 over SiO_2 is because hafnium oxide has a very high dielectric constant (ϵ_r) than that of SiO_2 (25 which is almost 6 times than SiO_2).

Usually the oxide layer is used to avoid the formation of a Schottky barrier between the metal gate and the semiconductor layer. The lower InAlAs barrier ensures that the charges accumulated when the device is switched on is trapped in the channel only and does not move to other regions.InAlAs and InGaAs are chosen as the materials because they have very close lattice constants. If lattice constant varies very much, then lattice mismatch will occur and hence electron scattering will take place. As a result it would cause the presence lattice defects and introduce trap charges in the channel.

5 ALGORITHM

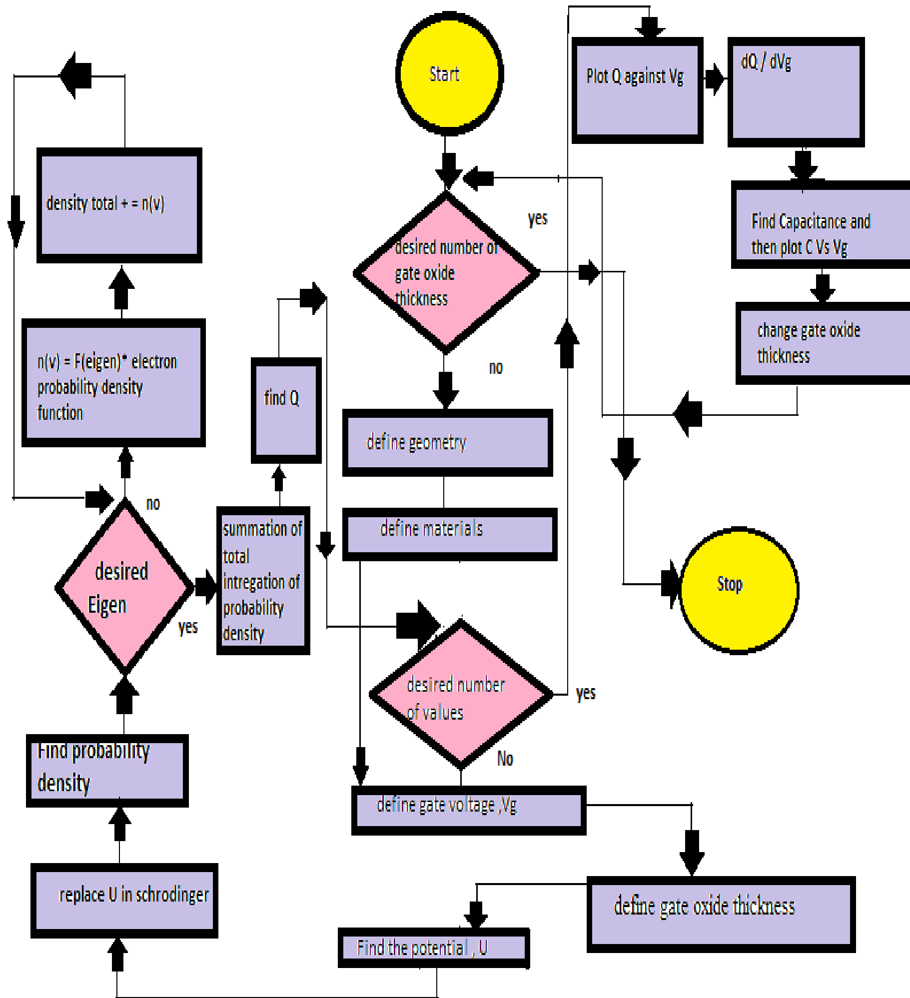

Fig: 5.1: Flowchart showing the procedure of changing gate oxide thickness

Starting with the algorithm, at first we will decidethe desired number of times we will alter the gate oxide thickness to find the C-V characteristics of the QWFET.After deciding the number of times we will alter the gate oxide thickness, we will then turn to define the geometry in COMSOL Multiphysics simulator. Defining the geometry includes setting up all the necessary parameters at each geometry domain for specific materials for the simulation reasons. We will also define the boundary conditions, for example gate voltage, oxide thickness, insulation etc. We will specify a certain gate voltage which will be applied on the material. By taking a specific gate oxide thickness, we will apply Poisson's wave equation to find the electric potential for a certain charge density, as provided in the parameter. Then we will incorporate the electric potential value in the Schrodinger wave equation to find the electron probability density function. After doing so, we will try to find the electron density at each discrete energy state. Then integrating the electron density over the entire surface, we will get the total charge accumulated in the edge of the QWFET barrier surface. Then we will see whether we got sufficient amount of charge accumulated to plot a graph of Charge against gate voltage (Q Vs Vg). If we manage to find them, we will try to get the capacitance values by differentiating the graphs. After calculating the capacitance value, we will plot a graph of capacitance against gate voltage to find the C-V characteristics of the QWFET. Then we will again alter the gate oxide thickness value until desired number of value is reached. If reached we will stop the procedure and simulation process. If not, then we will continue to run the entire procedure until the desired value exceeds.

6 OBTAINING C-V CHARACTERISTICS

Capacitance is the ability of a body to store an electrical charge. A material with a large capacitance holds more electric charge at a given voltage, than one with low capacitance. Any object that can be electrically charged exhibits capacitance.

In order to obtain the C-V characteristics, we first need to find out different capacitance values for certain gate voltages. According the equation $C= Q/V$, we will first find out the total charge accumulated by integrating the electron probability function over the entire surface. After finding the total charge, we will differentiate the total charge with respect to gate voltage. The gradient of the charge Vs Vg graph will give us the capacitance.

Here we are changing the gate oxide thickness as well as the metal work function to obtain the C-V characteristics. The reason behind in changing oxide thickness can be explained from the relationship $C = \varepsilon A/d$, where C is the capacitance and d is the gate oxide thickness. If we decrease the gate oxide thickness, Capacitance will increase which will increase the trapped electrons within the channel. As a result, electron concentration will increase and this in turn will increase the conductance of the materials. Hence using lower gate voltage we can increase the amount of current flowing within the material.

7 HOWCOMSOL SIMULATOR IS USED TO SOLVE DIFFERENT PARAMETERS

7.1 Finite Element Method used in COMSOL Multiphysics

In solving partial differential equation (PDE), COMSOL Multiphysics approximates a solution by using Finite Element Method (FEM), by generating discrete domains in the geometry called mesh. In each domain, COMSOL makes a mathematical model$u$, based on a linear combination of a basis function and given boundary conditions.

$$u_h = \sum_i u_i \Psi_i$$

Where u_h = approximated functionof$u$,

Ψ_i= basis function

u_i = the coefficient of the basis function.

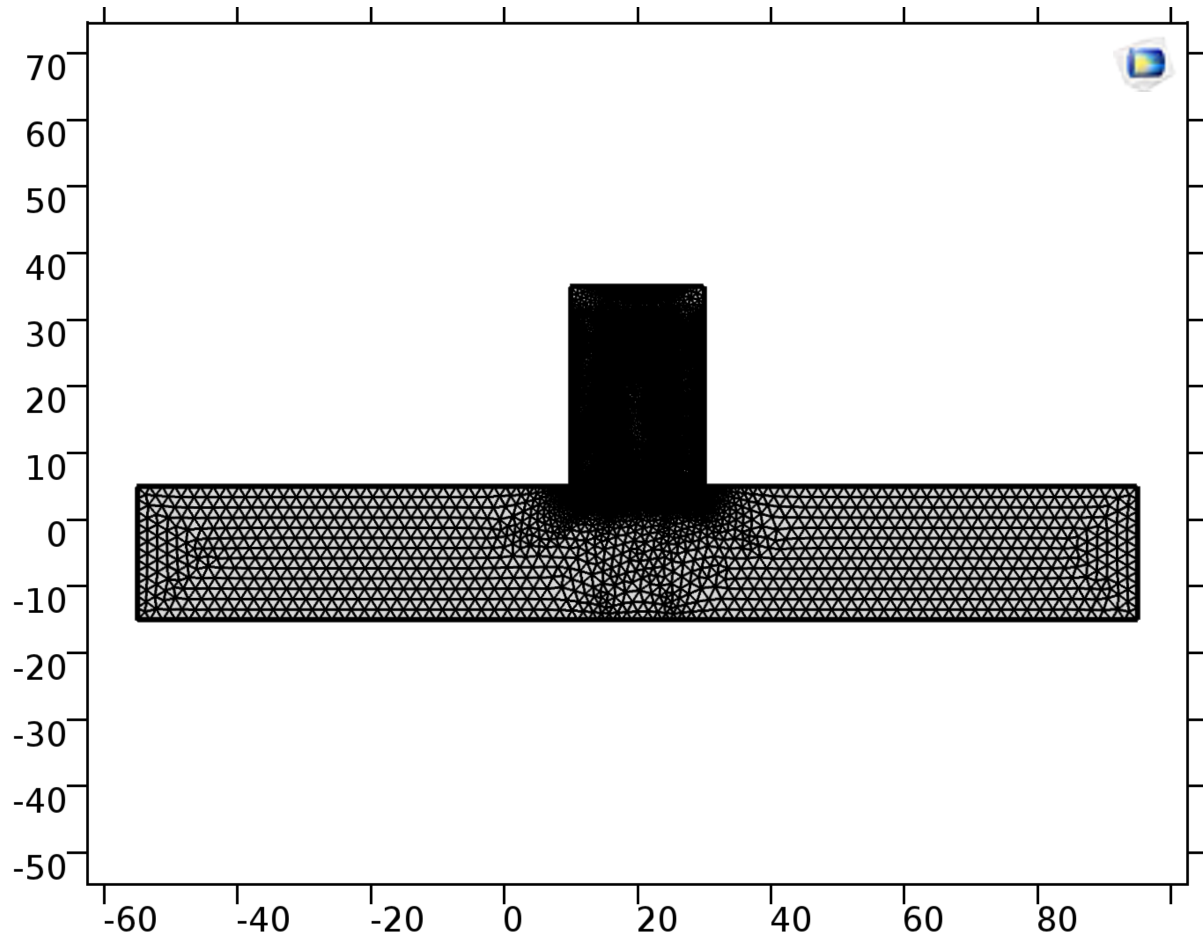

Fig: 7.1.1: Mesh formed in the QWFET 2D structure in COMSOL

COMSOL uses Finite Element Method to solve various equations and studies. In this case, we used built-in Semiconductor Study that analyses the geometry using Mesh Analysis using the given parameters in the given domains made of different materials, and also using different boundary conditions COMSOL establishes a mathematical model on each discrete domain in the mesh by iterative process, until the error reaches a certain tolerance level.

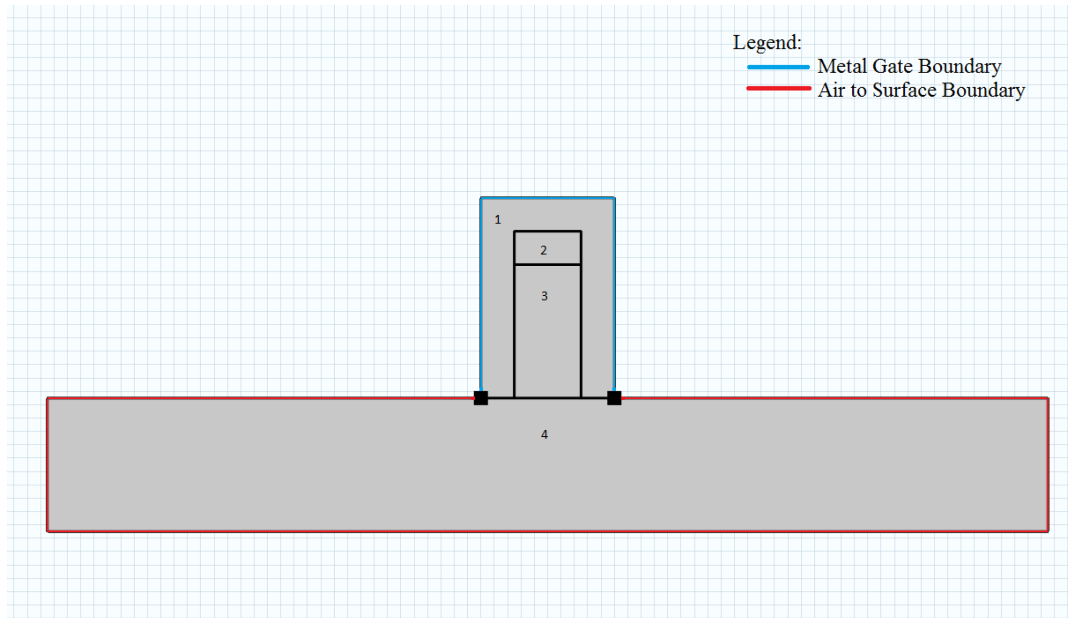

Fig: 7.1.2: Different Domains and Boundaries in the 2D QWFET Structure

In the figure above, domain 1 is the insulator oxide region made of Hafnium Oxide (HfO_2) with high-k dielectric ($\epsilon_r = 25$), domain 2 is the high band gap Indium Phosphide(InP) region, domain 3 is the Indium Gallium Arsenide (InGaAs) channel with lower band gap and domain 4 is the high band gap Indium Aluminum Arsenide (InAlAs) region.

7.2 Semiconductor Module

Apart from myriads of Physics Modules COMSOL provides to study different phenomena, it offers us with a module called Semiconductor Module that computes various parameters such as band profiles, electron concentration using semi-classical model, current components etc. The list of equations used by Semiconductor Module is as follows:

$$\nabla.(-\epsilon_r \nabla V) = (n - p + N_a^+ - N_d^+)$$

$$\nabla.J_n = -qU_n$$

$$\nabla.J_p = qU_p$$

$$J_n = -q_n \mu_n \nabla E_c + \mu_n K_B T G\left(\frac{n}{N_c}\right) \nabla n + qnD_{n,th} \nabla \ln(T)$$

$$J_p = -q_p \mu_p \nabla E_v + \mu_p K_B T G\left(\frac{p}{N_v}\right) \nabla n + qpD_{p,th} \nabla \ln(T)$$

$$E_c = -(V + \chi_0) - \alpha \Delta E_g$$

$$E_v = -\left(V + \chi_0 + E_{g.0}\right) + (1 + \alpha \Delta E_g)$$

These equations were fed with the given parameters of the materials mentioned above in their respective domains, and results such as Ec profile was obtained for the whole QWFET cross-section which was later on incorporated in Schrodinger Physics Module to find probability density distribution at various Eigen states of electrons.

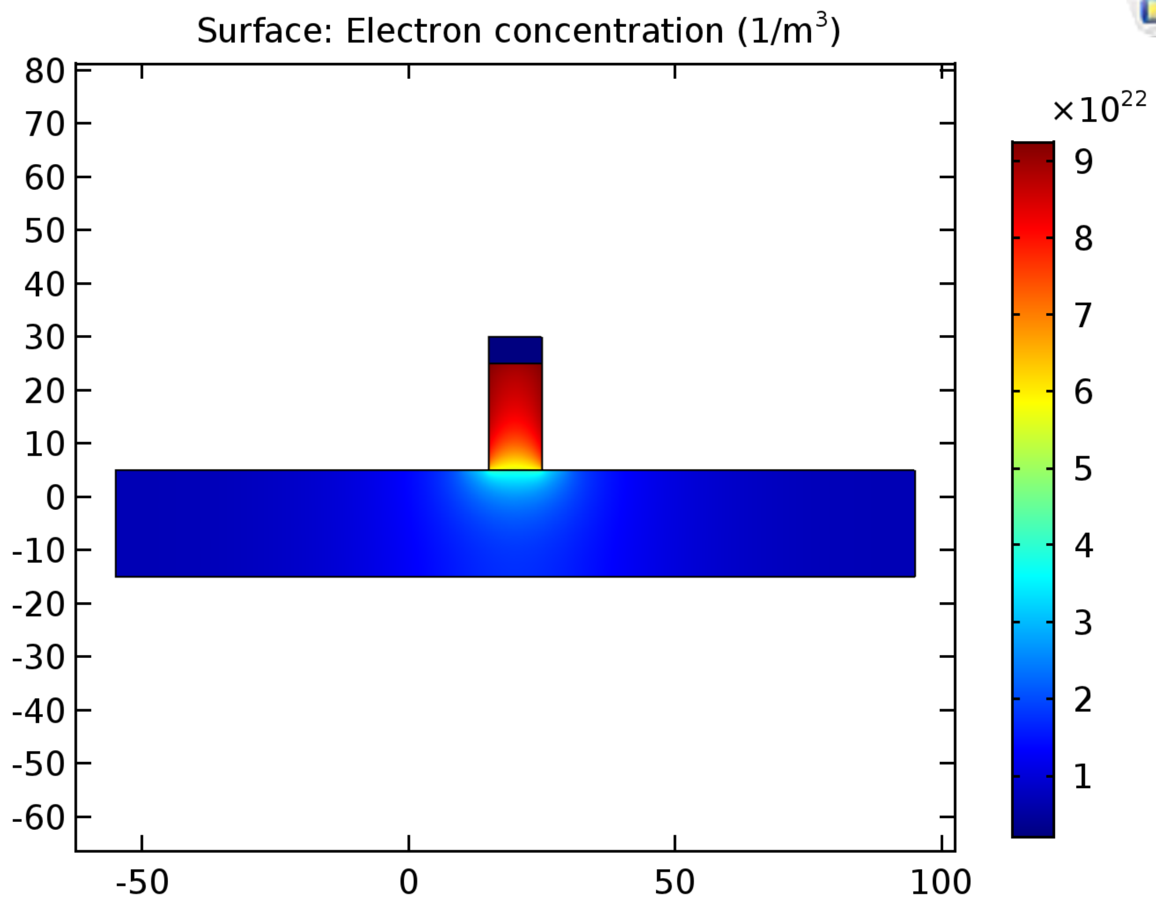

Fig: 7.2.1: Election concentration predicted by classical equation (Semiconductor Module)

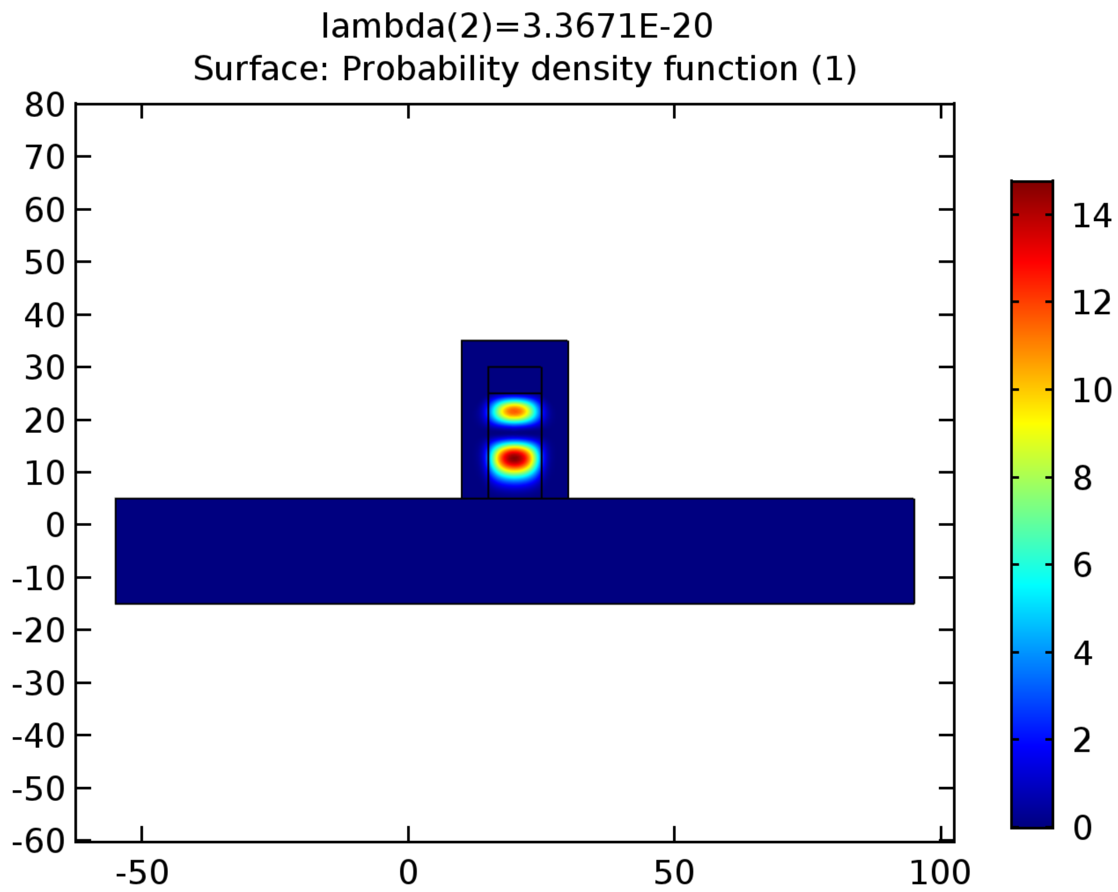

Fig: 7.2.2: Probability density distribution of InGaAs QWFET with gate metal work function 4.7 and Vg=0 at a particular Eigen state.

7.3 Schrodinger Model

As we approach the nano scale region in fabrication process, classical equation fails to predict the actual electron density in the thin channel (around 10nm). As in such, we need to apply Schrodinger model to predict the probability distribution of electrons at different discrete energy states. By summation of the probability distributions of electrons having energy just above the conduction band energy state, we can predict the amount of electrons ready to create a channel

and conduct between source and drain. To find the actual electron density at each Eigenvalue, we need to multiply the probability density with the 'modified' Fermi Level at that Eigenvalue, and sum up the electron density of all Eigenvalues to find the total charge density. The reason underlying the modification of Fermi Level with its application in finding the electron density is as follows.

Using Modified Fermi-Dirac Function to obtain Electron Density

In order to obtain electron density in proper manner, we not only need to sum electron concentration of all the Eigen values above the conduction band (E_c), but we also need to take into account the changing *k*vector in that particular Eigen value. Considering the equation for finding electron density,

$$n(\bar{r}) = \sum_a (|\Psi_a(\bar{r})|^2 f_0(E_a - \mu)$$

WhereE_a is the eigenvalue at a particular energy state, we are not taking into account the change in k space in each eigenvalue. $E_a$can be written as,

$$E_a = E_m + \frac{\hbar^2 k_x^2}{2m_c}$$

Therefore, we can modify the above electron density equation as,

$$n(\bar{r}) = \sum_m \sum_a (|\Psi_m(\bar{r})|^2 f_0(E_a - \mu)$$

In order to accommodate for the changing *k* space in one dimension, we need to modify the Fermi Dirac function in the given form,

$$f_{1D} = \frac{1}{L} \sum_{k_x} f_0(E + \frac{\hbar^2 k_x^2}{2m_c})$$

We can assume that *k* changes continuously over given energy state. So the above equation converts to,

$$f_{1D} = \frac{dk}{2\pi} \int_0^\infty \frac{1}{1 + \exp\left(\frac{E}{k_B T}\right) . \exp\left(\frac{\hbar^2 k_x^2}{2m_c k_B T}\right)}$$

Where$\frac{1}{L} = \frac{dk}{2\pi}$

After some algebraic manipulation, we can finally obtain,

$$f_{1D} = \frac{\sqrt{2m_c k_B T}}{4\pi\hbar} \int_0^\infty \frac{\frac{1}{\sqrt{y}}}{1 + \exp(y + x)} dy$$

Where y=$\frac{\hbar^2 k_x^2}{2m_c k_B T}$ and x=$\frac{E}{k_B T}$

This modified Fermi Dirac Function was coded in MATLAB and multiplied with the Probability Density function obtained from the Schrodinger Model in COMSOL to find the electron density at each Eigen value. The results were added to obtain total electron density of the surface.

8 SIMULATION RESULTS

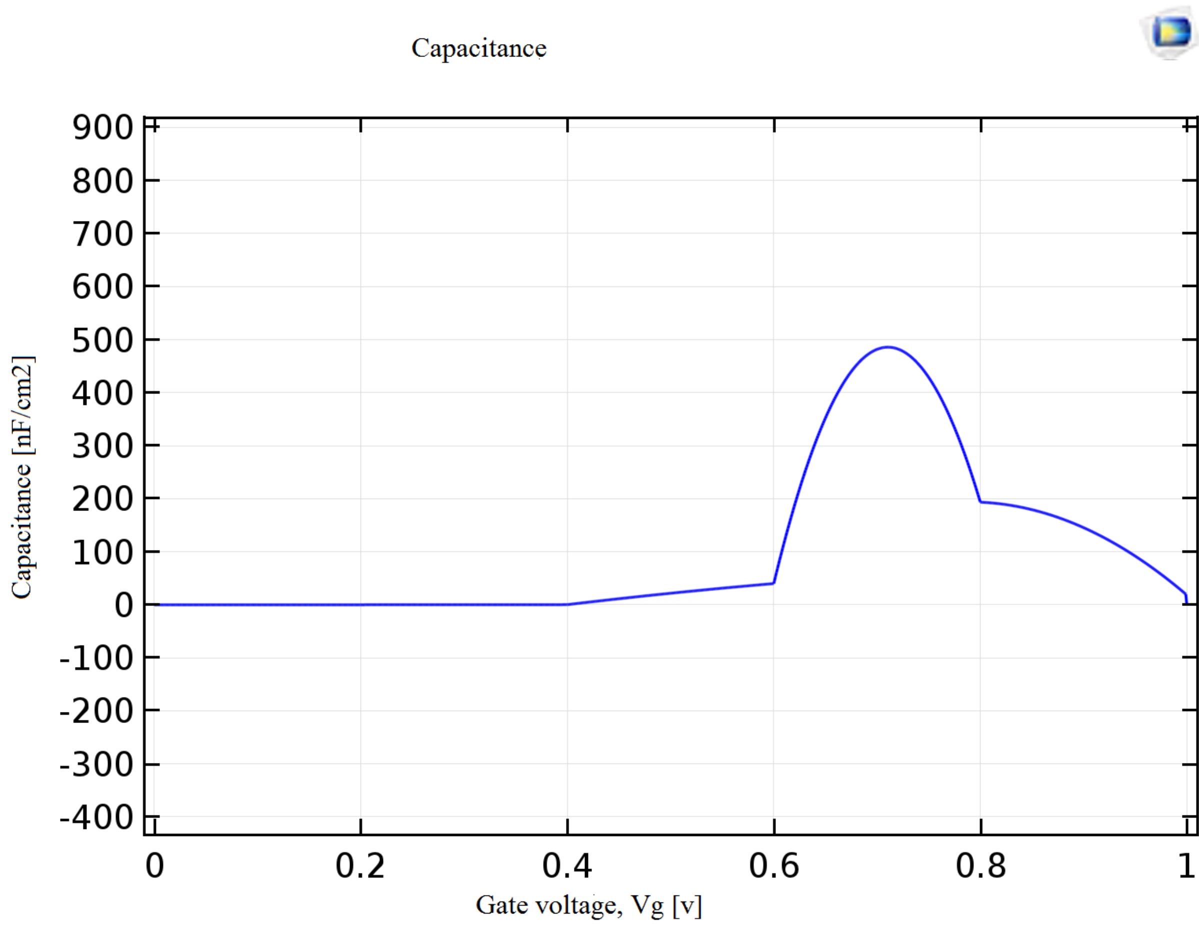

Fig 8.1: C-V characteristics for work function 4.5 and gate thickness 5nm

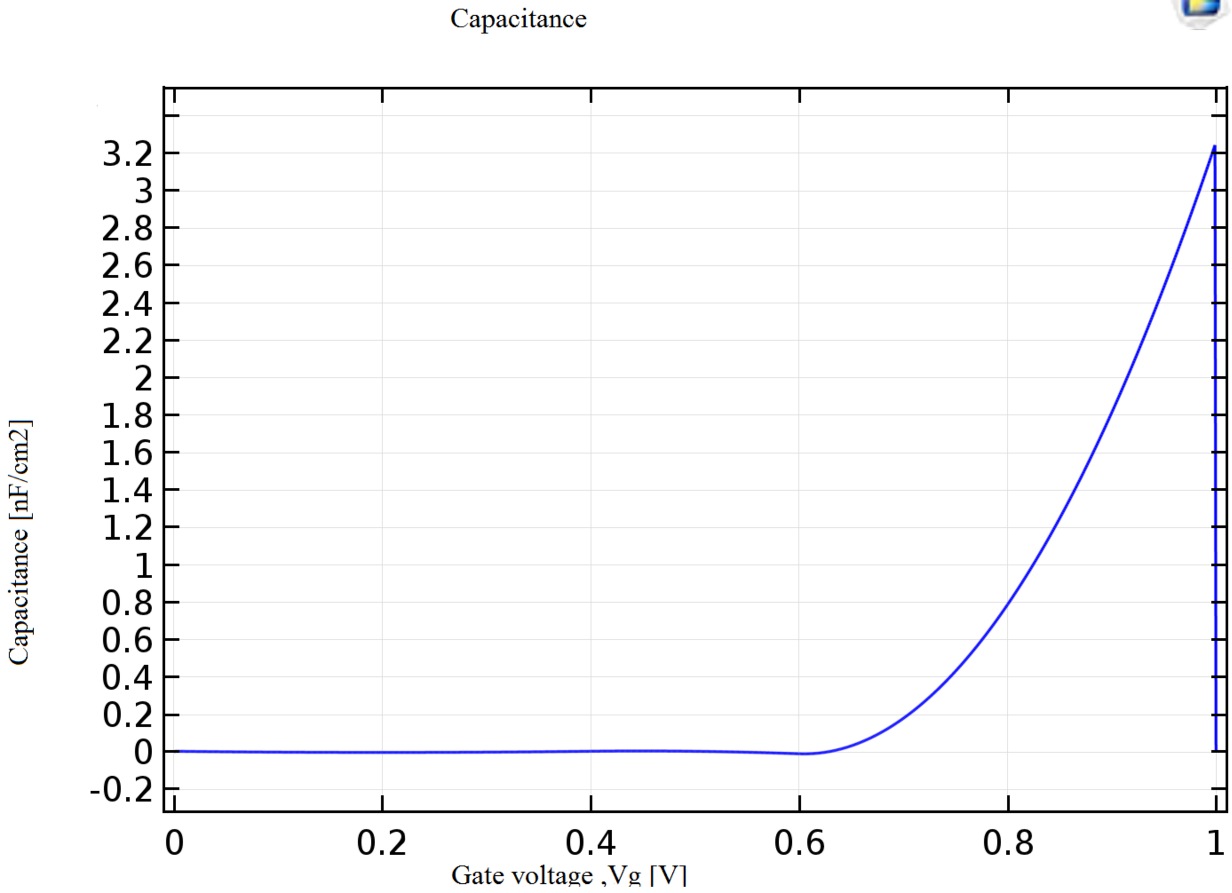

Fig 8.2: C-V characteristics for work function 4.5 and gate thickness 10 nm

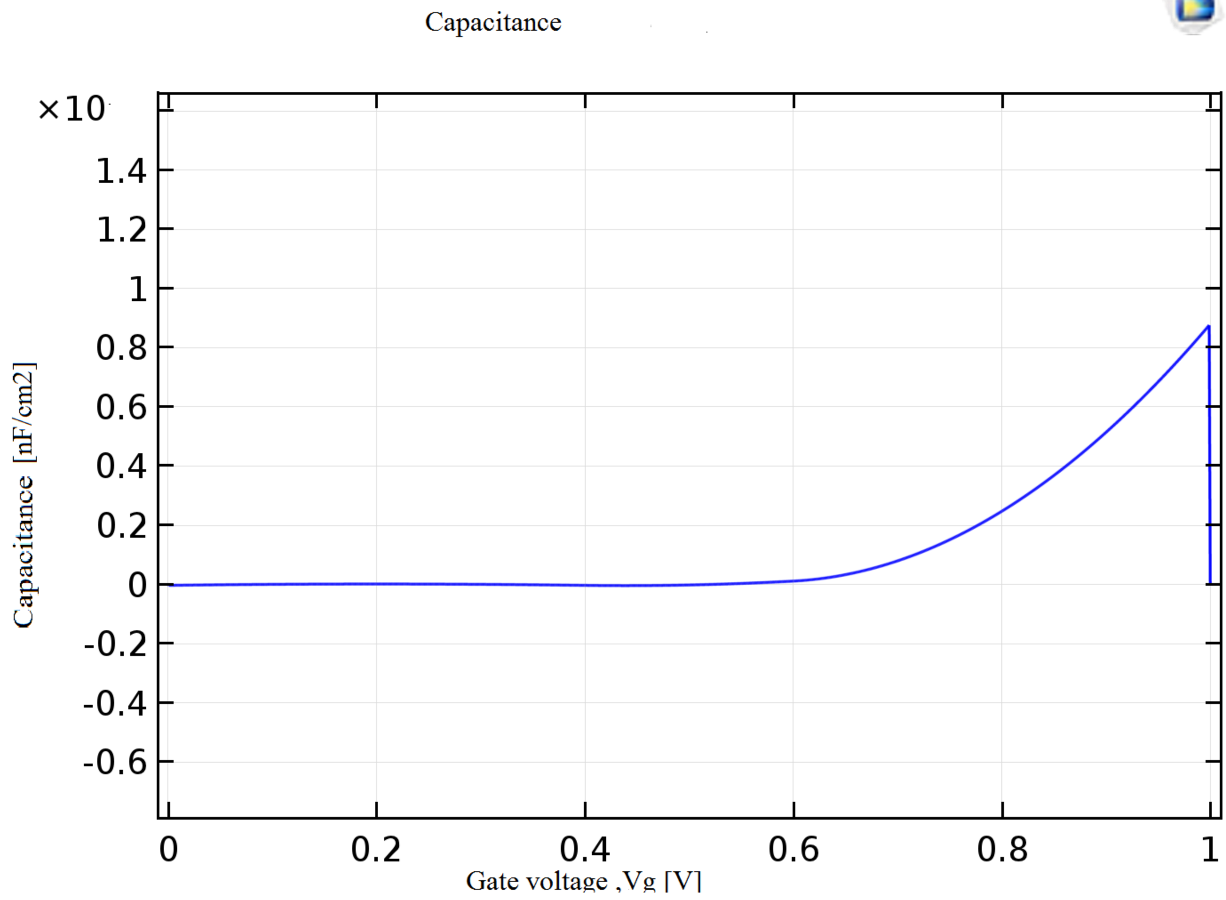

Fig 8.3: C-V characteristics for work function 4.7 and gate thickness 5 nm

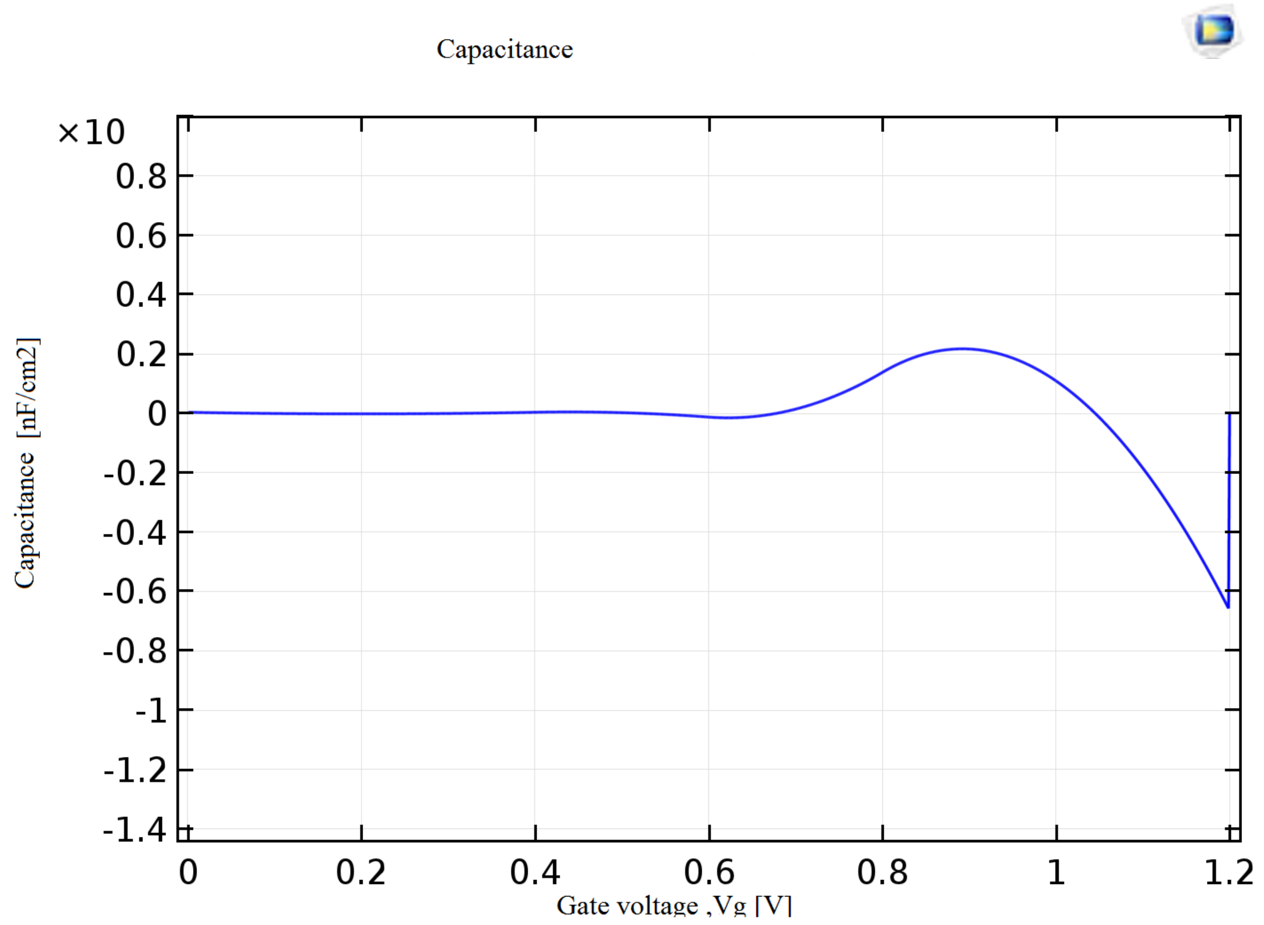

Fig 8.2: C-V characteristics for work function4.7 and gate thickness 10 nm

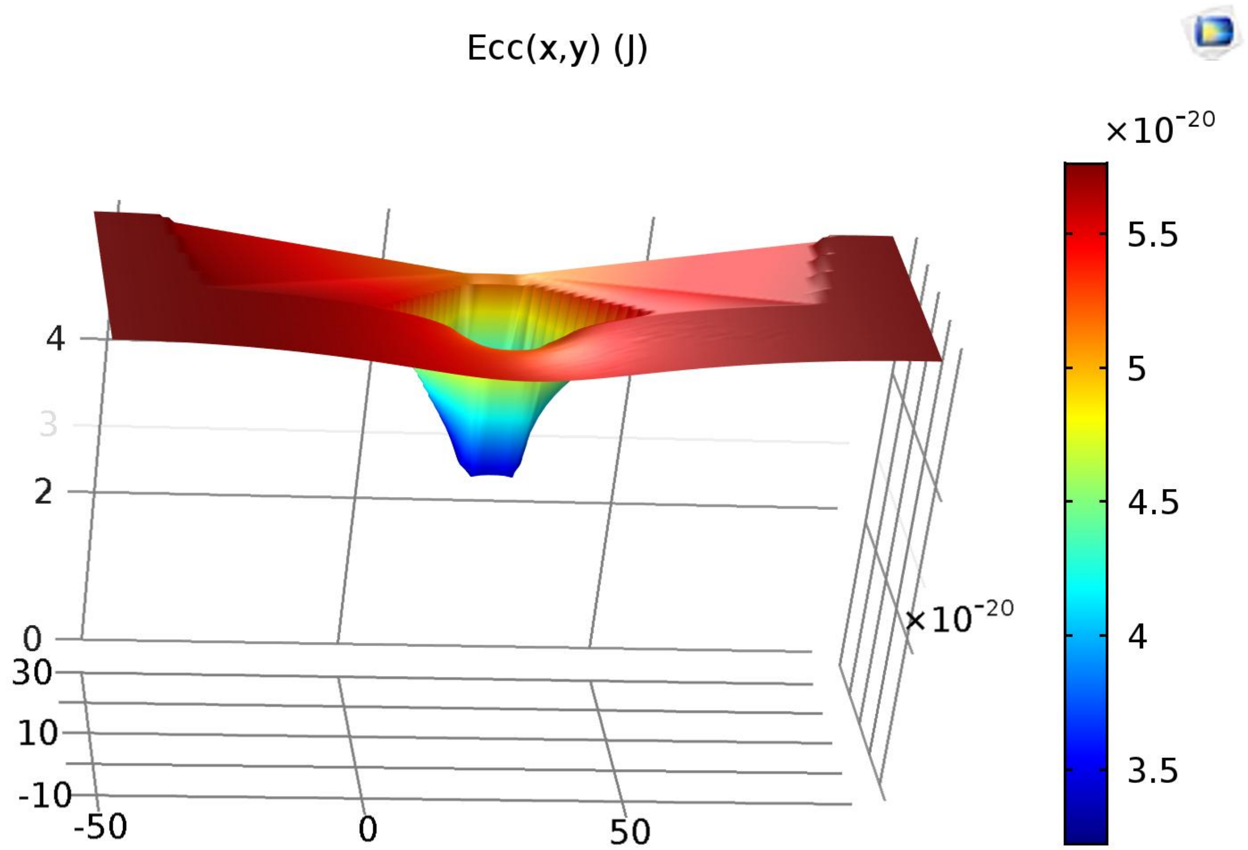

Fig 8.5 Cavity formed at work function 4.5 and oxide thickness 10nm

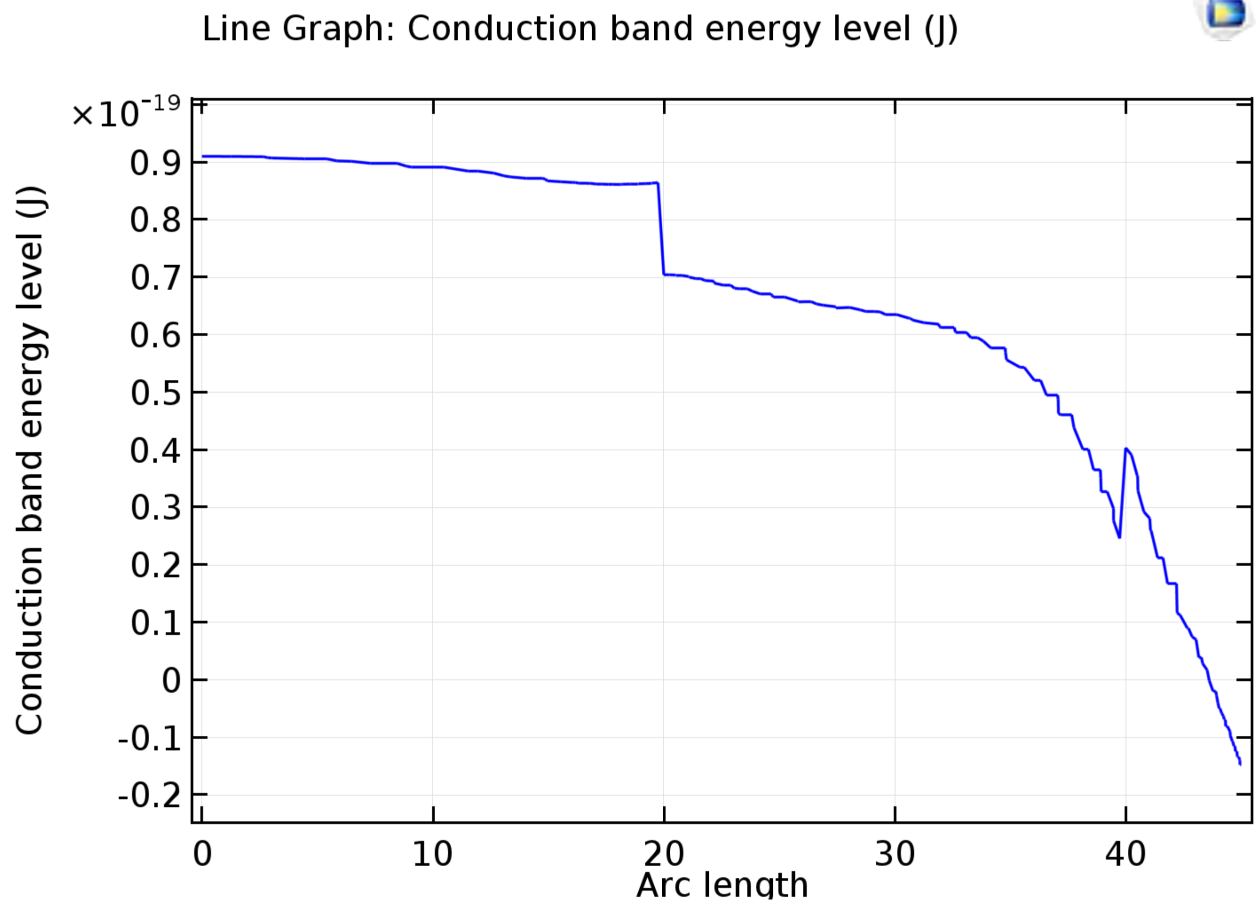

Fig: 8.6: Ec profile at work function 4.7 oxide thickness 5nm and Vg=0

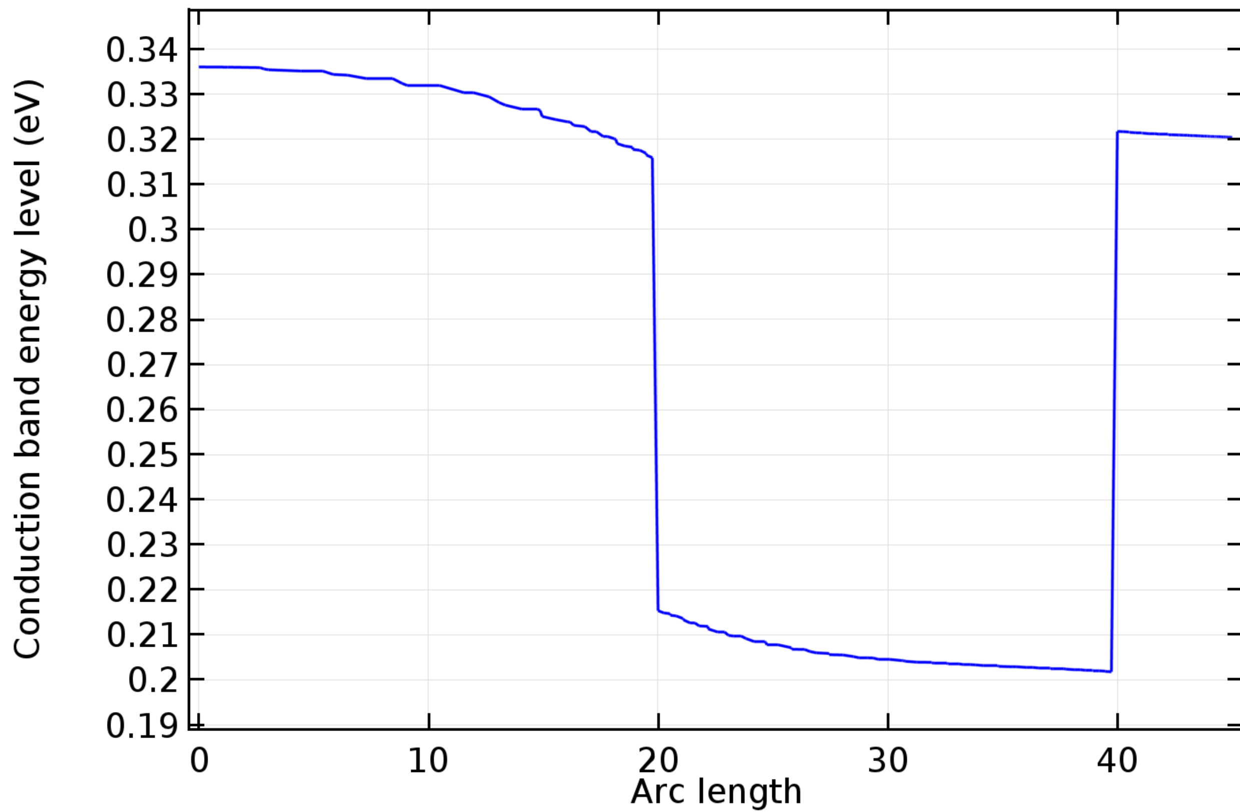

Fig: 8.7: Ec profile at work function 4.7 oxide thickness 5nm and Vg=0.6

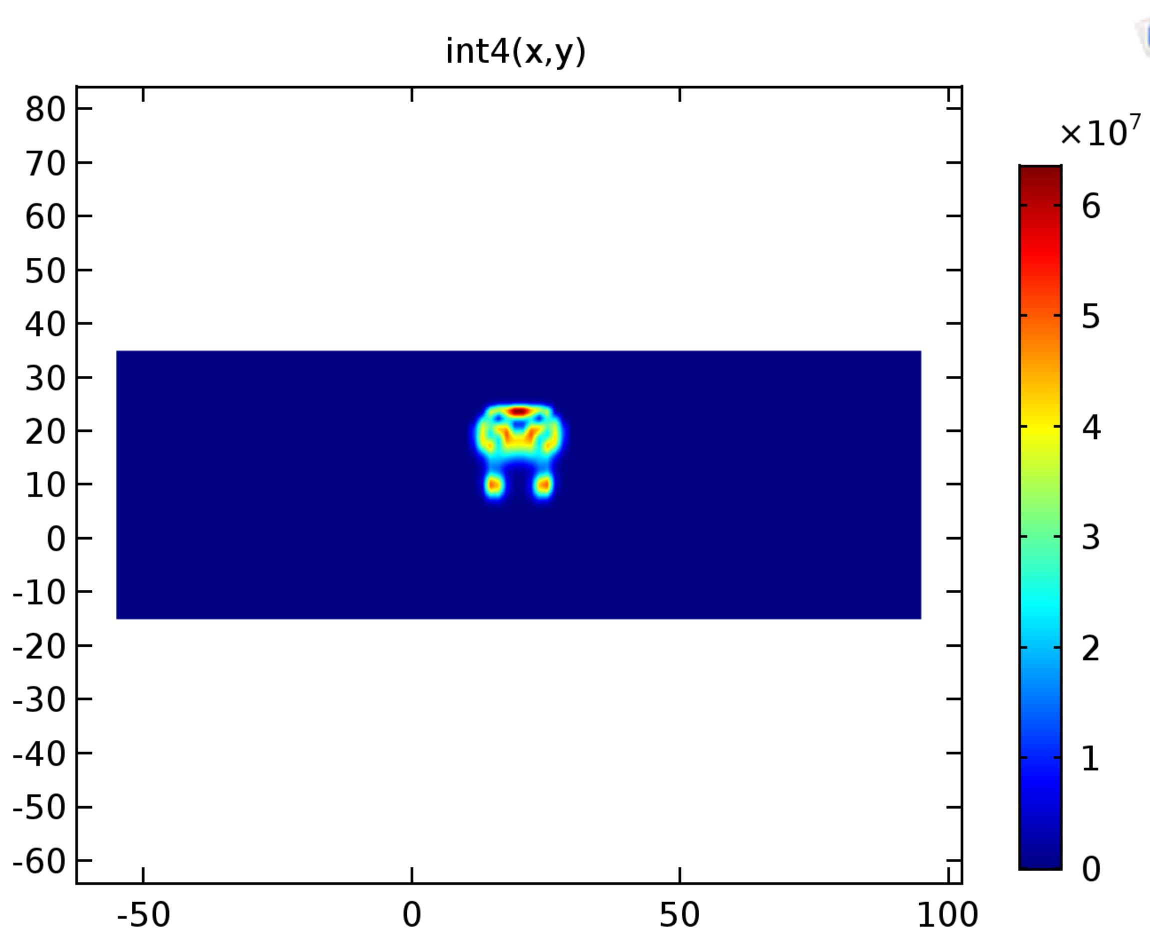

Fig: 8.8 Electron Density predicted by quantum mechanics

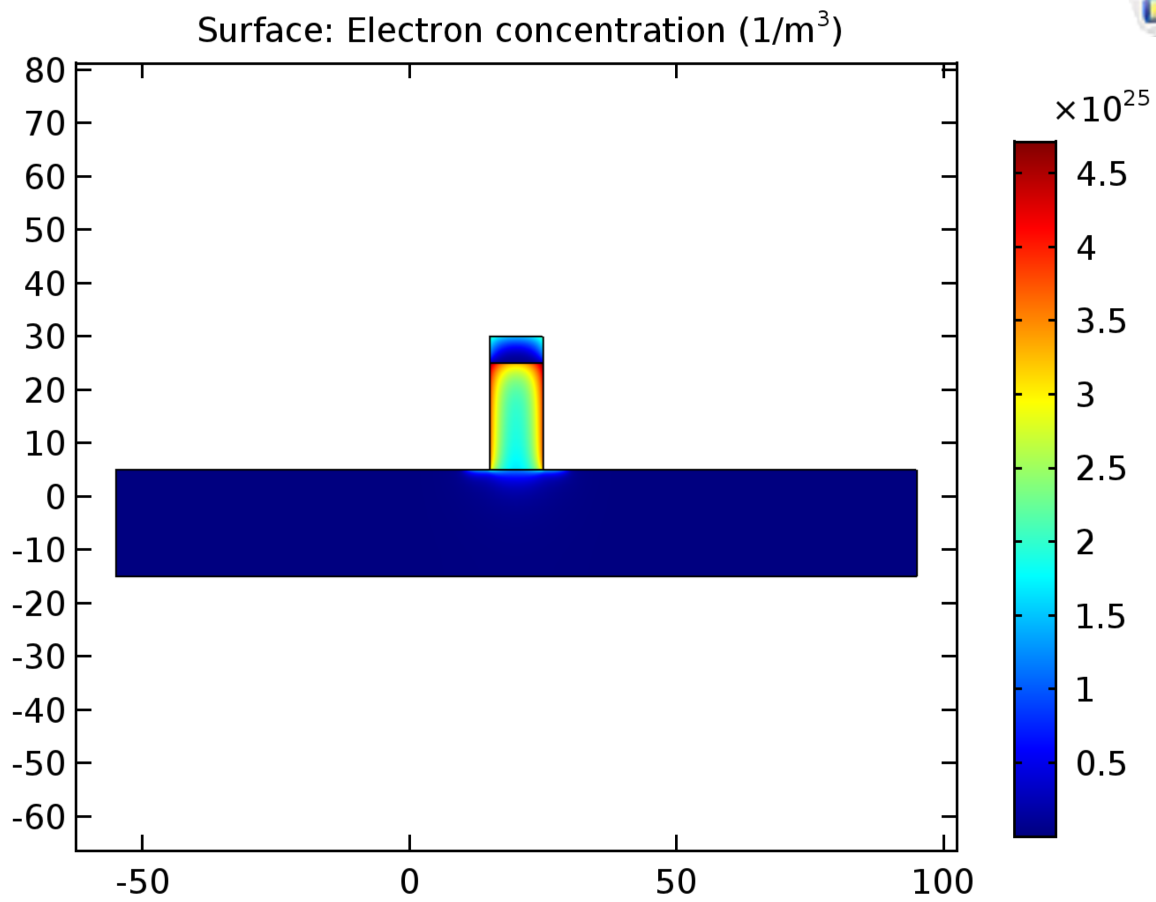

Fig: 8.9 Electron Density predicted by classical mechanics at work function 4.7 oxide thickness 5nm and Vg=0.6 v

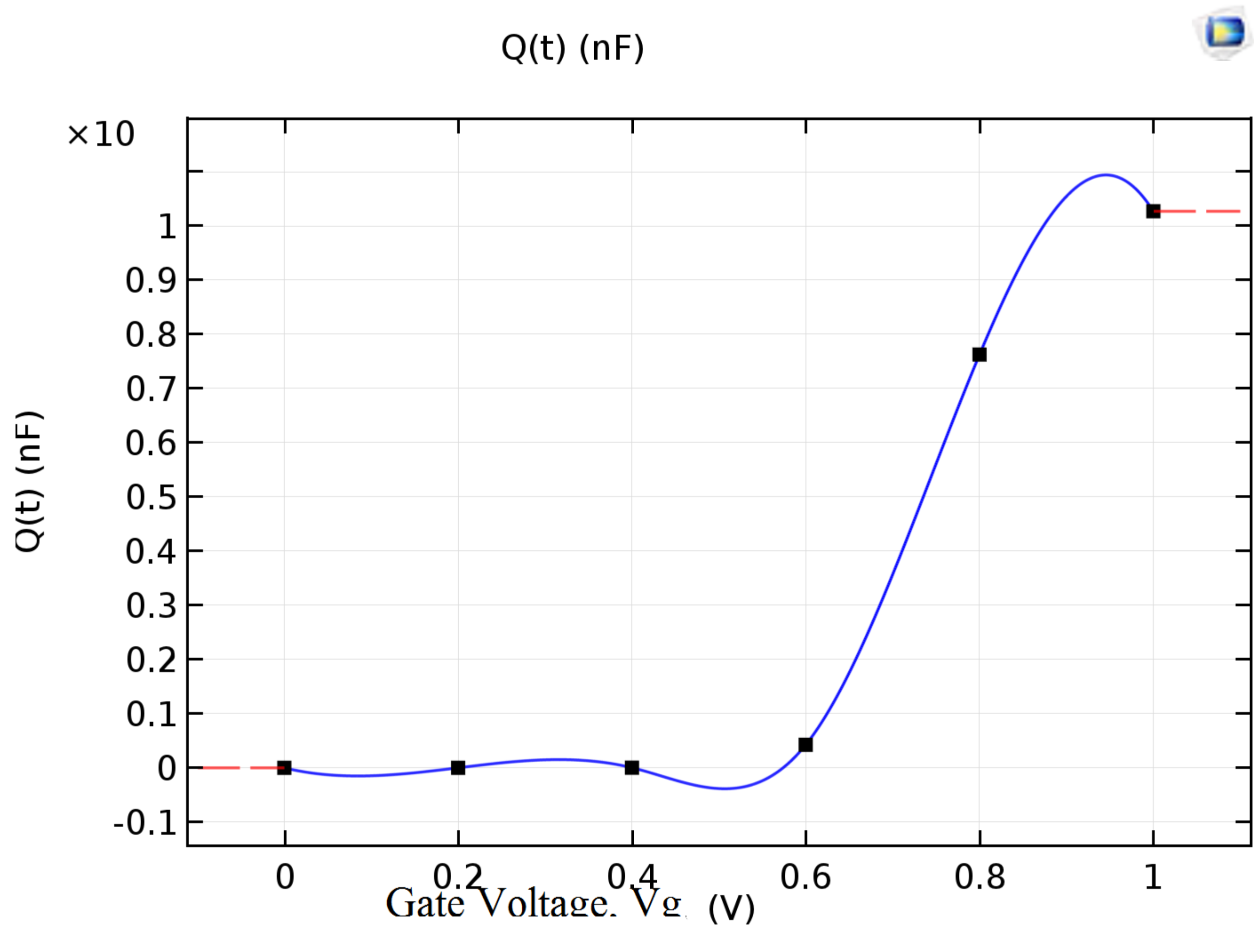

Fig: 8.10 : Q-V characteristics at work function 4.5 and oxide thickness 5nm

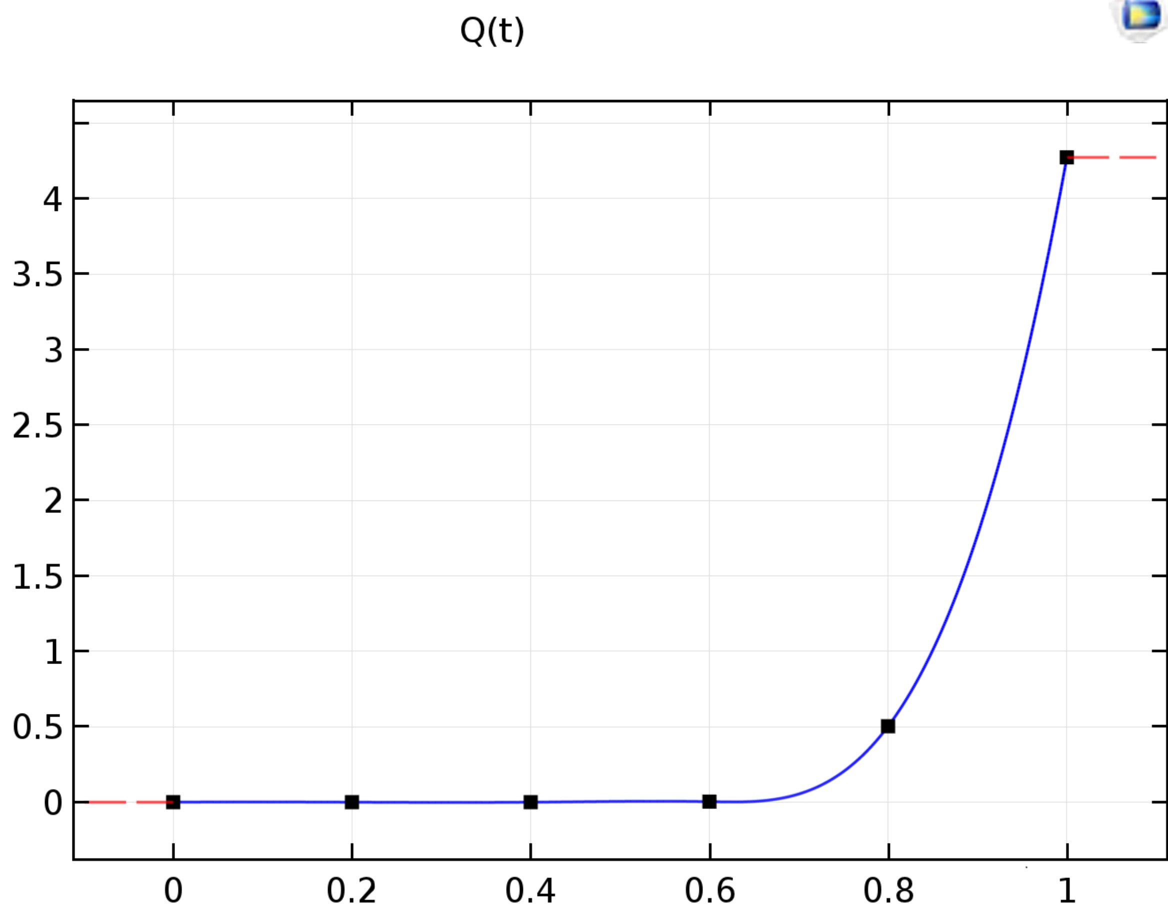

Fig: 8.11: Q-V characteristics at work function 4.5 and oxide thickness 10 nm

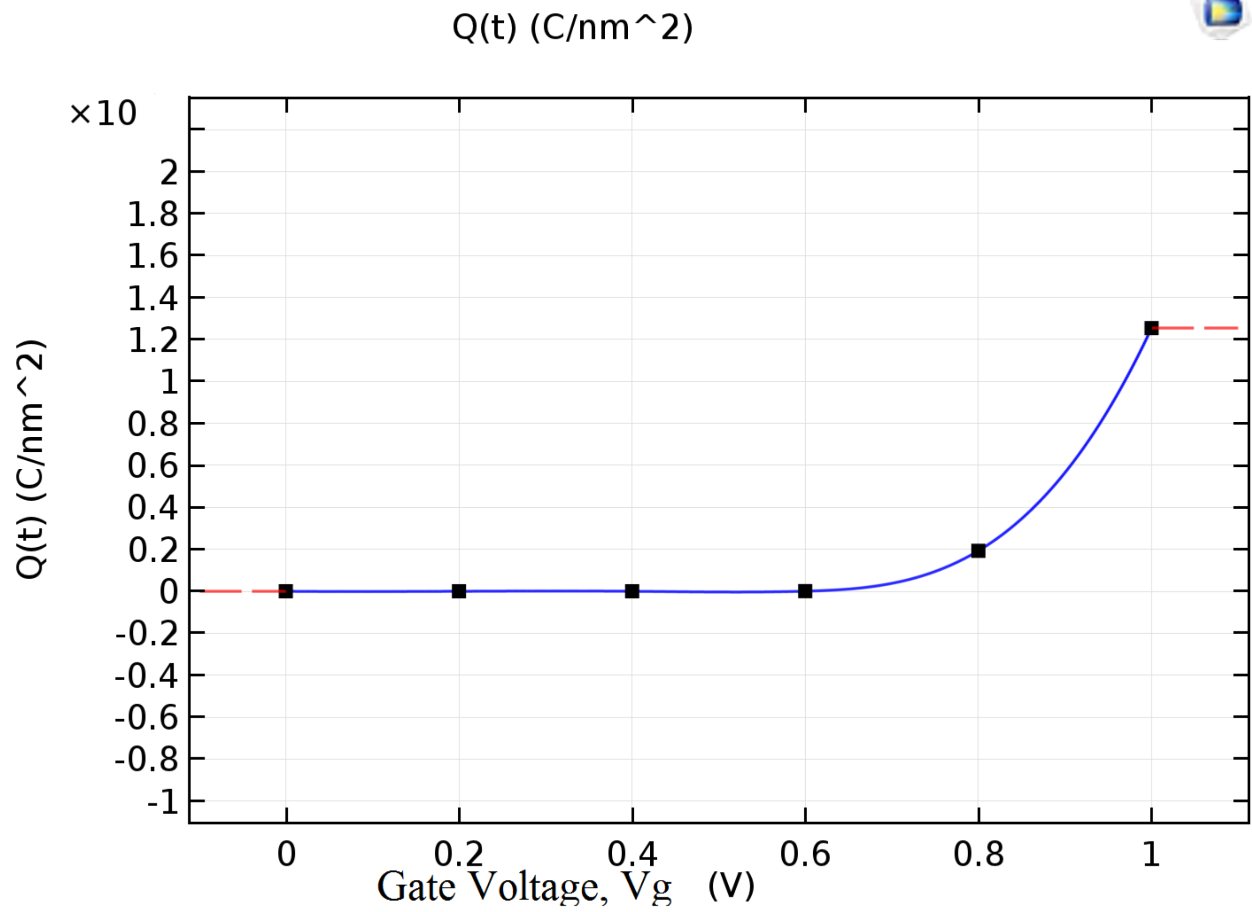

Fig: 8.12: Q-V characteristics at work function 4.7 and oxide thickness 5 nm

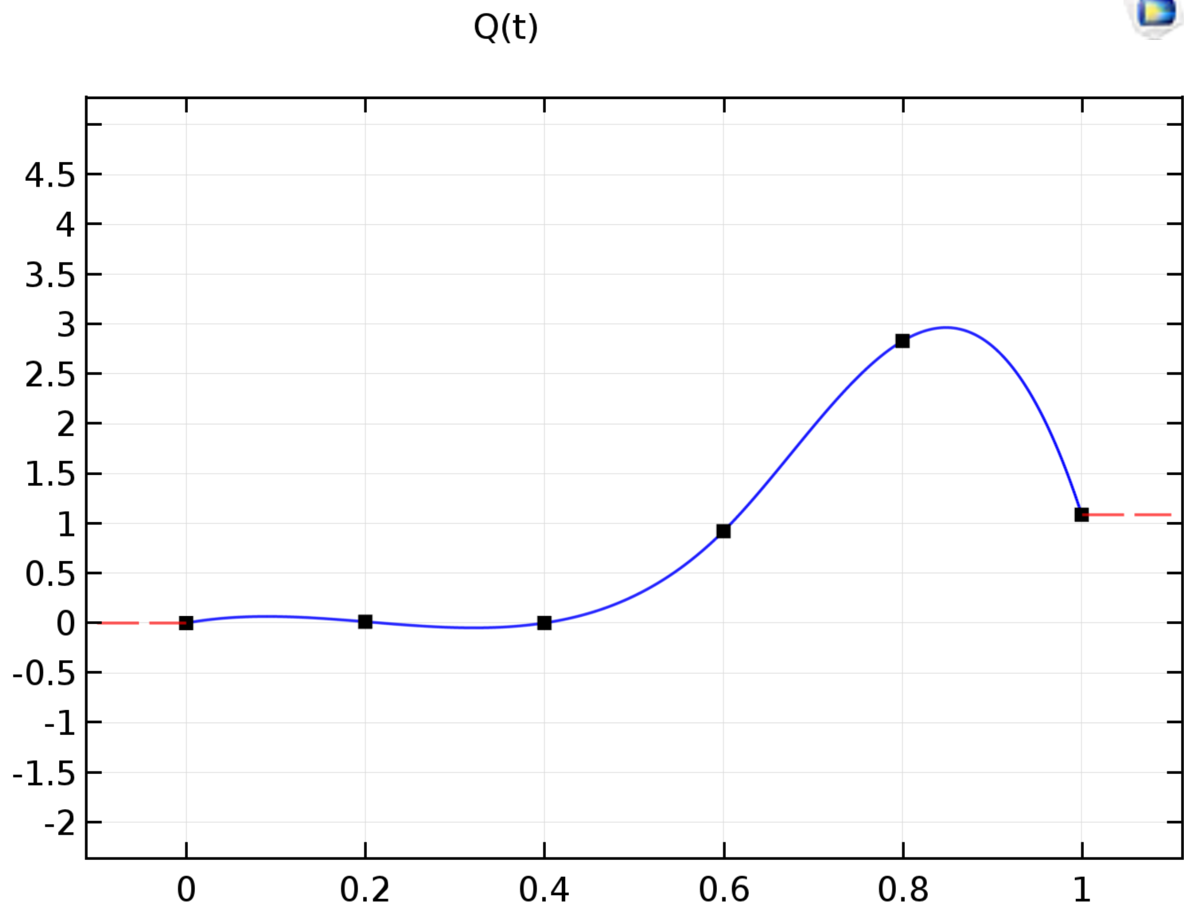

Fig: 8.13: Q-V characteristics at work function 4.7 and oxide thickness 10 nm

9 CONCLUSIONS

In this paper Poisson solver coupled with Schrodinger equation is used to obtain charge density in each point of the channel region of QWFET by carrying out simulations using COMSOL Multiphysics linked with MATLAB simulator by incorporating various electrostatic parameters of different semiconductor materials in suitable domains with suitable boundary conditions. We analyzed the C-V characteristics by altering the gate oxide thickness and metal work function used in the gate of non-planer, multi-gate In GaAs channel Quantum Well Field Effect Transistor (QWFET), and compared with previous research on the same field to demonstrate that reducing the gate oxide thickness does increase the conductance of a material. Limitations were such that the Semiconductor Module in COMSOL may not have given accurate results given a nanoscale structure. We suggest writing a program to properly couple Poisson-Schrodinger where the output from the Poisson solver goes directly into Schrodinger and vice versa at each iteration.

However, our simulation results show that QWFET have shown to improve in performance, scalability and gate control than any other transistors available in recent times. This in turn makes it faster and ideal for lower scaled voltage logic applications and makes it the ideal device to be used in upcoming nano structured based electronics industry.

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