DEVELOPMENT OF AN AUDIO EVOKED RESPONSE SYSTEM TO FACILITATE ANAESTHESIA MONITORING

A Thesis

Submitted by

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DECLARATION

We hereby declare that this thesis is based on results found by ourselves. Materials of this work found by others or taken from other sources have been stated or mentioned in the reference list. This thesis, neither in whole nor in part, has been previously submitted for any degree.

Supervisor

Authors

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ABSTRACT

General anaesthesia allows patients to undergo surgical procedures without the distress and pain they would otherwise experience. However, in about one in five hundred, the anaesthesia does not work, the patient feels the full pain but cannot communicate because of muscles being paralysed by drugs. Existing monitoring techniques depend on indirect measurements or qualitative observations and cannot give the right information in such cases. Heart rate variability and Bispectral Index (the latter based on brain signals, EEG) are recent monitoring techniques, but they too are not also foolproof. When a patient is anaesthetized, the hearing ability is the last sense to disappear, and measuring this ability could give a very good indication of the state of anaesthesia. To assess the hearing ability objectively an evoked brain potential known as Audio Evoked Response (AER) is very effective. As the patient is anaesthetized the AER fades out gradually till it vanishes on full anaesthesia. However this test takes a few minutes, and so is not suitable for instantaneous feedback necessary for drug administration. We feel AER could be useful at least in the beginning, before the actual surgery is started, to ensure that the patient has really been anaesthetized. This could also be repeated at certain intervals during surgery.

The present work is part of an on-going project by the University of Dhaka in developing a practical and effective anaesthesia monitoring system. Previously, aspects of anaesthesia had been studied by another group of BRAC University students and an attempt was made to understand the differences in EEG signals that may be brought about by anaesthesia. In this project we will be examining and developing a PC based AER system.

AER involves producing a series of click stimulii at the patient's ear via a headphone or a loudspeaker and picking up the evoked voltage signals from the brain using electrodes fixed at suitable locations on the patient's head. The AER signals, which are of the order of 10μV, are usually associated with thousands of time larger mains borne 50Hz noise. This noise will need minimization using a front end instrumentation amplifier with a very large CMRR. This will then need to be filtered, further amplified, electrically isolated and received by the computer via an analog interface, which has to have an A/D converter. The click generator will also need to send a trigger pulse to the computer in order to initiate the process of data acquisition for about 500ms each time (considered as one sweep of data) under software control. So development of appropriate software is also an essential part of this project. The reduction of the 50Hz noise using hardware as mentioned above is not adequate for this application. Besides, spontaneous EEG from brain also clutters the signal and appears as noise. Since these noise potentials do not have any phase relationship with the trigger of the evoked response, these can be eliminated using a signal averaging technique, employed through software. About 50 to 100 sweeps of data will be collected and averaged for this purpose.

In the last semester, we gathered relevant information for this project, made the initial overall design, and developed a pulse generator to give a click sound output using a headphone. Narrow electrical pulses (~1 ms width) produced by the click generator could provide the necessary sound stimulus (approximately 60 to 80 db) to the ear via the headphones.

This semester, we first worked on the Front-end amplifier circuit using IC's available in the laboratory. We used an instrumentation amplifier IC - AD521, and made up instrumentation amplifiers using op-amps available in two quad op-amp IC packages - TLO74 and LM324. TL074 has an FET input while LM324 uses bipolar transistors. CMRR values of approximately 104dB, 96dB and 86dB were obtained using AD521, LM324, and TL074 respectively.

Obviously the decision went in favour of using the IC AD521 which requires a few external components to make a complete instrumentation amplifier.

Since this equipment is supposed to be used in a hospital, special electrical isolation circuitry needs to be incorporated to save a patient from 'microshock' hazards that can result from the use of ordinary power transformers, or in case there is an accidental connection of the equipment to the mains live wires. The optical isolation will be performed using an opto-coupler IC 4N35, and an analogue isolation technique, developed at Dhaka University, will be used. Finally the output will be converted to digital values using an 8 bit A/D converter, ADC0820 for acquisition in a PC through its printer port (LPT1).

Software will be developed under MSDOS using either QBASIC or C language. The software will first acquire the trigger signal from the click stimulator. On receiving a trigger it will acquire AER data for about 500ms in one sweep, at a sampling frequency of about 1kHz. It will also perform the task of signal averaging by acquiring the required number of sweeps in succession. The averaged data will be displayed graphically on a video monitor as a function of time. Absence of AER will confirm the success of anaesthesia.

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1. Introduction

1.1) Background

Anaesthesia allows patients to undergo surgical procedures without the distress and pain they would otherwise experience. Anaesthesia basically means 'loss of sensation'. Medications that cause anaesthesia are called anaesthetics.[1] Anaesthetics are used for pain relief during tests or surgical procedures so that patients do not feel pain, touch, pressure and temperature. Types of anaesthesia include Local Anaesthetic, Regional Anaesthetic, Epidural Anaesthetic, Spinal Anaesthetic, Sedation and General Anaesthetic.[2]

Monitoring during anaesthesia is crucial for guiding the anaesthetist and for ensuring that vital parameters are in the safe physiological range, particularly for haemodynamic (dynamic regulation of the blood flow in the brain) and respiratory consequences. Traditional methods include monitoring of pulmonary artery pressure, cardiac output, urine output, invasive blood measurements (like arterial blood pressure), etc. [3] and observation of sweating, and of tears coming out of the eyes. The latter two are very much qualitative, and the former vital signs can be modified by a wide range of variables, including drug administration and surgical impact. Similarly, a large number of variables can interfere with the conduction of anaesthesia, such as age, concomitant disease or therapies, physiological parameters and human variability.

Most anaesthetics are given without monitoring the effect of the anaesthetic on the target organ. Depending on the stimulus, there is a depth of anaesthesia at which the patient becomes aware, i.e the patient can sense the pain even through he or she cannot communicate this situation to others since all the muscles are simultaneously caused to be temporarily paralysed using muscle relaxation drugs. The incidence of awareness or recall during general anaesthesia is about 1 in 500 patients [4] and it usually leads to severe trauma to the patients, some of which can haunt the patients throughout their lifetime.

Several quantitative methods for measuring the depth of anaesthesia like Heart rate variability and Bispectral Index (based on brain signals, EEG) are recent monitoring techniques, but they too are not foolproof. [4]

The present work is a part of an on-going project by the University of Dhaka in developing a practical Anaesthesia monitoring system. Previously aspects of anaesthesia had been studied by another group of BRAC University students and an attempt was made to understand the differences in EEG signal that may be brought about by anaesthesia[1]. In order to obtain a preliminary idea about the parameters of EEG to be used for the above purpose, a study was conducted on normal subjects while awake and while asleep. It was assumed that EEG patterns during sleep may have resemblance to that during

anaesthesia. Obtaining 20 EEG signals from two subjects while asleep and while awake, first the signals were filtered in two frequency windows of 7 to 10Hz and 12 to 15 Hz respectively using Fast Fourier Transforms (FFT). The means, Standard deviations, RMS value and integrals of these FFT values were then obtained. Then ratios of each of these values obtained for the above two frequency ranges were computed for all the data sets (20 each). Subjecting the results through statistical T-tests, it was found that the ratio of the above values of mean, Standard deviation, and integral were highly significant, at $P<0.001$, while that of the RMS value was significant at $P<0.06$. This result is expected since it is known that during sleep, alpha waves of EEG between 7 to 12 Hz become dominant. The various FFT parameters studied gives a direction that can be followed in further work based on EEG only.

It is also well known that when a patient is anaesthetized, his/ her hearing ability is the last sense to disappear, and this, if measured objectively, could give an indication to initiate surgery with confidence. To assess the hearing ability objectively an evoked brain potential known as Audio Evoked Response (AER) is very effective. As the patient is anaesthetized the AER fades out gradually till it vanishes on full anaesthesia. However this test takes a few minutes, and so is not suitable for instantaneous feedback necessary for drug administration. We feel AER could be useful at least in the beginning, before the actual surgery is started, to ensure that the patient has really been anaesthetized. This could also be repeated at certain intervals during surgery. Therefore the present work was taken up to develop an AER system.

1.2) Aims of this Project

In this project, we will be examining and developing a PC-based AER system. Within the limited time frame given for the thesis it is not possible to develop a full fledged AER system ready for clinical measurement. However, we will try to prepare the initial design of the whole system based on studies of the fundamental requirements, make a detailed design of the electronic circuits including the necessary analog computer interface, and develop these circuits as far as possible bringing in improvisations as needed, based on availability of components locally. Preliminary software will be developed for acquisition of AER data into a standard IBM compatible PC.

AER involves producing a series of click stimulii at the patient's ear via a headphone and picking up the evoked voltage signals from the brain using electrodes fixed at suitable locations on the patient's head. These voltage signals, of the order of 10 μVs, with frequency content between 1 Hz and 30 Hz, are accompanied by much larger mains borne 50 Hz noise, whose magnitude is almost the same (common) all over a human body. A good quality differential amplifier (called an instrumentation amplifier) is to be used to minimize this common mode noise. Again, large EEG potentials also appear as noise since most of these are not related to the sound stimulus. These unrelated signals appear randomly with respect to the stimulus and can be eliminated by averaging the evoked potential many times, the technique being called 'signal averaging'. The target signal has the same shape and

phase with respect to the stimulus and therefore adds up in this averaging technique, thus enhancing the signal to noise ratio (S/N). Again, since this equipment is supposed to be used in a hospital, special electrical isolation circuitry needs to be incorporated to save a patient from 'microshock' hazards that can result from the use of ordinary power transformers, or in case there is an accidental connection of the equipment to the mains live wires. Lastly, the analogue signal has to be converted to a time series digital signal and interfaced to a personal computer (PC) through the parallel printer port. The PC will perform necessary data acquisition, signal averaging, analyses, display and data storage through appropriate software. The present work will involve developing the necessary hardware and software for PC-based data acquisition, signal averaging, and display of the resulting AER. The circuitry, including the PC data acquisition system with analogue to digital conversion will be integrated into a single unit. Dhaka University has a long experience in the design and fabrication of such equipment, data acquisition systems and software, and this experience will be used to build a fresh design of AER, specially targeted to anaesthesia monitoring.

Although AER is a part of a whole anaesthesia monitoring scheme as mentioned above, it can be used as a standalone monitoring technique to assess whether a patient is anaesthetized or not. AER is to be the last test before surgery is started.

1.3) Motivation and Justification

Readymade AER systems are already available in the global market. So, the reasons behind building such a system locally are:

- Imported ones are very expensive as they come from economically rich countries where scientific human costs are very high. Therefore, developing such equipment locally will reduce the costs significantly thus making the benefit available to the common people in the Third World.
- Repair and maintenance can be accomplished at low cost if developed and made locally.
- The system can be modified whenever necessary, as we will have full control over the technology.

The next chapters of this thesis presents the work in detail, including the methods used, the developed circuitry and software, and the results of some of the tests performed.

References for this Section

[1] http://www.nhs.uk/Conditions/Anaesthesia/Pages/Introduction.aspx
[2] http://www.datadictionaryadmin.scot.nhs.uk/isddd/37930.html
[3] http://www.articlesbase.com/health-articles/anesthesia-monitoring-1070414.html
[4] http://www.anaesthesiauk.com/documents/3_12_477.pdf

2. Methods

2.1) Audio or Auditory Evoked Potentials (AEPs)

An evoked potential (or evoked response) is an electrical potential recorded from the neuro-muscular system of a human or other animal when a stimulus is presented at a suitable point. [17] It is distinct from the spontaneous potentials as detected by normal EEG or voluntary EMG (Electromyography- which is a technique for evaluating and recording the activation signal of muscles). Evoked potential amplitudes from the brain are usually very low, ranging from less than a μV to several μVs, compared to tens of μVs for EEG, and millivolts for EMG and ECG (Electrocardiography- which is a transthoracic interpretation of the electrical activity of the heart over time, captured and externally recorded by skin electrodes). To resolve these low-amplitude potentials against the background of ongoing EEG, ECG, EMG and other biological signals and ambient noise, particularly that from the mains power line at 50Hz, signal averaging is usually required. The signal is time-locked to the stimulus and most of the noise and other unrelated potentials occur randomly, allowing the noise and unwanted signals to be averaged out with averaging of repeated responses. Signals can be recorded from the cerebral cortex, brain stem, spinal cord and peripheral nerves (the nerves which extend or reside outside the brain and spinal cord, which constitute the central nervous system). Three kinds of evoked potentials have been widely used in clinical diagnostic medicine since the 1970s: auditory evoked potentials, usually recorded from the scalp but originating at brainstem level (ABR, BAER, BSER, BAEP, BSEP), visual evoked potentials (recorded from the brain by giving photo stimulation to the eye), and somatosensory evoked potentials (recorded by stimulating the peripheral nerves with an electrical stimulus and used to assess the function of a patient's spinal cord during surgery). [18]

Our focus is on the Audio Evoked Response (AER). AER is the electrical response produced involuntarily by the brain when a sound stimulus is given to the ears. AER can be used to trace the electrical signal generated by a sound from the cochlear nerve, through the lateral lemniscus to the medial geniculate nucleus and to the cortex. The cochlear nerve, also known as the auditory or acoustic nerve, is a nerve in the head which carries signals from the cochlea of the inner ear to the brain.

There are mainly three types of AER:

- ✓ Early (Brain Stem Evoked Response or BSER): It has a latency of 10 to 20 milliseconds and is not affected by anaesthesia
- ✓ Middle: It has a latency of 40 to 60 milliseconds and is affected by anaesthesia

- ✓ Late: It has a latency of 50 to 500 milliseconds and has additional affects of sleep and sedation

In our project, we are dealing with the middle and slow responses, also known collectively as Slow Vertex Response (SVR).

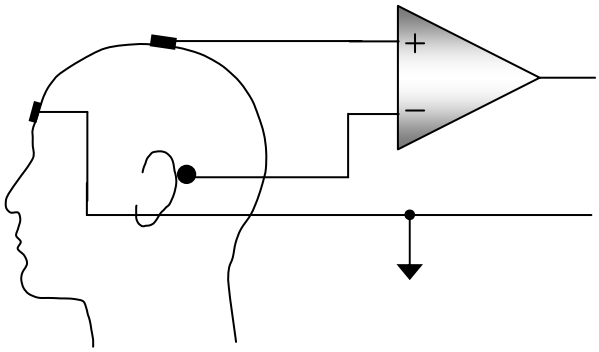

Fig.1: Electrode connection for SVR and BSER

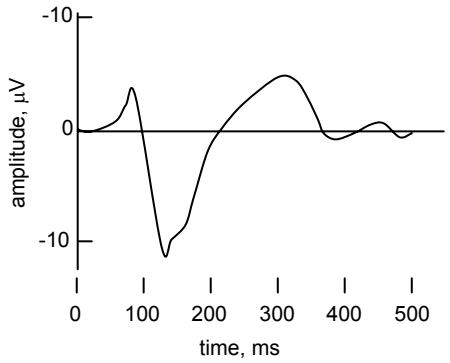

Fig.2: Typical Slow Vertex Response

SVR is thought to be generated by the cortex. It can be recorded by placing a surface electrode on the vertex or crown of the head and measuring the potential with respect to a reference electrode placed behind an ear, on the mastoid bone as shown in Figure 1. The common electrode for the differential input arrangement is usually placed on the forehead. The response (a typical one is shown in Figure 2) has latency (delay) of 50-300ms, i.e. it appears within this period after the sound has been presented to the ear and the amplitude of the response is about 10µV, which is less than the amplitude of the background EEG signal. However, by averaging about 30 responses, the signal can be enhanced adequately. The lowest frequency of the signal is approximately 3Hz while the highest frequency is about 25Hz.

For SVR, the stimulus may be applied as a free field sound generated by a loudspeaker or through headphones. The sound may be a click stimulus, or it may be a filtered tone burst, and is repeated once every 2 seconds. The signal (called a sweep) is usually collected for about one second after a stimulus, and the number of sweeps to be averaged to get an adequately clear signal is about 30.

Each average of 30 stimuli will take about one minute and repeat averages are usually required to check the consistency of the response. In hearing assessment studies such evoked responses are taken at different intensities of the stimulus. However, in the case of anaesthesia monitoring, possibly evoked responses at a single sound intensity level, sufficiently loud, would suffice.

2.2) The AER System

Figure 3 gives a simplified overview of the desired system.

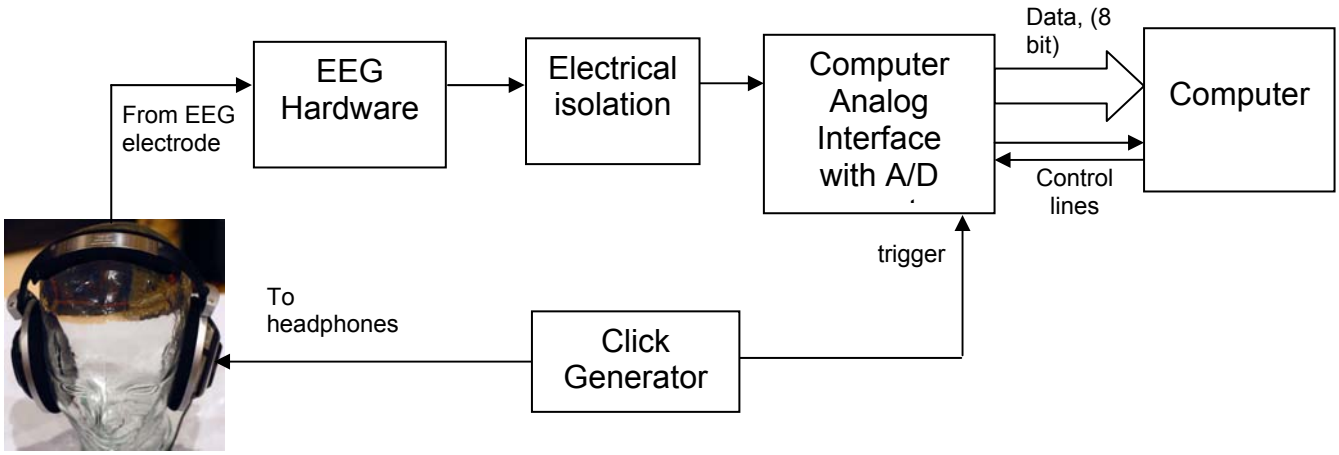

Fig. 3: Block diagram of the AER hardware

Narrow electrical pulses (~1 ms width) produced by the click generator provides the necessary sound stimulus to the ear via the headphones. A loud enough stimulus (approximately 60 to 80 db) is given. Evoked potentials are involuntarily produced by the patient's brain and these are picked up by the electrodes and fed to EEG hardware. The voltage signals are amplified, filtered, electrically isolated and received by the computer via the computer analog interface, which has a built in A/D converter. The click generator also sends a trigger pulse to the computer via the computer interface. This initiates the data acquisition process for each sweep under program (software) control. Each time the computer receives the trigger pulse, it acquires a certain number of data points (e.g., 1000 samples of data) with a particular sampling interval through the interface. The samples are held for a certain interval (of the order of μs), converted from analog to digital form by the analog-to-digital converter, delivered to the computer via the data bus 8-bits at a time, and stored in the computer's memory in an array configuration.

2.3) Necessity of Electrical Isolation

For the AER circuit it is necessary to electrically isolate the patient from the mains electricity connected equipment for the following two reasons:

i) To save the patient from electrical hazards in case of an accident in which the mains 220V ac line touches the patient connected wires directly. Even if this does not happen there is another possibility that currents of the order of 100 μA may flow through a patient if ordinary step down transformers (as used in normal appliances) are used in making low

voltage supplies. Such currents are safe for home and office equipment but are considered a hazard for hospital equipment because a patient may have a direct electrical connection to a heart muscle through a catheter. In that case even 50 μA flowing directly through the heart may be fatal.

ii) Because of a circuit loop created through the patient connected leads to mains ground, 50 Hz mains borne noise is introduced into this circuit through magnetic fluxes crossing this loop. This contributes to a 50Hz common mode voltage noise added to the signal. By providing the electrical isolation, this loop is essentially broken, and the 50Hz common mode noise is minimized.

2.4) Instrumentation Designed

Figure 4 shows the components of the EEG hardware which has been planned and developed for the project. In the present work electrical isolation of the patient end of the circuitry from mains connected equipment has been achieved through the use an opto-coupler to electrically isolate the signal. The circuitry at the patient end is powered by batteries, eliminating the need of power isolation circuitry.

The evoked voltage signals received via the electrodes (showed as V_{in}) are delivered to the Front End Amplifier. Next, the high pass and low pass filters take out dc offsets and noise. The voltage signals are then further amplified and sent to the next block. Here the voltage signals are converted to current signals by the V-to-I converter and the level of
the signal is shifted. Level shifting is done to give a dc bias to the LED of the opto-coupler so that it can operate in both the positive and negative cycles of the input signal. The opto-coupler output gives an analog signal which is proportional to the input signal but is electrically isolated from the patient end circuitry. After further amplification and level shifting, the signal goes to the computer interface with ADC. Level shifting is done again before this stage as the ADC input needs a dc bias. The ADC converts the analog data to digital data on command from the computer which is achieved through appropriate computer interface circuitry. A trigger signal from the click generator goes through the interface to the computer to initiate data acquisition.

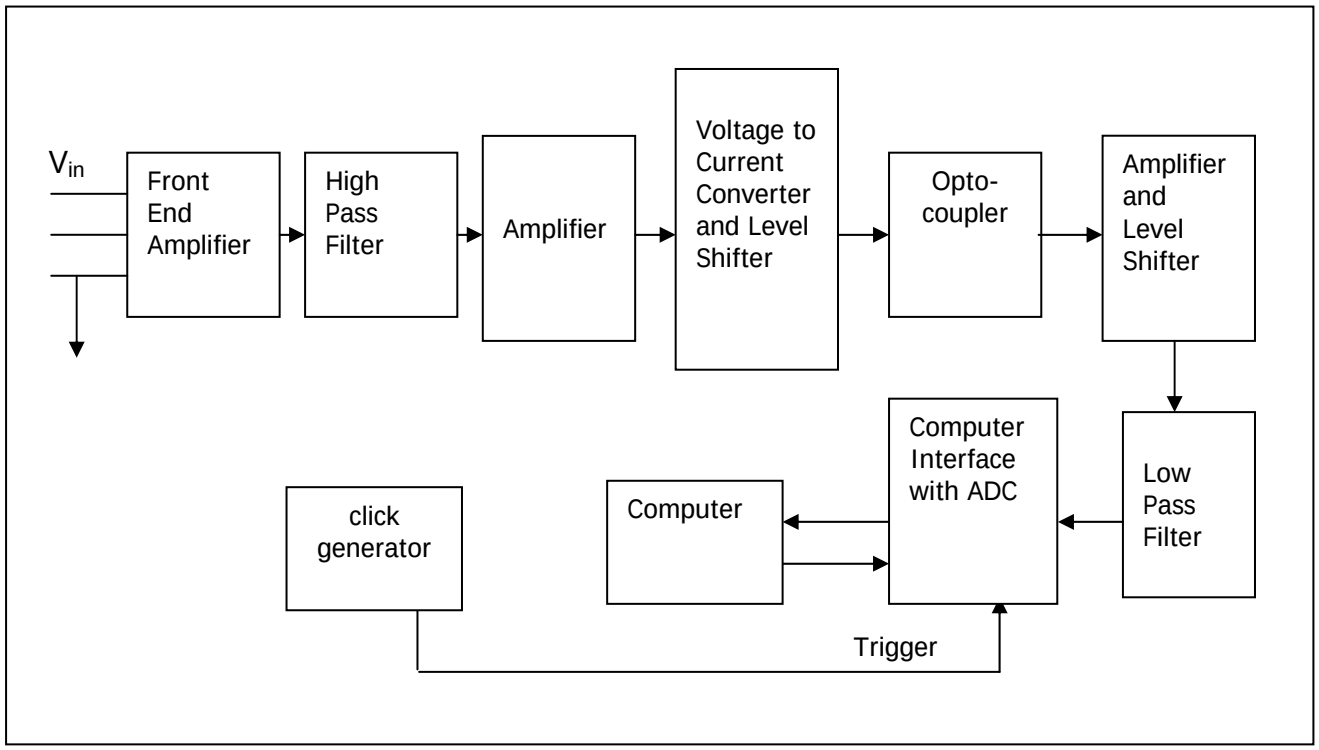

Fig. 4: The AER Hardware and Computer Interface (block diagram)

2.5) Details of the Instrumentation

Our system basically consists of 4 main components: the Click Generator, the Front-End Amplifier, the Electrical Isolation unit and the Computer Interfacing & Data Acquisition unit. These are discussed below.

2.5.1) The Click Generator (Non-Isolated)

The click generator as shown in Fig.5 essentially produces voltage pulses of specific width and height which drives a pair of headphones to produce click sounds repetitively. In the present work a click generator has been made using a 555 Timer IC networked with some resistors and capacitors to make an Astable Multivibrator. An Astable multivibrator is a type of oscillator that has no permanent “steady” state, but continously changes its output from low to high and high to low, producing a continous square wavefrom.

The 555 Timer IC basically operates in either Monostable mode or Bistable mode. The monostable multivibrator has only one stable state and produces a pulse of a specified time duration on receiving an external trigger pulse, after which it reverts back to its stable state again. A bistable miltivibrator has a flip-flop type switching action. It has two stable states, high and low, that can be toggled using a trigger pulse. The Monostable mode of the 555 IC can be used to generate an Astable condition through suitable external connections as described below.

In order to configure a 555 Timer IC into an Astable multivibrator, it is necessary to re-trigger the IC continously after each monostable timing cycle. The basic circuit of an Astable multivibrator using a 555 Timer IC is given in Figure 5.

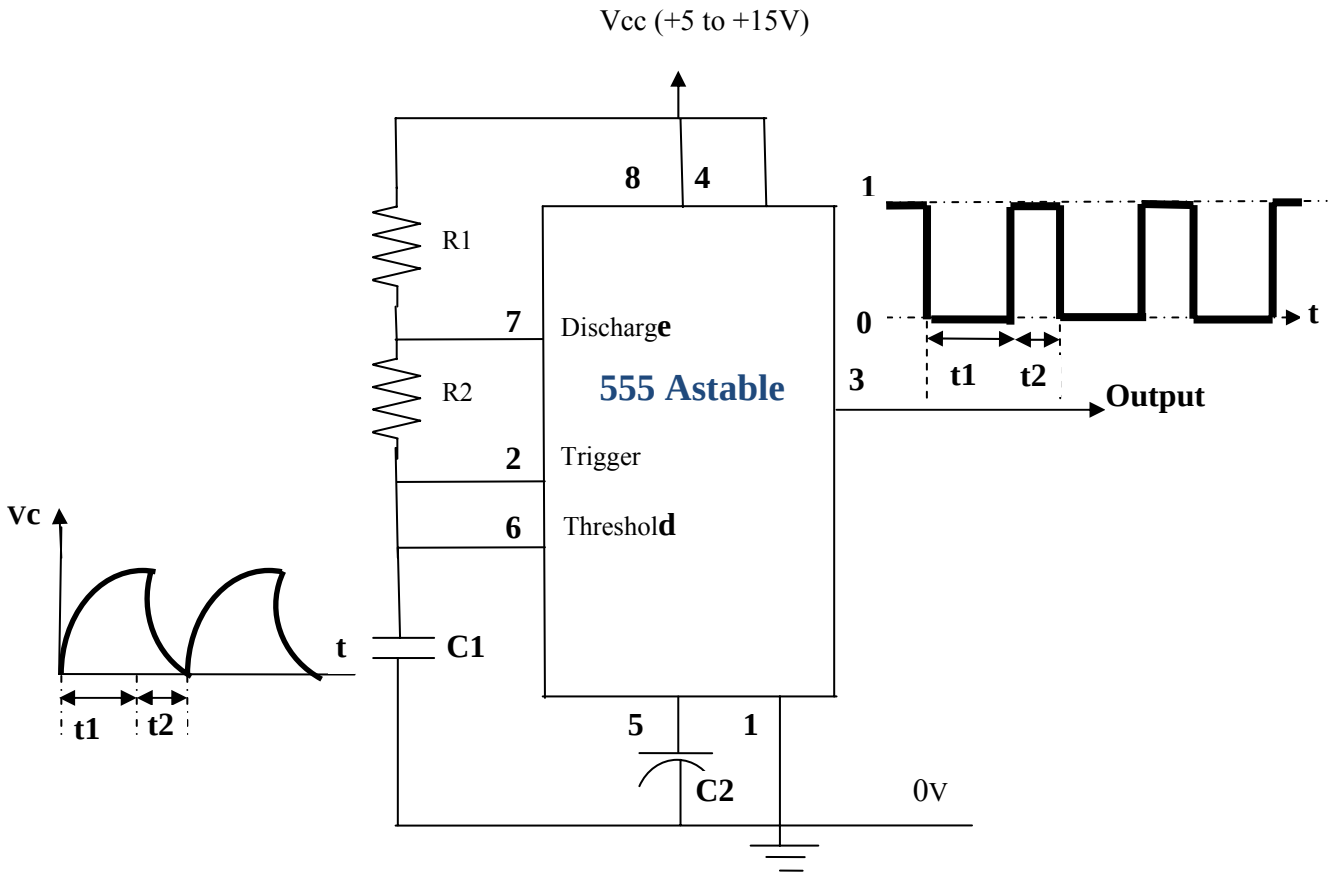

Fig. 5: Basic astable pulse generator using 555 IC

Here pin 2 (trigger) and pin 6 (threshold) are connected together allowing the circuit to re-trigger itself on each and every cycle allowing it to operate as a free running oscillator. Initially the capacitor C1 charges through the series combination of R1 and R2 which has an exponential behaviour as shown on the left hand side of the figure.

The capacitor charges upto $2/3V_{cc}$ (with a target voltage of V_{CC}) the duration of which is determined by the combination of (R1 + R2)C. The output (pin 3) remains high during this charging phase. When the capacitor voltage, i.e., the voltage on pin 6 reaches $2/3V_{cc}$ the internal discharge transistor (connected to pin 7) becomes on and the capacitor discharges down to $1/3V_{cc}$, whose duration is determined by the combination R_2C. During this discharging phase the output at pin 3 remain low. As soon the capacitor voltage (voltage on pin 6) reaches 1/3Vcc, the internal discharge transistor at pin 7 switches off and the capacitor charges again through R1 and R2. This sequence continues indefinitely. The result is an output waveform whose output goes 'ON' or High and 'OFF' or Low repeatedly. The time periods are determined by the capacitor and resistor combination below.

Output ON time = Charging time: t1= 0.693(R1 + R2)C

Output OFF time = Discharging time: t2= 0.693(R2)C

The output will be changing indefinetly, charging and discharging between 2/3Vcc and 1/3Vcc as long as the power supply remains connected.

Therefore, the total time period T= t1 + t2 = .693(R1 + 2R2)C

Connection of the Headphone and choice of R1 and R2:

For the desired click generator a short pulse (~1 ms) is to be repeated about every second. In view of current consumption considerations, R1 needs to be made large, making the charging time, or the output high state of long duration (~1000ms). So we made R2 small to make the discharge time, i.e., the output low state of short duration (~1 ms). To achieve this we used R1 = 1MΩ, R2 = 1 kΩ, and C1 = 1.5μF.

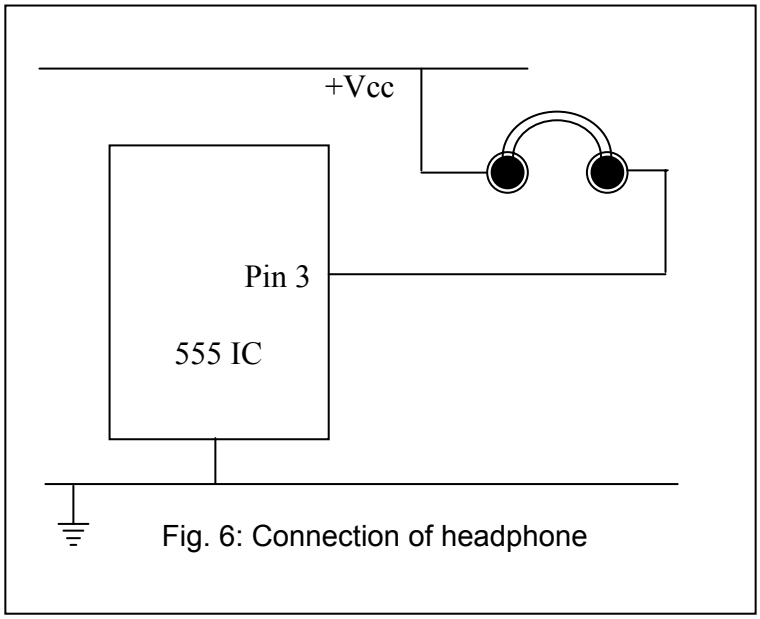

Fig. 6: Connection of headphone

In the above circuit the output is low during t2 and high during t1. This means
t1 ≅ 1000 ms

t2 ≅ 1 ms

The Headphone should take current only during the short 1ms pulse. Therefore, it was connected between the output and +Vcc rail as shown in Figure 6. Pictures of the voltage pulse produced by the fabricated click generator and of the system with the pulse fed to the headphones are shown in Figures 5 and 6 respectively.

2.5.2) The Front-End Amplifier (Isolated)

It has been mentioned previously that the Audio Evoked Response voltage signals received via the electrodes are very low amplitude signals and are easily cluttered by noise. Therefore a special front end amplifier has to be used to make these weak signals stronger, to a manageable signal level.

An amplifier is any device that changes (usually increases) the amplitude of a signal. The relationship of the input to the output of an amplifier (usually expressed as a function of the input frequency) is called the transfer function

of the amplifier, and the magnitude of the transfer function is termed as gain. In popular use, the term usually describes an electronic amplifier, in which the input signal is usually voltage or current. Amplifiers may be classified according to the input (source) they are designed to amplify (such as a guitar amplifier, to perform with an electric guitar), the device they are intended to drive (such as a headphone amplifier), the frequency range of the signals (e.g. Audio, IF, RF and VHF amplifiers), whether they invert the signal (inverting amplifiers and non-inverting amplifiers) or the type of device used in the amplification (valve or tube amplifiers, FET amplifiers, etc.). [1]

An operational amplifier (op-amp) is an amplifier circuit with differential inputs and very high inherent gain (called the 'open loop' gain). High input impedance at the input terminals and low impedance at the output are important characteristics of the op-amp[2]. It amplifies the voltage difference between the two inputs and rejects signals that are common to both the inputs. However, its open loop gain is generally too high to be of any practical use except in a comparator. Besides, the open loop gain varies with temperature, and considerable variation exists between devices with the same identification number. Usually an op-amp's very large open loop gain is controlled through negative feedback, which results in a very much reduced gain (called "closed-loop" gain) that is fairly stable and is almost independent of temperature and variations in op-amp characteristics. Two popular configurations of such feedback gives rise to non-inverting and inverting amplifiers, both having single ended inputs. A differential amplifier is also possible with negative feedback which amplifies the difference of the two inputs and eliminates any signal that is common to both. However, this elimination is not perfect and a parameter called Common Mode Rejection Ratio (CMRR) is of importance in such circuits. It gives a measure of the elimination of the common signal compared to the difference of the two inputs, but is commonly expressed in the reverse, as the ratio of the differential gain to common mode gain. Therefore higher the CMRR, better is the elimination of the common mode signal, and better is the differential amplifier.

Typical biological signals like ECG, EMG and EEG are usually associated with a large noise at the mains power line frequency of 50Hz which is picked up by the human body and associated electrical leads. For example, ECG, EMG and EEG signals are approximately 1mV, 1mV and 30μv respectively while AER signals are even smaller. On the other hand 50Hz mains borne noise has typical magnitudes of about 20mV when a human body is wired up for measurements in premises surrounded by 50Hz power lines and equipment. This means the signal to voltage ratio is very small. Therefore such biological signals cannot be measured using conventional single ended amplifiers where the output voltage is simply proportional to the input voltage, both referred to a common ground potential.

Because of a low internal resistance within the body, of the order of a few hundred ohms, almost the same 50Hz noise voltage (20mV) appears throughout the body with respect to the common ground potential. This gives an opportunity of eliminating this large noise using a differential amplifier. The two input electrodes are attached such that the biological signal of interest

appears as a differential signal, and as already mentioned, the 50Hz noise appears in common mode to both the inputs. Typically, at least 60dB of CMRR is necessary to record ECG signals of 1 mV amplitude, while almost 100dB is required for AER signals, which are less than 10μV in amplitude. Of course this also requires further signal to noise ratio enhancement using signal averaging which will be described later. The figure below shows a basic differential amplifier followed by a brief analysis.

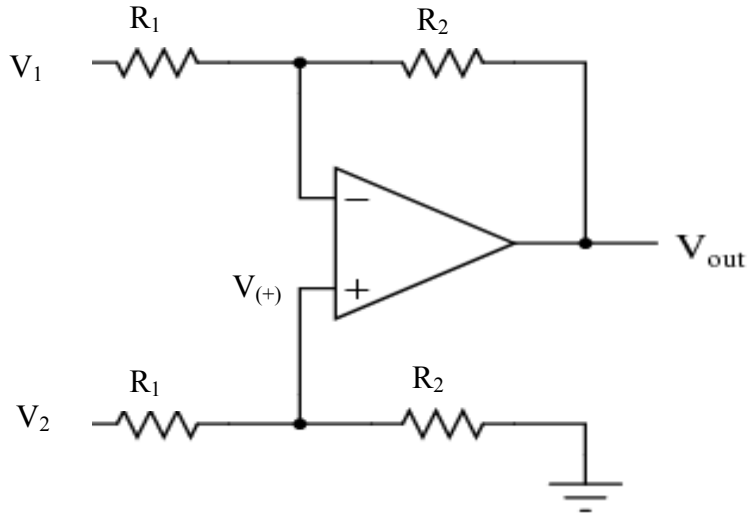

Fig. 7: A Differential Amplifier

Here V_1 and V_2 are the two inputs, and the voltage gain may be obtained using the Superposition principle. One needs to note that the actual non-inverting input $V_{(+)}$ to the op-amp has been reduced by a voltage divider consisting of R_1 and R_2, the reason for which will become apparent as one follows through the analysis given below.

i) Firstly with $V_2 = 0$, $V_{out\_1} = -(R_2/R_1)V_1$

ii) Then with $V_1 = 0$, $V_{out\_2} = [1 + (R_2/R_1)]V_{(+)}$

$= [(R_1 + R_2)/R_1)]\ (V_2)(R_2)/(R_1+R_2) = (R_2/R_1)V_2$

iii) Therefore, the total output:

$V_{out} = (R_2/R_1)\ (V_2 – V_1)$

i.e., the output voltage is proportional to the difference of the input voltages.

iv) Therefore, the Differential Voltage Gain, $A_d = V_{out}/(V_2 – V_1) = (R_2/R_1)$

For a special case, if $R_1 = R_2$, then the Gain = 1

There is another problem while picking up electrical signals from the human body. The skin has a high electrical resistance, and any electrode fixed on to the skin surface has a typical resistance between 5kΩ and 20 kΩ, depending on skin preparation, size of the electrode, and the metal used. These contact

resistances can jeopardize the whole design of the above differential amplifier since these appear in series with the resistances at the inputs. Therefore two more op-amps are used at the front to isolate this input electrode impedance. These op-amps can also be wired up to provide a further differential gain with a high CMRR. This whole combination is called an instrumentation amplifier which we will use in our project. Thus an instrumentation amplifier is a type of differential amplifier with a very high CMRR and high input impedance, practically unaffected by source impedance variations.

The instrumentation amplifier:

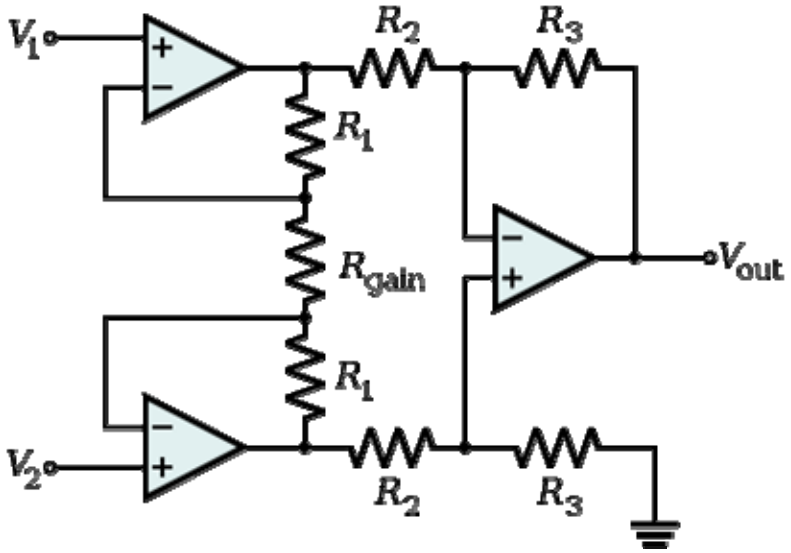

Fig. 8: A Typical Instrumentation Amplifier Configuration

In the Instrumentation amplifier the two inputs of the basic differential amplifier have been buffered by two op-amp circuits which have almost zero output impedances and almost Infinite input resistances. These buffers pick up the source voltage from the electrodes on the body without any drop, and deliver their output voltages, at zero output resistance, to the inputs of the basic differential amplifier. This solves the input impedance mismatch problem. A further twist of adding three resistors in a chain to the outputs of the two front end op-amps transform this part to another differential amplifier, with double ended inputs and double ended outputs, contributing to a very high CMRR. The gain of this front end differential amplifier can be regulated simply by changing a resistor, R_{gain}.

This instrumentation amplifier combines very high input impedance, very high gain, high common-mode rejection, low DC offset, low drift, low noise and other properties used in making very accurate, low-noise measurements and for short and long-term stability. [5]

The total gain of the circuit is:

$V_{out}/(V_2-V_1) = (1 + (2R_1/ R_{gain}))(R_3/ R_2)$. [6]

The rightmost amplifier, along with the resistors labeled R_2 and R_3 is just the standard differential amplifier circuit, with gain = R_3/ R_2.

It increases differential-mode gain of the buffer pair while leaving the common-mode gain to a low value. This increases the CMRR of the circuit and also enables the buffers to handle much larger common-mode signals without clipping than would be the case if they were separate and had the same gain. Another advantage of the method is that it boosts the gain using a single resistor rather than a pair, thus avoiding a resistor-matching problem (although the two R_1 resistors need to be matched), and very conveniently allowing the gain of the circuit to be changed by changing the value of a single resistor. A set of switch-selectable resistors or even a potentiometer can be used for $R_{gain,}$ providing easy changes to the gain of the circuit, without the complexity of having to switch matched pairs of resistors. [6]

We can change the differential gain of the instrumentation amplifier simply by changing the value of R_{gain}. We could change overall gain by changing the values of some of the other resistors but this would necessitate balanced resistor value changes for the circuit to remain symmetrical. The lowest gain possible can be obtained with R_{gain} completely open (infinite resistance) and that gain value is 1. [9]

As it has been mentioned earlier, the ideal common-mode gain of an instrumentation amplifier is zero. In the circuit shown, the common-mode gain is caused by mismatches in the values of the equally-numbered resistors and by the mismatch in common mode gains of the two input op-amps. Obtaining very closely-matched resistors is a significant difficulty in fabricating these circuits, as is optimizing the common mode performance of the input op-amps[6]. In practice R_3 connected between the ground and the non-inverting input is usually a variable resistance, which is adjusted to obtain the highest CMRR experimentally. Then the resistors are automatically matched.

An instrumentation amplifier can be made using discrete op-amps, however, the CMRR remains limited to about 100 dB. Instrumentation amplifier IC's are nowadays available with individually monitored LASER trimmed resistors, taking CMRR to a staggering 120dB! However, external input circuitry usually reduces these values to some extent.

Earlier on, we had decided on using the INA110 IC in our front-end amplifier circuit. Some of the essential features of INA110, which influenced our decision, are given below: [11]

- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 4µs to 0.01%
- HIGH CMR: 106dB min; 90dB at 10kHz
- INTERNAL GAINS: 1, 10, 100, 200, 500
- VERY LOW GAIN DRIFT: 10 to 50ppm/°C
- LOW OFFSET DRIFT: 2µV/°C
- LOW COST
- PINOUT SIMILAR TO AD524 AND AD624

- APPLICATIONS
  - MULTIPLEXED INPUT DATA ACQUISITION SYSTEM
  - FAST DIFFERENTIAL PULSE AMPLIFIER
  - HIGH SPEED GAIN BLOCK
  - AMPLIFICATION OF HIGH IMPEDANCE SOURCES

	INA110[11]
Gain (V/V)	1, 10, 100, 1000
Non-Linearity (+/-)(Max)(%)	0.01
Input Bias Current (+/-)(Max)(nA)	0.05
Output Offset (+/-)(Max)(uV)	3000/G
Input Offset Drift (+/-)(Max)(uV/Degrees Celsius)	2
Output Offset Drift (+/-)(Max)(uV/Degrees Celsius)	50/G
CMRR (Min)(dB)	106
Bandwidth at G=100 (Min)(kHz)	470
Noise at 1kHz (Typ)(nV/rt(Hz))	10
Vs (Min)(V)	12
Vs (Max)(V)	36
Quiescent Current (+/-)(Typ)(mA)	3
Pin/ Package	16PDIP, 16SOIC

INA110 Pin Configuration

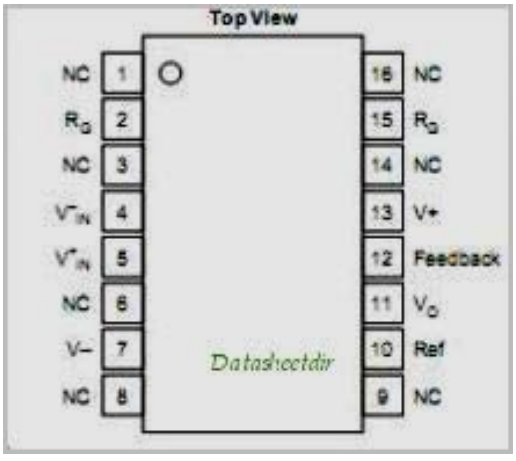

Fig. 9: INA110 Pin Diagram

Other than INA110, we used an instrumentation amplifier IC- AD521 and made up instrumentation amplifiers using op-amps available in two quad op-amp IC packages- TL074 and LM324. TL074 has an FET input while LM324

uses bipolar transistors. We measured the common-mode gains (A_{CM}) and the differential gains (A_d) of these instrumentation amplifiers from which we determined the Common Mode Rejection Ratio using the formula: CMRR = A_d / A_{CM}.

The detailed results are given in *Section 3: Results and Observations*. We found that the CMRR was the highest for AD521 IC, and decided to use this IC in our circuit. This IC also needs only a few external components to make a complete instrumentation amplifier.

AD521 Features[12]

Programmable Gains from 0.1 to 1000
Differential Inputs
High CMRR: 110dB min
Low Drift: 2μVs/^{o}C max (L)
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Very Low Noise: 0.5μVs p-p, 0.1Hz to 10Hz, RTI @ G = 1000
Chips are Available

Other Features of AD521

- AD521 is a true instrumentation amplifier in integrated circuit from offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
- The AD521 has low guarantee input offset voltage drift (2μVs/^{o}C for L grade) and low noise for precision, high gain applications.
- The AD521 is functionally complete with the addition of the two resistors. Gain can be preset from 0.1 to more than 1000.
- The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
- Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
- Offset nulling can be achieved with an optional trim pot.
- The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.

AD521 Description

The AD521 is a second generation, low cost monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier,

the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, high linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the extended temperature range: -55°C to +125°C.

Pin Configuration of AD521

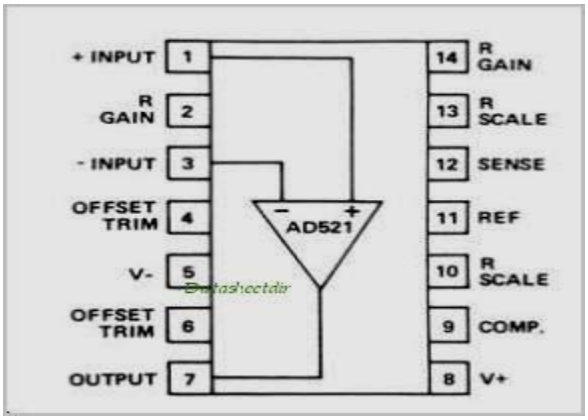

Fig. 10: AD521 Pin Configuration

The Front-End Amplifier Circuit Using AD521 and LM324

The Slow Vertex Response, i.e. the response from the patient's head which we will be monitoring, has amplitude of approximately 10μV. Our computer interface needs approximately 1V for displaying the response. So, the required gain is 1V/10μVs or 100, 000. We already get a gain of 100 from the instrumentation amplifier stage using AD521. So, to get a further gain of 1000, we are using the LM324 IC. We are using only 1 of the four operational amplifiers present in the IC. Another one is used in our electrical isolation circuit. The circuit diagram of our Front-End Amplifier circuit, using AD521 (for a gain of 100) and LM324 (for a gain of 1000) is shown in Figure 11.

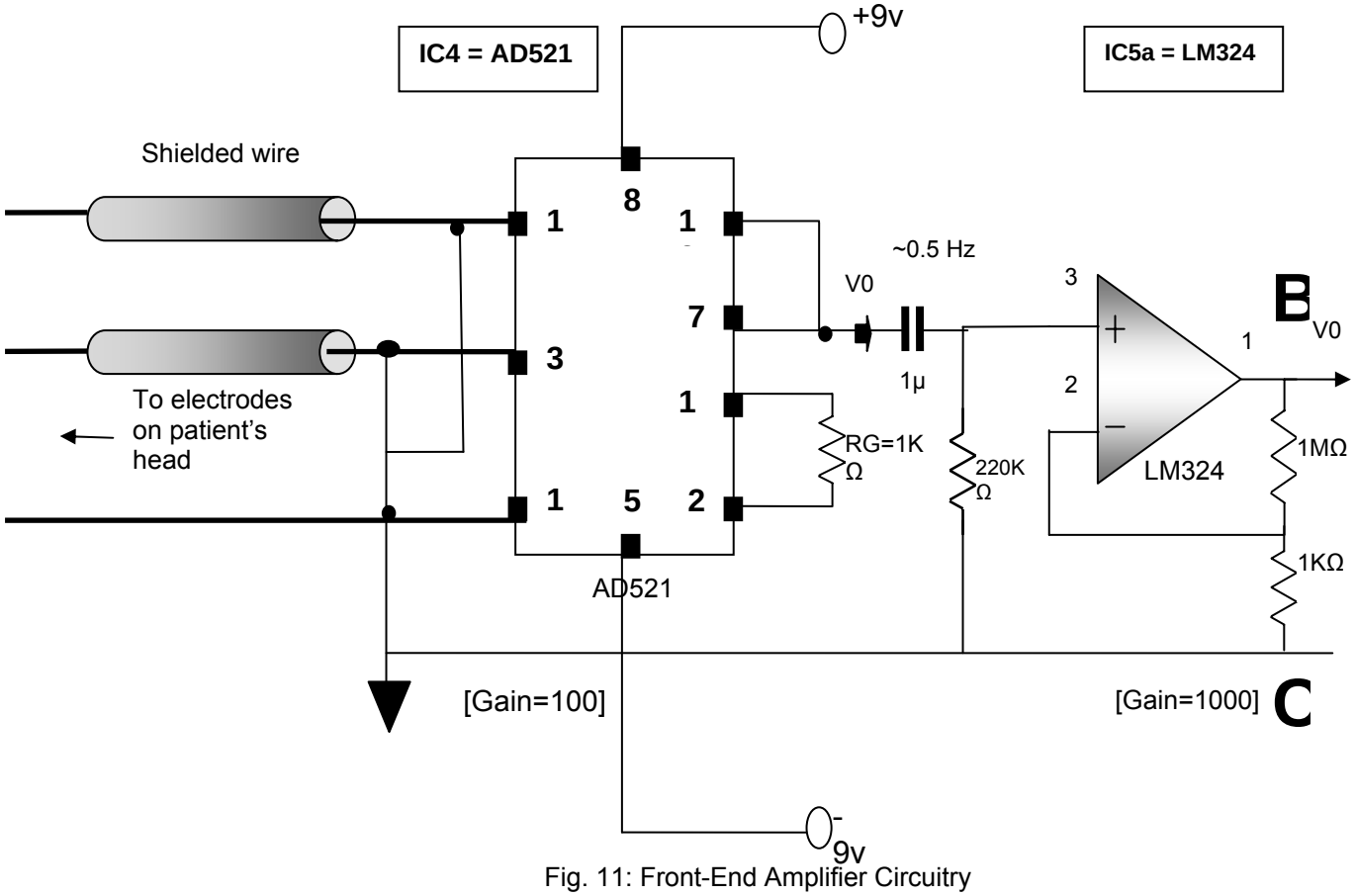

Fig. 11: Front-End Amplifier Circuitry

The audio evoked potentials come via shielded wires from electrodes fitted to the patient's head and are received via input pins 1 and 3 of the AD521 IC. R_G has a value of 1kΩ for a gain of 100. So, the signal is amplified by that order. The signal then passes out of output pin 7 and goes to the high pass filter, which has a cutoff frequency of approximately 0.0723Hz and consists of a 220kΩ resistor and a 10µF capacitor. DC offsets and noise are filtered out and the signal arrives at input pin 3 of the LM324 IC. The LM324 circuit is in non-inverting configuration and the resistor values of 1MΩ and 1kΩ mean that the signal will be amplified by a further 1000 times. This output signal is then fed to the optical isolation circuit via a level shifter. This part of our instrumentation is isolated to ensure patient safety.

The LM324 pin diagram and characteristics are given below:

Pin Configuration of LM324

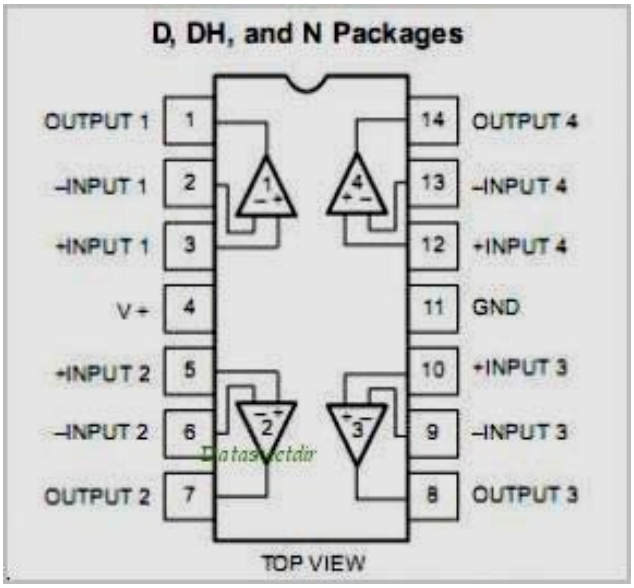

Fig. 12: LM324 Pin Configuration

LM324 Features

- Supply Voltage, V+ : 32V
- Differential Input Voltage : 32V
- Input Voltage : −0.3V to +32V
- Input Current (VIN < −0.3V) : 50 mA
- Operating Temperature: 0^{o} - $+70^{o}C$
- Input Offset Voltage: 7mV (maximum)
- Input Bias Current: 250nA (maximum)
- Input Offset Current: 50nA (maximum)
- Input Common Mode Voltage Range: 0V(min), V+ -1.5 (max) V
- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range: Single supply 3V to 32V or dual supplies ±1.5V to ±16V
- Very low supply current drain (700 μA)-essentially independent of supply voltage
- Low input biasing current 45 nA (temperature compensated)
- Low input offset voltage 2 mV and offset current: 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V^{+} - 1.5 V

LM324 Description

The LM324 consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM324 can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Changes Made in the Circuitry

We had tested our AD521 and LM324 ICs separately at first on a breadboard. The AD521 IC gave the required gain of 100. When we set the input voltage to 10mV, the output voltage was the required 1V. As for the LM324 IC, an input voltage of 5 mV was given and for a gain of 1000, we got the required output voltage of 5V. However, we could not test the circuit by connecting the AD521 and LM324 together as the gain was 100,000, and the input voltage had to be set to a very low level (preferably in the μV range) , in a noise fee condition to see the output within the V_{cc} range. This needed housing the whole circuitry in a shielded environment to eliminate external interference.

2.5.3) Analog Electrical Isolation using an Opto-coupler

The reasons for electrical isolation have been stated earlier in our thesis: to save the patient from electrical hazards in case of an accident where the mains 220V ac line touches the patient connected wires directly and to minimize the effects of the 50Hz common mode voltage noise added to the patient's signal.

This electrical isolation, also known as optical isolation, may be provided effectively using an opto-coupler. An Optocoupler is a device that uses a short optical transmission path to transfer an electrical signal between two isolated electronic circuits. Here the electronic signal is converted to a light beam, typically using an LED (Light Emitting Diode), transferred optically, and then converted back to an electrical signal in a separate destination circuit employing photodiodes or phototransistors. [http://en.wikipedia.org/wiki/Opto-isolator]

When an electrical signal is applied to the LED of the opto-coupler, it illuminates the photo-detector producing a corresponding electrical signal in the output circuit. With a photodiode or a phototransistor as the detector, the output current is proportional to the intensity of the incident light supplied by the LED. The diode can be used in a photovoltaic mode or a photoconductive

mode. The photovoltaic mode is used to obtain power in solar cells rather than for sensing light. Here the output current and the voltage are dependent on the load impedance and the light intensity. In photoconductive mode, the magnitude of the reverse biased or short-circuit current is directly proportional to the intensity of light. The optical path may be air, providing electrical isolation. When high noise immunity is required an optical conductive shield can be integrated into the optical path.

Opto-couplers typically come in 6pin to 8pin IC packages but are essentially a combination of two distinct packages, an optical transmitter typically a gallium arsenide LED and optical receiver such as a silicon photo-transistor. The two are separated by a transparent barrier which blocks any electrical current flow between the two, but does allow the passage of light. Opto-couplers are basically meant to be used as digital or switching devices. So they are best for transferring on-off control signals or digital data. Analog signals can be transferred by the means of frequency or pulse –width modulation using such optocouplers.[13]

The opto-coupler IC which we have used in our project is the 4N35. The pin diagram of the 4N35 and some of its characteristics are given below:

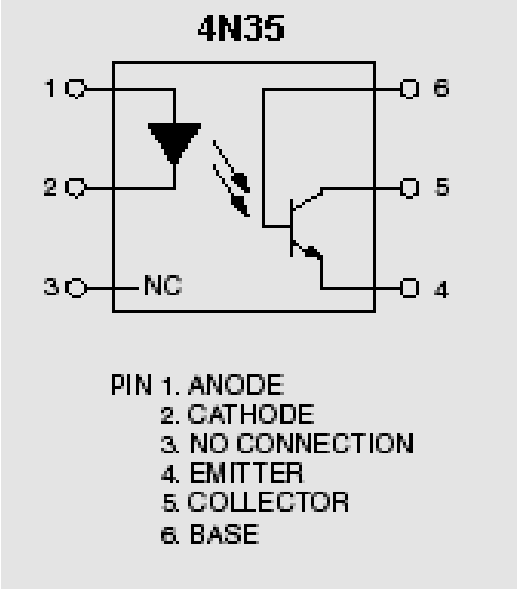

Fig. 13: 4N35 Pin Configuration

Characteristics and absolute maximum ratings of 4N35 are as follows:

- Gallium arsenide infrared emitting diode driving a silicon phototransistor in a 6-pin dual in-line package
- Average Forward Input Current of emitter: 60mA
- Reverse Input Voltage: 6V

- LED Power Dissipation at 25^{o}C: 120mW
- Collector-Emitter Voltage of detector: 30V
- Collector-Base Voltage of detector: 70V
- Emitter-Collector Voltage of detector: 7V
- Detector Power Dissipation at 25^{o}C: 150mW
- Maximum Input Forward Voltage (at a test condition of 10mA forward current): 1.50V
- Maximum Reverse Leakage Current (at a test condition of 6.0V of reverse input voltage): 10μAeres
- Collector-Emitter Breakdown Voltage: 30V (minimum), 100V (typical)
- Collector-Base Breakdown Voltage: 70V (minimum), 120V (typical)
- Emitter-Collector Breakdown Voltage: 7V (minimum), 10V (typical)
- Collector-Emitter Dark Current: 50nA
- Collector-Base Dark Current: 20nA
- Capacitance: 8pF

Digital or analogue isolation, our choice

Our requirement is to isolate an analogue signal. This we can achieve using an optocoupler in two ways – digital and analogue. In digital mode, we have to first convert the analogue signal into a digital form, electrically isolate it using the optocoupler, and then revert to the analogue signal using a digital to analog converter. In the analogue mode the optocoupler is biased in the linear range of operation and an analog signal is fed directly, to get an analogue output. However, the LED intensity may vary with temperature, therefore the dc value of the output in an analogue isolation may not remain error free. However, in our application since we are using only ac signals, the dc can be blocked off, so it may be possible to use analogue isolation, which we have chosen for or work.

Design of the analogue isolation circuitry:

As mentioned before, a problem with analogue isolation circuitry is that there is a slight temperature dependence of the LED which is expected to change the transfer function. However, it is only the dc value which changes significantly, the slope of the transfer function does not change significantly.

Since we are interested in only the ac component of a signal, the slope of the transfer function is important, which does not change significantly. Again, the phototransistor current of a silicon device does not change significantly with temperature if the light level is reasonably high. Therefore, based on such understanding, local ingenuity has led to this improvised analogue opto-isolator using commonly available opto-coupler packages (Ref. Rabbani, Dhaka University, personal communication). Tests have shown that for measurements of bioelectrical signals this optical isolation is serves the purpose very well. This is further explained below.

Light output from an LED is almost linearly related to its forward current, i.e., if I_F is the forward current and Q is the light output, then,

$Q \propto I_F$

Again the collector current I_C of a phototransistor is almost linearly related to its light input, i.e.,

$I_C \propto Q$

Therefore, combining, we get,

$I_C \propto I_F$

This relationship has been effectively used in this design of the analogue opto-isolator as shown in the following circuit. Here the input voltage V_{in} is fed to a voltage-to-current (V to I) converter circuit based on an op-amp. The LED of the opto-coupler forms the feedback loop of this V to I converter. Here, since the non-inverting input is grounded, the voltage of the inverting input would be zero in the presence of a negative feedback, and would be at virtual ground. Therefore, the input current is

$I_1 = V_{in} / R$

Since no current goes into the input of an ideal op-amp, all the current goes into the feedback loop, and through the LED. Therefore,

$I_2 = I_1 \propto V_{in}$

This shows that the current in the feedback loop is proportional to the input voltage, and this circuit forms a basic V to I converter. These behaviours are sketched in Figure 14.

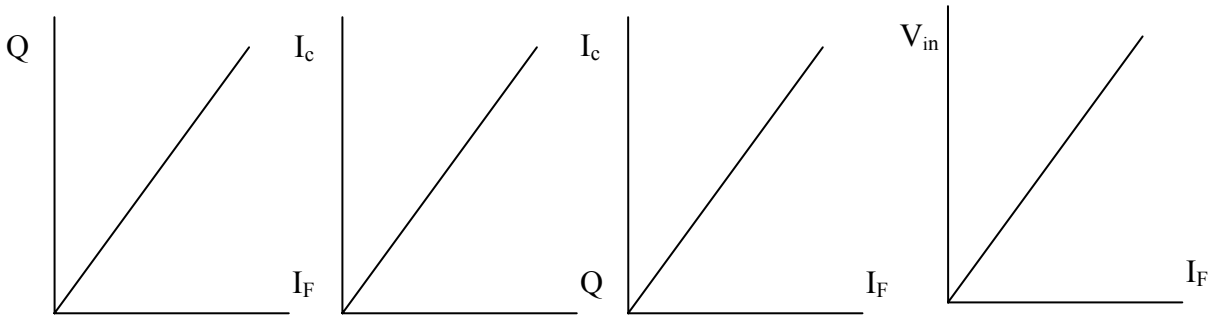

Fig. 14: Voltage to Current Conversion

However, to have current through the LED in both the positive and negative half cycles of the input it is necessary to add a dc bias which has been done by obtaining a dc voltage from $+V_{cc}$ rail of the isolated part of the circuit through a preset resistor. The preset resistor was actually used to set the Q point. This operation is performed by the part of the analogue isolation circuitry marked as Part A, which is basically a summing amplifier. The output voltage V_{out} on the non-isolated side is proportional to the collector current of the phototransistor (with an inverted phase). The dc power supply and the grounds on the two sides of the opto-coupler are entirely separate, and it is usual to drive the isolated section with battery power to keep it completely isolated and hazard free for the patient. The symbols of these parameters are therefore shown different in the figure. A high pass filter has been used at the output to block the dc bias obtained in this arrangement.

Figure 15 shows the analogue isolation circuit used in the present work. It is basically a summing amplifier, which again is based on an inverting amplifier principle.
The output current of the opto-coupler is proportional to the ac input voltage V_{in}.

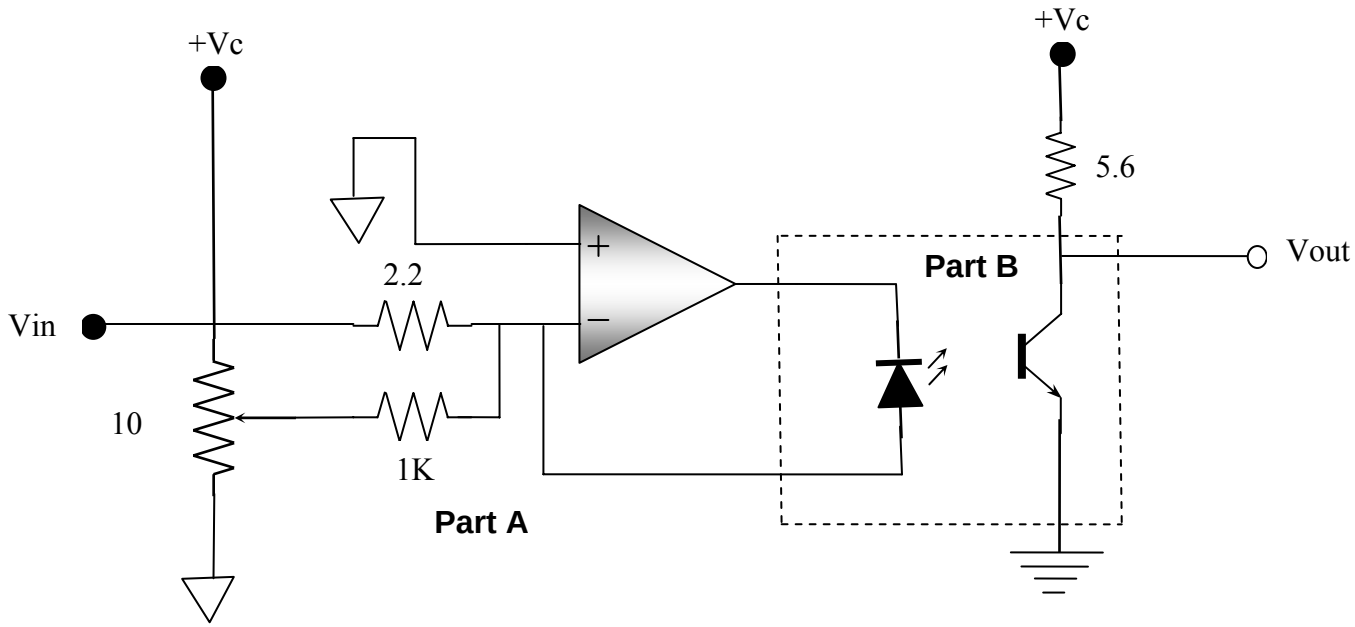

Fig. 15: Analog Isolation Circuitry

Here the ac input V_{IN} is added with an adjustable dc voltage obtained from V_{CC} using at the summing point (inverting input of op-amp). In fact the currents through the two input channels are summed which flows eventually through the feedback path which incorporates the LED of the opto-coupler. The light output of the LED is proportional to the sum of the currents. On the non-isolated side, the current through the collector of the phototransistor will be proportional to the light output of the LED. The bias voltage of the phototransistor can therefore be controlled by the dc current going into the input of the op-amp. In our work the Q-value of the collector of the phototransistor was maintained at ½ V_{CC} by adjusting the dc input to the op-amp using the potentiometer shown.

Finally the dc from the output is removed using a high pass filter (not shown in the above diagram). The relevant waveforms at different points of the above circuit are shown below in Figure 16.

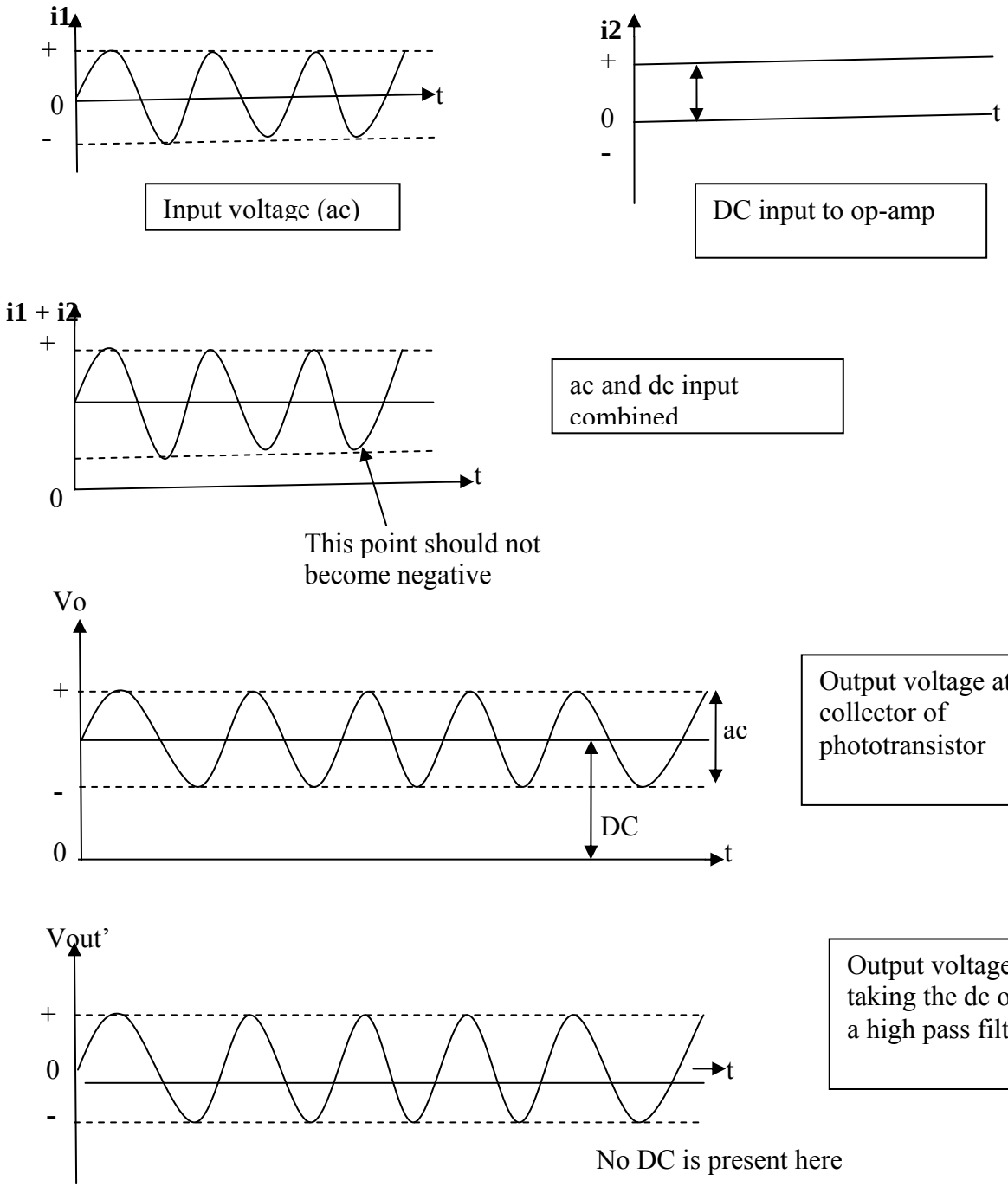

Fig. 16: Waveforms after different operations in the opto-isolator designed

2.5.4) Further Amplification (non-isolated)

One of the four op-amps of an LM324 IC (the other three have been used in the voltage divider circuit) has been used in non-inverting configuration to amplify the signal from the opto-coupler (isolated section) from which the dc bias was removed by a high pass filter. The signal has been amplified by an order of 2 and sent to a low pass filter having a cutoff frequency of 482 Hz (Resistor value: 10kΩ and Capacitor value: 0.033μF). From the filter, the signal goes to ADC0820.

2.5.5) ADC Circuitry

An interface is a point of interaction between two systems or work groups. Here we mean the interfacing between conventional electronic circuits and the computer, so that the information can be transferred between the two devices.

When we want to connect a computer to any outside electronics for data acquisition or control purposes we have to check whether the electrical characteristics of terminals or ports (input/output) of the outside electronic circuitry matches with the characteristics of the appropriate terminals or ports (output/input) of the computer or not. Here matching mainly means compatibility in terms of voltage levels and impedance characteristics.

The computer itself is an electronic device capable of executing instructions to and from the external hardware in order to establish communication with it. All of this has to be performed under program or software control run from the computer. These commands are basically given by human and are called the program or software stored in the computer. The special electronic hardware needed to adapt any electronic device to the requirements of a computer, and the software necessary to perform the desired function, together, is called computer interfacing.[14]

As we know that the computer is basically a digital electronic device, that involves the two voltage levels which are represented by 0V and 5V respectively. These levels represent the two binary logic ‘0’ and ‘1’ where 0 represents low and 1 represents high respectively. A programming language enables the programmer to write the programs that are more or less independent of a particular type of computer. Such languages are considered as the high level languages because they are closer to human languages and far from the machine languages. A human programmer needs to know the particular machine language that a computer understands. If the program is written in binary codes like (000, 001, 011 etc) then these are called the low level languages which is very closer to the machine languages. Most of the time a program is written in certain English words, which is easier to read, write and maintain. Ultimately a program written in high level language must be translated to the machine language by the interpreter or compiler to be understood by the computer.[15]

Data acquisition involves acquisition of signals and waveforms and processing the signal to obtain desired information. The components of data acquisition systems include appropriate sensors that convert any measurement parameter to an electrical signal. The signal or physical property can be temperature, change of light source, force applied on an object etc. In our case, we are taking the trigger from the click generator as the analog input signal.

Analogue interfacing

Our known world is mostly analogue where values change continuously from a minimum to a maximum, and ideally, these can assume any value within the allowed range. Since a digital computer cannot take such analogue information we need an analog-to-digital converter (abbreviated ADC, A/D or A to D) which converts continuous signals to discrete digital numbers.

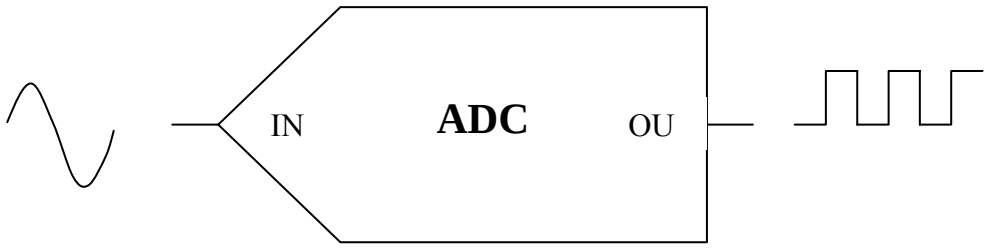

Fig. 17: Analog-to-Digital Conversion

An ADC is an electronic device that converts an input analog voltage (or current) to a digital number proportional to the magnitude of the voltage or current. The digital output may use different coding schemes, such as binary, Gray code or two's complement binary.

Signals in the real world, such as light and sound, are analog in nature and have to be converted into digital, using a circuit called ADC, before they can be manipulated by digital equipment. E.g. when a picture is scanned, the scanner does an analog-to-digital conversion. It takes the analog information provided by the picture (light) and converts it to digital.

Conversion of digital-to-analog is done for a variety of reasons. One reason is noise. Since analog signals can assume any value, noise is interpreted as being part of the original signal. On the other hand, digital systems can understand only zeroes and ones. Anything different is discarded. Another advantage of digital system against analog is the data compression capability. Since the digital counterpart of an analog signal is just numbers, these numbers can be compressed easily to save storage space or bandwidth.

In the figure below, it is assumed that the analog signal shown is an audio signal. The “y” axis represents voltage while the “x” axis represents time.

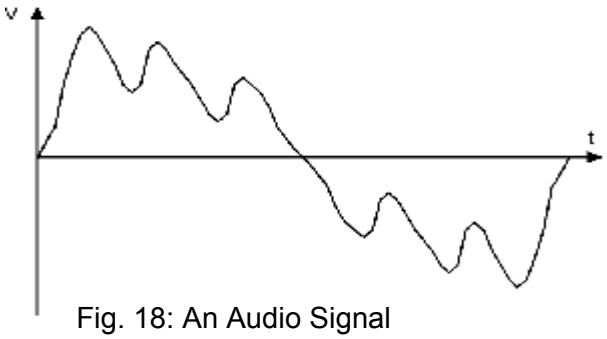

Fig. 18: An Audio Signal

The ADC circuit takes samples from the analog signal from time to time. Each sample is converted into a number, based on its voltage level. The figure below shows an example of some sampling points on the analog signal. [3]

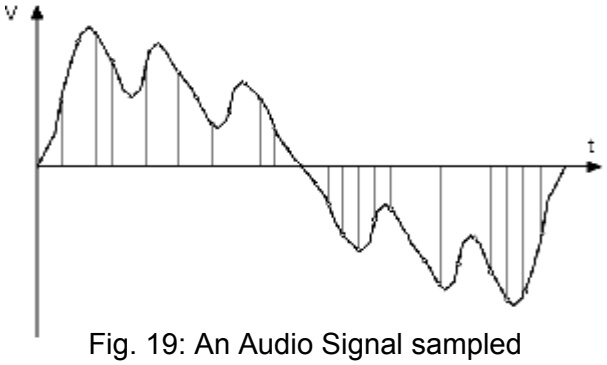

Fig. 19: An Audio Signal sampled

The frequency at which the sampling is performed is called the sampling rate. E.g. if a sampling rate of 22,050 Hz is used, it means that in one second, 22,050 points will be sampled. Thus, the distance of each sampling point will be of 1/22,050 second (45.35 μs). The higher the sampling rate, the more perfect is the output quality but a lot of storage space is required. Quality deteriorates if a lower sampling rate is used. The balance between storage space and quality is determined by the Nyquist Theorem. The theorem states that the sampling rate on analog-to-digital conversions must be at least two times the value of the highest frequency to be captured. E.g. since the human ear listens too sounds up to the frequency 20kHz, for music, a sampling rate of at least 40,000 Hz is required. For our application the highest signal frequency would be about 100Hz, so that the minimum sampling frequency would be 200Hz. In practice we can achieve a much higher sampling frequency using modern day computers, so this limitation will not be of concern in this application.

The value of each sampled point is stored on a fixed-length variable. If the variable uses eight bits, this means it can hold values from 0 to 255 (2^8=256). If this variable uses 16 bits, this means it can hold values from 0 to 65,535 (2^16=65,536). So, if, e.g. an 8-bit analog-to-digital converter is used, the lowest value is zero and the highest value is 255.

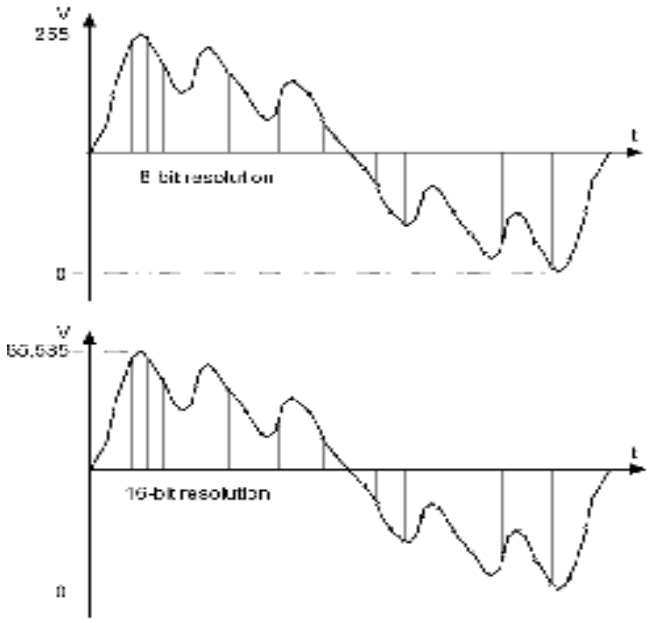

Fig. 20: An Audio Signal Being Converted to a Digital Signal

ADC divides the “y” axis into “n” possible parts between maximum and minimum values of the original analog signal, and this “n” is given by the variable size. If the variable size is too small, two sampling points close to each other will have the same digital representation, thus not corresponding exactly to the original value found on the original analog signal and resulting in a poor quality output signal. One of the ways to know the necessary number of bits for an ADC is by calculating the desired noise level. Since the values sampled from the original analog signal will be “rounded” several times to the nearest possible digital equivalent, quantization noise is produced. The signal-to-noise ratio (SNR), which measures the noise level, can be easily calculated using the following formula: [4]

SNR = 6.02 x n + 1.76 dB, where n is the number of bits used on the ADC.

The higher the SNR, the better it is. An 8-bit ADC provides a SNR of 49.9 dB, while a 16-bit ADC provides a SNR of 98 dB (which is a virtually no-noise value).
The data obtained from the analog-to-digital conversion is better known as PCM (Pulse Code Modulation).

The following figure shows an analog-to-digital converter:

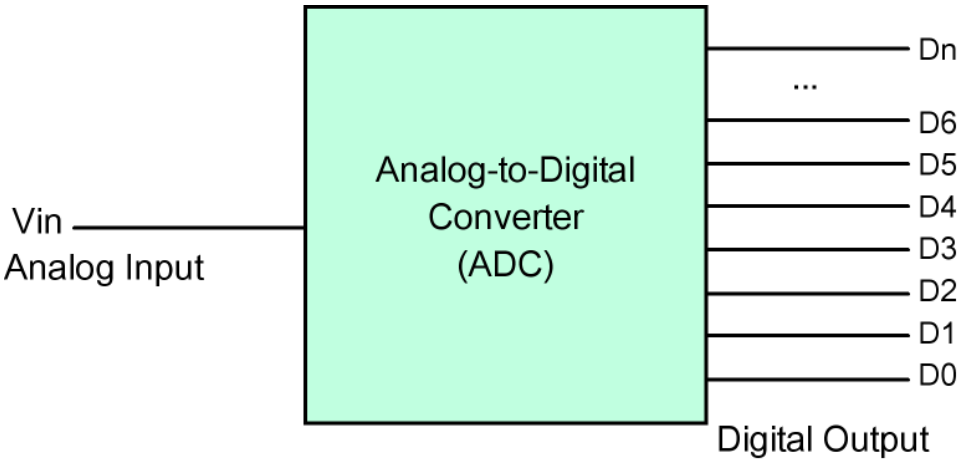

Fig. 21: Analog-to-Digital Conversion

There are several ways to build an ADC. We can divide ADC design into four main groups:

- Parallel design (also known as Flash ADC)
- Digital-to-Analog Converter-based design (e.g. ramp counter, successive approximation, tracking)
- Integrator-based design (e.g. single-slope, dual-slope)
- Sigma-delta design (also known as delta-sigma, 1-bit ADC or oversampling ADC).

Each one of these main groups can have several different implementations.
The IC to be used for analog-to-digital conversion in our project is ADC0820. The ADC0820 is an 8-bit CMOS A/D which uses a half-flash conversion technique and offers a minimum of 1.5 μs conversion time and dissipates only 75mW of power. The half-flash technique consists of 32 comparators for two halves, a most significant 4-bit ADC and a least significant 4-bit ADC. The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100mV/μs.[16]

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/0 port without the need for external interfacing logic. The ADC0820 costs about $2, so it is quite cheap.
The key specifications are:

- Resolution: 8 bits
- Conversion Time: 2.5 μs Max (RD Mode), 1.5μs Max (WR-RD Mode)
- Low Power: 75mW Max
- Total Unadjusted Error: +/- 0.5 LSB and+/- 1 LSB

- Temperature Range: 0^o Celsius to $+70^o$ Celsius[6]

Pin Configuration of ADC0820 (Top View)

Dual-In-Line, Small Outline and SSOP Packages:

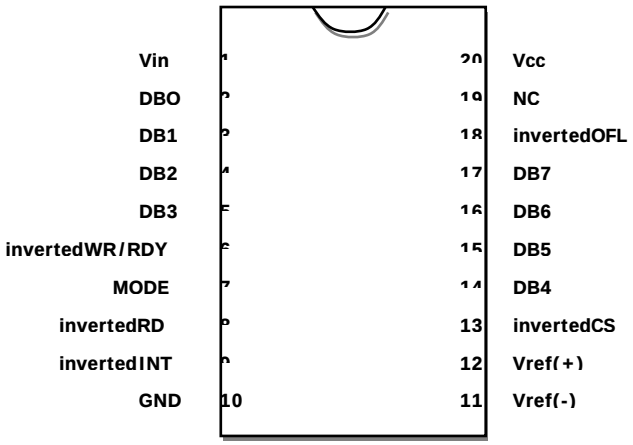

Fig. 22: ADC0820 Pin Configuration

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. They are suitable for applications requiring very large bandwidths. However, flash converters are known to consume a lot of power, have relatively low resolution and can be quite expensive. This usually limits them to high frequency applications that typically cannot be addressed in any other way. However, in our case, the ADC0820 uses two four-bit flash converters[7] as mentioned above. So, the problems of excessive power consumption and high cost are overcome quite easily and the ADC0820 delivers optimum cost and performance.

Flash ADCs are made by cascading high-speed comparators. Each comparator represents 1 LSB, and the output code can be determined in one compare cycle. The figure below shows a typical flash ADC block diagram. For an “N” bit converter, the circuit employs 2^N-1 comparators. A resistive divider with 2^N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a “1” when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is “0”. Thus, if the analog input is between V_{X4} and V_{X5}, comparators X_1 through X_4 produce “1”s and the remaining comparators produce”0”. The point where the code changes from ones to zeros is the point where the input signal becomes smaller than the respective comparator reference voltage levels[7].

A typical Flash ADC:

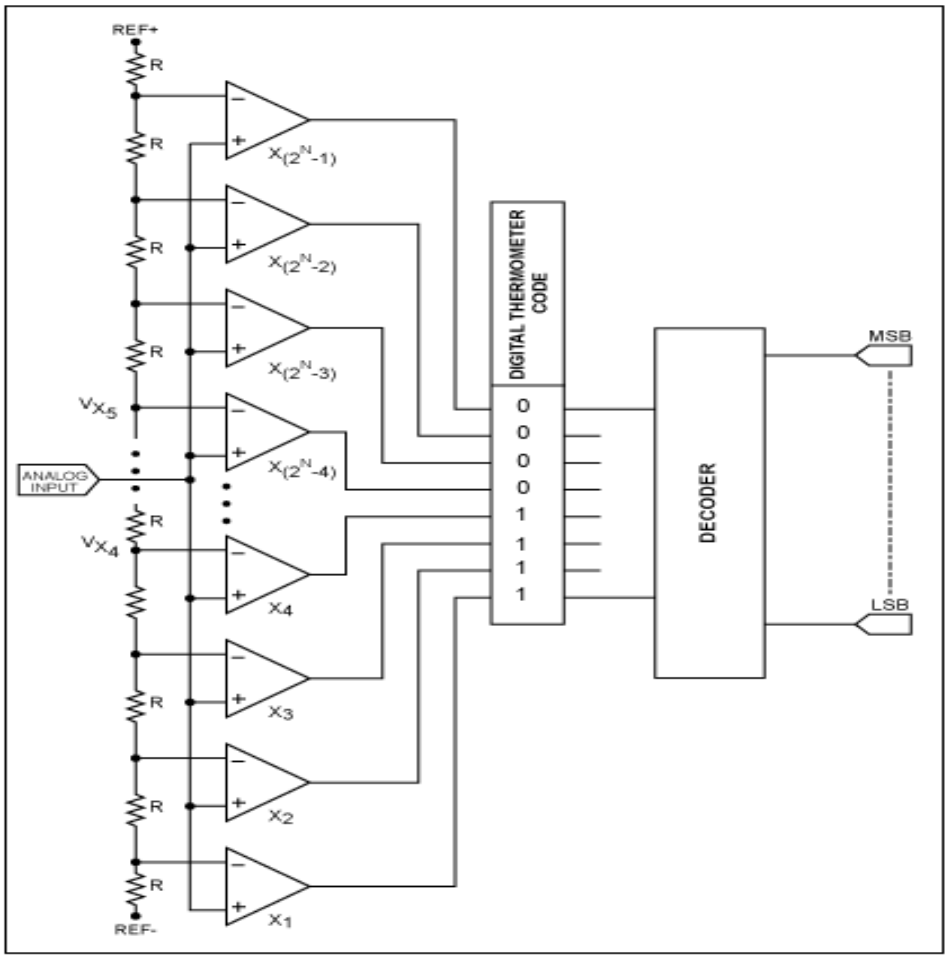

Fig. 23: A Typical Flash ADC

Interfacing through the parallel printer port:

A printer port is a special hardware circuit within the PC which has a few memory bytes (called registers) that take up address space within the main memory array of the PC. These memory bytes have one special quality to link with the outside world. To control any external circuit or to interact with the outside world for sending data we can either put values or binary numbers into some of these memory bytes from within the computer. In fact this is the way data is sent to the printer for printing. Again binary numbers (through one of two voltage levels) can also be placed into these memory locations from outside, which can then be read by the computer and stored in more conveniently placed memory locations for further processing. This latter procedure is called ‘data acquisition’.
In a typical IBM compatible PC, the standard printer port has the following three memory registers:

1. Data Register (DR) with address at decimal 888 (hexadecimal 378),
2. Status Register (SR) with address at decimal 889 (hexadecimal 379)
3. Control Register (CR) with address at decimal 890 (hexadecimal 37A)

Connections are brought out through the printer connector (25 pin D socket) only for the 8 DR bits (D0 - D7), 5 SR bits (S3-S7) and 4 CR bits (C0-C3) as shown in Table-1 where the respective pin numbers are also given. The last column indicates that for some of the bits, a software ‘1’ corresponds to ‘low or 0V’ and a software ‘0’ corresponds to ‘high or 5V’ at the terminals.

In the Standard Printer Port (SPP) mode all the DR connections are for taking data out from the computer, they cannot be used for data input, as this was the natural requirement for a printer. Only the 5 links to SR can be used as inputs. The 4 CR bits are mainly outputs, but can be used as inputs through special circuit techniques. However, in the recent IBM compatibles, an Enhanced Printer Port (EPP) option has been provided which allows data input through all the 8 bits of the DR. Of course it needs an additional step in the software; we need to place a '1' in the 6th bit of CR (C5, counting bits from C0) before giving an input command through DR.

Pin Assignments of the D-Type 25 pin Parallel Port Connector, and relevant register bits				
Pin No (25 pin D-conn)	**Direction In/out**	**Register**	**Register bit no.**	**Hardware Inversion**
1	In/Out	Control	C0	Yes
2	Out	Data	D0	
3	Out	Data	D1	
4	Out	Data	D2	
5	Out	Data	D3	
6	Out	Data	D4	
7	Out	Data	D5	
8	Out	Data	D6	
9	Out	Data	D7	
10	In	Status	S6	
11	In	Status	S7	Yes
12	In	Status	S5	
13	In	Status	S4	
14	In/Out	Control	C1	Yes
15	In	Status	S3	
16	In/Out	Control	C2	
17	In/Out	Control	C3	Yes
18 - 25	Gnd			

Design of Computer interface based on ADC0820

We used a design already worked out and tested by the supervisor of this project earlier. However, we retested its workings and made up our own circuitry for the present work. The detailed circuit design is given below.

In our project, we will be dealing with the middle and slow responses of Audio Evoked Responses (AER), also known as Slow Vertex Response (SVR). This signal is an analogue electrical one, coming from the patient's brain after the trigger audio pulses are given from the click generator. After necessary amplification and signal conditioning we present this signal to the input of the ADC as described before.

Handshaking of the ADC

The 8 bit ADC0820 has an analog input line, 8 digital data output lines, and a few control lines for 'handshaking' with the computer. 'Handshaking is a term used to indicate the process of proper interaction between the two devices in this case. We have chosen a particular mode for handshaking of this IC named the RD mode by connecting pin 7 to ground. When it is desired to acquire a data sample, the RD control input at pin 8 should be made low, which is maintained high normally. Several actions take place through this almost instantaneously, i) it takes a sample of the input voltage at that moment, ii) holds it for a brief period, iii) converts it to the corresponding digital value, iv) places it at the tristate output buffer, and v) delivers the 8 bit digital data onto the output data bus connected to the computer by enabling the tristate output buffer. RD input of the ADC is controlled from an output bit (C_0 in our case) of the CR of the computer printer port on software command. At the appropriate level, 0 or 1, the ADC takes a sample of the analogue input voltage and starts the conversion process. This conversion may take a few μs. During the conversion process the ADC can give out a 'busy' signal (0 or 1) which can be linked to one of the input lines of the printer port. The computer may use this information for waiting till the conversion is complete. However, we did not use any such connection since our signals are slow and we allowed enough time for conversion to be completed after the RD command is given. After such a delay, we read the 8 bit data through the DR to a particular memory location of the computer. This completes the acquisition of a byte of data.

We have planned to take 50 to 100 sweeps of data which will be stored in 50 or 100 such memory arrays. When the data acquisition is complete, corresponding values of data samples in all the arrays will be averaged and stored in another memory array. Thus signal averaging will be achieved simply through software. Each sweep of data will be initiated by a trigger coming from the click pulse generator, which has been connected to S4 bit of the Status Register (SR) at address 890.

Circuit diagram of computer interfaced ADC

The ADC circuit developed at the department of Biomedical Physics & Technology of Dhaka University and adapted for the present work is shown below.

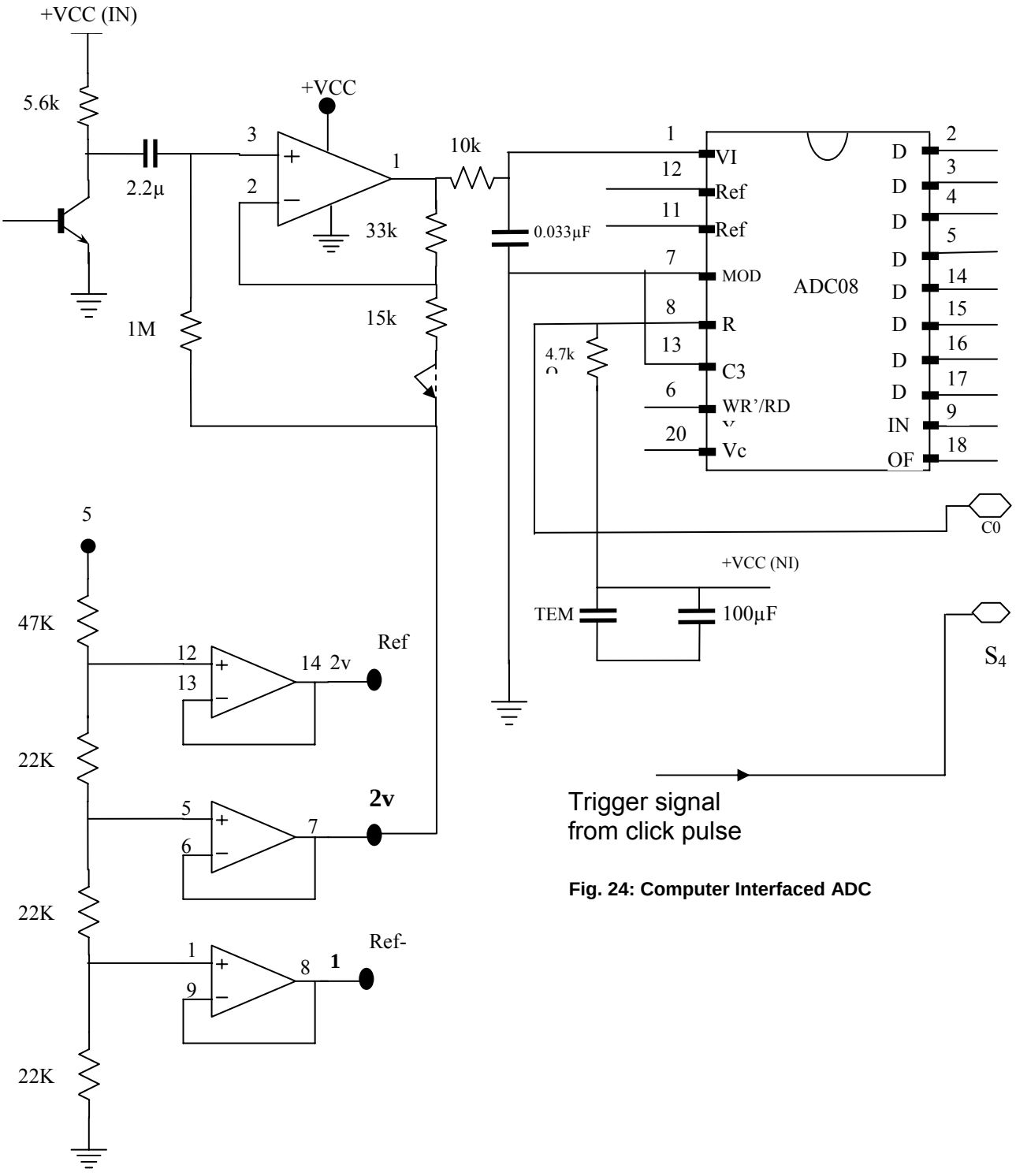

Fig. 24: Computer Interfaced ADC

2.5.6) DC references and level shifting

The ADC0820 chip runs on a single power rail between 0 and +5V. In the present design it was also set up so that input voltage between +1V and +3V are allowed for the ADC, +1V giving a digital 0 at the output (all binary outputs low), and +3V giving 255 (all binary outputs high). Therefore, the input ac voltage had to be level shifted to the mean value of +2V. This was achieved by producing three reference voltages : +1V, +2V and +3V using a potential divider and the three outputs were buffered using three unity gain buffer circuits as shown in the above circuit. The +1V and +3V were taken to the respective reference defining terminals of the ADC while the input op-amp circuitry were referenced to +2V instead of 0V as commonly used.

2.5.7) Software

Analog Data Acquisition

The interfacing was done through the printer port as mentioned above and a simple program was developed for basic data acquisition after getting a trigger signal from the click generator.

The programme have been given in QBASIC language in MSDOS operating system. We are using QBASIC language to develop software. For this we need a MSDOS operating system, un-interfered by WINDOWS operating system.

The software flow diagram of the process is shown in Figure 26 (for 50 sweeps). Firstly a counter-variable, n, is set to 0. The computer waits for the trigger signal through a program loop. The trigger in our design is taken from the bit S_4 of the Status register of the printer port, which is normally ‘0’ and becomes ‘1’ during the trigger pulse. If the trigger is not received, the program keeps waiting in a loop. When the trigger arrives, the program comes out of the loop and goes to the next data acquisition step. Here a loop is created to acquire many sweeps (typically, 50) of data for signal averaging. The main data acquisition part is another loop within the above loop. Here 1000 loops are made to acquire 1000 data samples which are stored in a variable array of 1000 elements, which is the current or raw data. Another array is created to store the sum of the current data and all previously collected data. To perform this all the elements of the sum-array is initially reset to ‘0’. When all the sweeps (here, taken as 50) of data are collected the program comes out of the loop. Then another array is created to obtain and store the average values of al the 1000 data points by dividing the sum values by the number of sweeps (here, 50), for which another program loop is used. Finally these averaged data points are suitably displayed using graphics commands.

The anaesthetist watches for the presence or absence of the AER potentials in the graphical output and takes a decision. A flow diagram of the developed

software is given below, which also includes the logical decision taken by the surgeon.

Software flow diagram (including logical decision making of the surgeon):

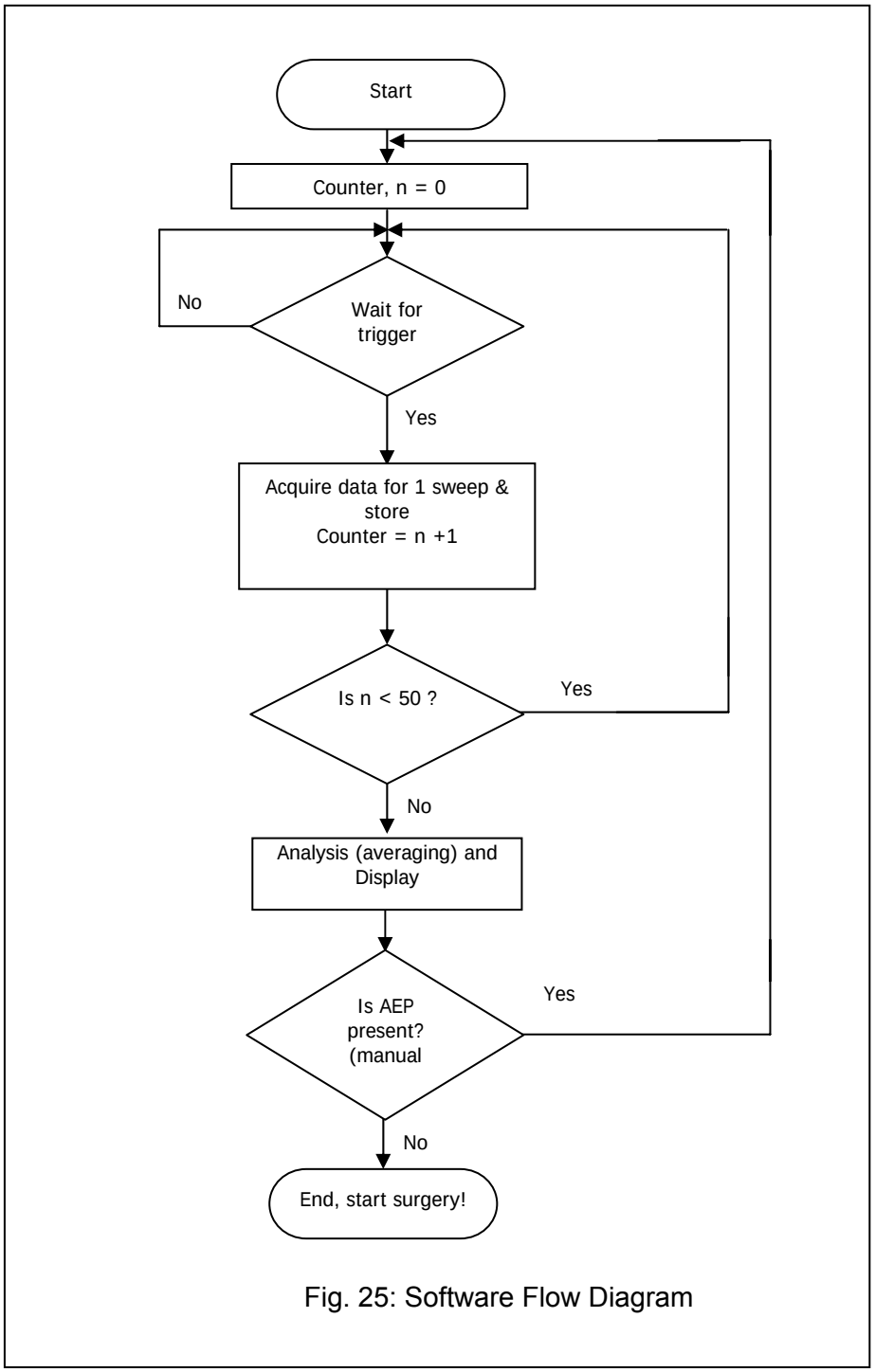

Fig. 25: Software Flow Diagram

Programming for simple data acquisition

Due to time limitation the full programming suggested above could not be developed. However a simple data acquisition software which collects a batch of 500 data points was written and tested, and is given below.

```
        DIM Y (1000), Sum Y (1000), AVY (1000)    [Reserves 1000 memory locations
in an array for y]
        SCREEN 12              [Makes a graphic screen with resolution 640 x 480]
        FOR i=0 TO 999
        SUM Y(i)=0                 [Initialize array to zero ]
        NEXT
        FOR j=0 TO 49                        [Loop for signal averaging (here for 50
sweeps)]
        PRINT "Waiting for Trigger"
        10Y= INP (888)                 [Looks for trigger from click generator]
        Z = Y AND 16
        IF Z=0 THEN 10
        PRINT "Got trigger"                [For monitoring during development]
        PRINT Z
        FOR i= 0 TO 999
        OUT 890, 32              [Keep data direction inward]
        OUT 890, 33              [Maintains data direction inward, pulls RD input low
to sample input data,                convert it to digital value, and make it available
through 8 bit data bus]
        Y(i) = INP (888)          [Read data from DR and store in array element Y(i)]
        NEXT i
        FOR i = 0 TO 999
        SUM Y(i)= SUMY(i) + Y(i)
        NEXT i
        NEXT j
        CLS                              [clears screen]
         LINE (0,100)-(500,300), 7, BF
        PSET (0,200)                  [Line position]
        FOR I = 0 TO 999
        AVY(i)= SUMY(i)/5
        COLOR 1
        LINE –(i/2, AVY(i)/2 + 125)       [To make 500 points horizontal (within 640
points
                                                in this graphics mode)]
         NEXT
        END
```

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[2] http://en.wikipedia.org/wiki/Operational_amplifier
[3] http://en.wikipedia.org/wiki/DC_offset
[4] http://en.wikipedia.org/wiki/Signal-to-noise_ratio
[5] http://en.wikipedia.org/wiki/Drift
[6] http://en.wikipedia.org/wiki/Instrumentation_amplifier
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4. Discussions and future work

The aim of the present work was to develop an anesthesia monitoring system based on Audio Evoked Response (AER). The system is quite complex and normally such a project cannot be undertaken and completed within the time available in an undergraduate project. However, the objective was to initiate the project and develop as much as possible within the limited time frame. The expertise and facilities available at Dhaka University allowed taking up of such an ambitious and complex project.

Firstly literature survey was performed to understand the various aspects of anesthesia monitoring and that of AER. Then an overall design for the AER system was made by studying the requirements of necessary functions. Then each individual segment was designed in detail based on the availability of electronic components locally. Each of these individual circuitry was first developed on breadboard and studied in detail. This allowed some in-depth understanding of the workings of these segments and of the circuitry. When the circuit on breadboard performed satisfactorily the components were mounted on a copper stripboard and soldered. These would form part of the final instrument. This aspect of the work needed learning of new skills which are very much essential for the training of an engineer towards making of finished instruments.

In the above mentioned way the hardware of our entire system has been built. The main four components of our system, i.e. the Click Generator, the Front-End Amplifier, the Electrical Isolation unit and the Computer-interfaced ADC have all been built and tested separately. The components are working quite well and according to our requirements. Moreover, the software has been written and tested. The outcome of software testing has been very satisfactory. Some of the segments of the system were then joined together including the isolated and non-isolated segments and tested. The results were very much satisfactory.

However, due to time constraints, the system could not be tested on a human subject. This would require mounting of the parts, particularly of the front end, in shielded enclosures and connections taken to the other parts using shielded cables. Due to the extremely sensitive nature of these systems and the fact that the system will be used in a hospital environment (with many other machinery near it) on patients, the system needs further modifications in terms of design and noise reduction. The software developed is just the bare basics, which will need to be developed further to calibrate the waveforms, and to have user friendly controls, keeping in mind that the end users would be clinicians in an emergency situation in a surgical operation theatre.
When the instrumentation part is complete and tested, it would be used to record AER from normal human subjects to see if further improvements are necessary. Then it would be tested on anesthetized patients in a hospital to

look for its usability. Furthermore, modifications probably need to be done according to requirements after such rigorous testing, both in hardware and software.

Looking back over the whole exercise carried out through the project period, it has given us the confidence of building up of a sophisticated instruments such as the AER system. When done, this will go a great way in relieving a large number of patients going through severe trauma because of faulty anesthasia administration.