WIRELESS INTERCONNECT FOR FUTURE ULSI

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The thesis title **"WIRELESS INTERCONNET FOR FUTURE ULSI"** submitted by Fahmida Sultana(ID:12121035), Samiha Sultana (ID:13321085), Maria Sultana (ID :13321082) Session:2015-2016 has been accepted as satisfactory in partial fulfillment of the requirements for the degree of bachelor of science in Electrical and Electronics Engineering .

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Abstract

In this age of compressed CMOS technology, due to stringent systems requirements in power, performance, and fundamental physical limitations, future ULSI systems are relying more on ultra-high data rates, scalable, re-configurable highly compact and reliable inter-connect fabric. To suppress these fundamental limits a RF/Wireless inter-connect concept is proposed for future inter/ intra chip communications. The RF/Wireless inter-connect is based on low loss and dispersion free microwave signal transmission using near field capacitive coupling with multiple access. Recent advances in wireless interconnect in different potential applications will be reviewed. Based on these developments and on the basis of the reviews future inter/ intra ULSI interconnect system will be proposed and analyzed in this thesis project.

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We would like to thanks our family who has been extremely supportive throughout the time we have been working on our thesis.

Declaration

It is declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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List of Acronyms:

- **CMPS= chip multiprocessor**
- **3 D= Three dimensional**
- **3D Chip Stack**
- **DSM= Deep Submicron**
- **Micro Bump technology**
- **NIC= Network in chip**
- **PCB= printed circuit board**
- **3D NOC= Network on chip**
- **RF= Radio Frequency**
- **SIPS= System in chips**
- **SOCS= System on chips**
- **TSV= Through Silicon Via**
- **HFSS=High Frequency Structure Simulator**
- **CST=Computer simulation Technology**
- **SRF=Self Resonant Frequency**

- **CMOS=Complementary MOSFET**
- **EMC=Electromagnetic compatibility**
- **FEM=Finite Element Method**

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Dedicated to our Parents and Teachers

Chapter 1

Introduction

1.1 Introduction

The number of transistor counts in integrated circuit is increasing twice the rate every 1.5 years. In deep submicron level (DSM) VLSI technology, design of multiprocessor system on chip (MPSOC) is becoming complex due to the increasing number of component integration [7]. Because of technology advancement many layers of caches memories, devices are connected on a single chip. Rising challenge is how to effectively communicate between cores with less power dissipation to improve the device and chip performance [3]. The task of on chip interconnect architecture is to ensure that data streams are transmitted and received correctly into the device with minimum power dissipation and delays. Traditional copper interconnects are used in MPSOC for on chip interconnect. As interconnect are scaled down design complexity increases, so copper based electrical interconnect becomes a problem due to its restraint of power delays and bandwidth.

To cope up with the increasing performance requirement the interconnect technology went through various evolutions like 2D network, shared buses crossbar architecture. The scalable interconnect technology on which researchers are currently working is 3D NOCS (network on chip) an extended version of network on a chip that utilizes three dimensions. When 3D NOCS is applied to copper interconnection, it cannot be scaled down further as it increases gate and RC delays which degrade circuit performance. According to ITRS roadmap interconnect advance is the key to increase consistency and power [3].

To support future MPSOCS achieving high speed in a range of terabits/s and also to reduce power dissipation in SOCS and high speed SIPS (system in package), many potential changes

were proposed. Material solution includes introductory low K dielectric here the material of interconnect has evolved from aluminum to copper k<2, but these materialistic solutions are no more viable when we try to achieve the speed of terabit/s, and power dissipation of fempto joule/bit in DSM technology because of increasing RC and gate delays. The future interconnect

solution includes RF wireless, optical interconnect, and carbon nanotube. Ongoing research methodologies include RF wireless which we are going to discuss further. Other technologies like optical interconnect and carbon nanotube are still in their initial stages, and requires further development.

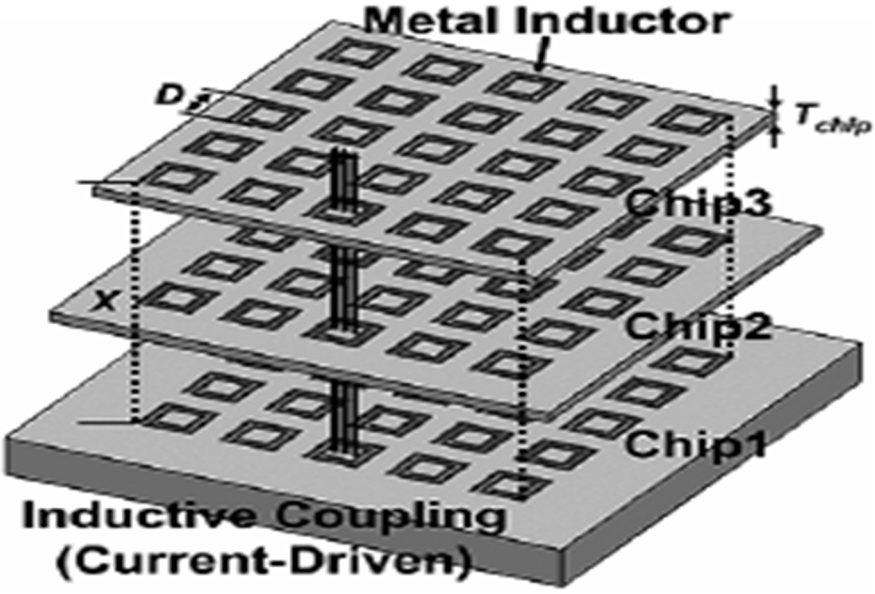

Figure 1.1:3D Stacked Inductive Inter-chip wireless Super connect

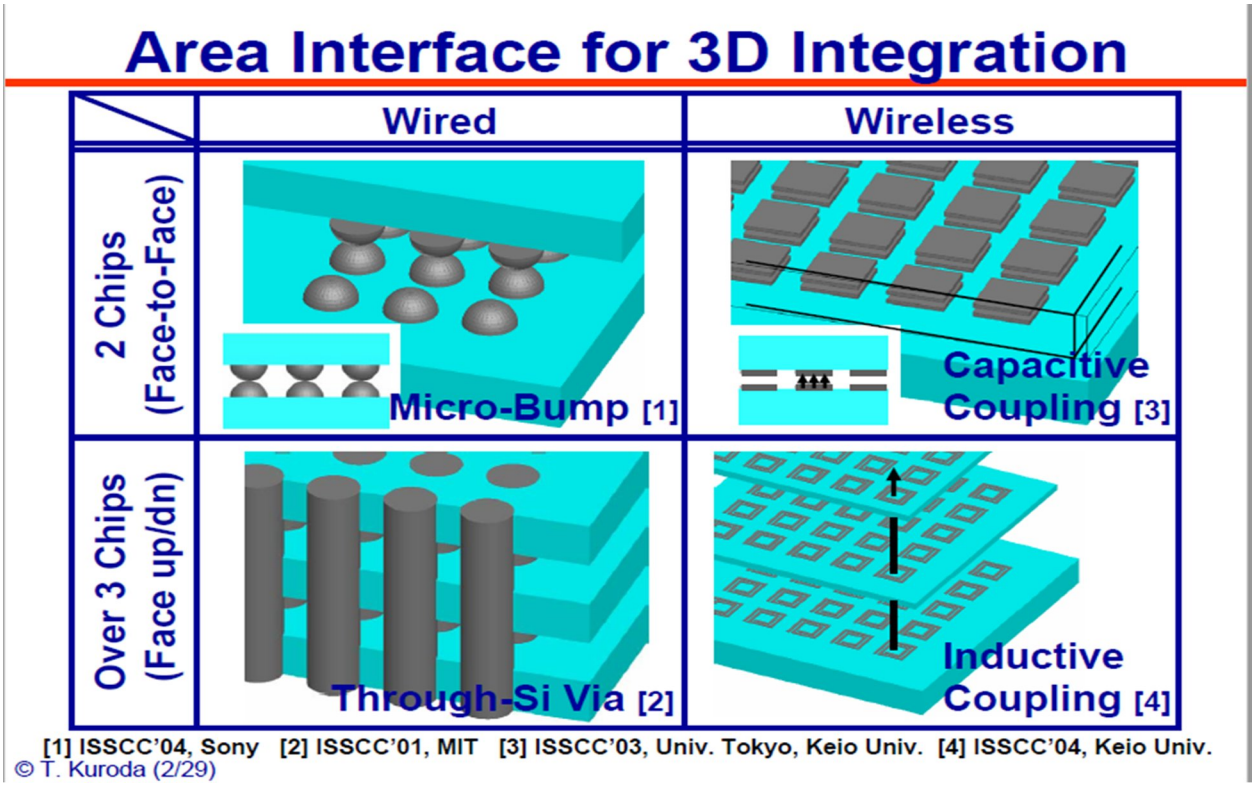

Figure 1.2:Interfacing Schemes for 2D and 3D Chip Stacks [16]

1.2 Background

Connecting different components of CMPS within a core in a scalable and efficient way become quite difficult as the number of cores in chip multiprocessors (CMPS) is increasing quickly [8]. In this paper [8] a network design for CMPS is implemented with 128 multithreaded cores, after implementation they concluded that (NOCS) network on the chip's major constraint is network latency. Another parameter that has been explored is the interconnect topology, from which they concluded that when system's area and power is increased Flattened Butterfly out performs Mesh and Fat tree [8]. For efficient large scale CMPS design interconnects must be studied with the hierarchy of memory caches [8]. The number of cores in CMPS design has to be amplified, to get better overall performance.

For connecting the large number of cores and chips in a scalable manner a new topology multi drop express channel (MECS) was proposed, which maintain a sense of balance between performance energy consumption and price [9]. MECS provides point to multipoint unidirectional links, which provides a high degree of connectivity with lower hop count and higher bisectional channel. According to this paper [9] in 64 terminals, network MECS has 9% latency advantage in low network latency [9]. Another proposed scheme includes, partitioning wires into multiple networks and channels. This plan has improved energy efficiency and bandwidth, but it degraded network performance and router density [9]. Lastly generalized express cube is introduced. Due to planer limitation generalized express cube is further mapped in to low dimension k cube. This method divides the baseline MECS channel into two, so it improves bandwidth employment, reduces headline block for shorter packets and improves latency factor for larger packets [9].

In (CMPS) network on chip (NOC) is the key technology for connecting multi-core processor and system on chip (SOCS), which are basic construction blocks for microprocessor and other embedded system [11]. Communication between components of CMPS is mounting design issues for multi-core system on chip [10]. Due to the technology scaling, traditional metal interconnects cannot be improved further, because it degrades system performance and increases gate delays. As a result, researchers came up with an alternative design, this includes 1)3D integration 2) nano photonic communication 3) wireless interconnect [10].

To ensure that power requirement of electronic device are kept in place with the semiconductor industry and ITRS roadmap, device and the communicating infrastructure, power levels are key factors, changes demand very high communication bandwidth [14].possible changes in communication infrastructure include, interconnect within 3D chip stack and intraconnect between 3D chip stack. These technologies achieves a data rate of 100Gbits /s [14]. Efficient communication link design becomes challenging for technology with high data rates. So the researchers designed a wireless link between boards (PCB), where each node is considered as a 3D chip stack, from which link budget, power dissipation and data speed can be calculated by different methods [14]. Moreover NICS technology used in 2D and 3D mesh was more efficient in terms of lower latency, high throughput, and to some extent helped to achieve future data rates [14].

Various existing input, output scheme of wireless super connect interface scheme includes (1) High speed link (Buffer or ESD pad PCB connection) (2) 3D MEMS (MEMS I/O) (3) system on chip (SOC) (4) Micro Bump technology based on micro bump I/O. Previous works include Ac coupled interconnect for high speed and high density packaging, this scheme has a number of advantages gained over mechanical structure [1] [12].

Ac coupled interconnect technology with buried solder bumps the method is implemented on MCM and MCM substrate. This technology provides high data rates and low I/O pitches less than 75um [12] [13]. Ac coupled interconnect is contactless technology, data rates can be achieved up to multi gigabits/s the average pin count of ICs also increased to satisfy ITRS roadmap prediction power/pin=10.0mW (70W for 7000pin) [1]. This technology also decreases the power consumption between chips to package [12]. For AC coupling signals are transmitted using contactless series capacitance or inductance [13]. For capacitive coupling buffers are required this increases the area occupied and the circuit complexity and increases power dissipation, but in inductive coupling I/O pitches can be reduced to 75um for impedance control. Buried solder bumps are used to provide DC power and ground over the same interface in AC interconnect technology [13]. Higher densities can be achieved with contactless technology without much mechanical complexity regarding I/O pitches.

Due to the high channel frequency and the number of wires in inter chip communication, signaling power thermal complexity and the power dissipation increases [5].These problems can be reduced by a method known as pulse signaling for capacitive coupling. Generally a capacitive coupled circuit without pulse signaling suffers from DC balancing issues that increase the circuit overhead power. When this technology is implemented over 10cm PCB lines it increased the channel bandwidth by 3dB of 2.94GHz [5]. This is only possible because device loading effect was reduced by decoupling the net parasitic capacitance from the I/O pin that has reduced the ESD structure. Thus CCBI pulse signaling is an excellent method for multi gigabit/s speed with low power, inter chip interface, it also reduces cross talks and L (?? ?? noise [5].

Transmission of digital signal directly over stacked adjacent chip layer is investigated with metal layers and TSV. However the vertical signaling method is analyzed using capacitive coupling between chip layers in 3D circuits this method improves speed, signal delay and power

dissipation [6]. Chip layers, stacking are thinned to about 1um-5um [6]. The vertical chip layers are interconnected by side wall metallization. For coupling capacitors the upper electrode is formed on the lowest layer of the top chip in SOI (silicon on insulator) and the lower electrode will be formed on the top most metallization layer of the lower chip to ensure small communication distance as better coupling between chip to chip an electric field will be set up between the insulating and adhesive layers [6]. This vertical transmission technology gains the advantage of larger integration density and higher bandwidth for three dimensional integrated circuits [6]. Another method of RF wireless for 3D stacked chips includes Inductive interchip wireless super connect.

Inductive coupling can be modeled by equivalent circuit and the parameters could be found using biot sarvert law [2]. Inductive coupling is used for long distance wireless communication, where chips are faced up and inductively coupled by metal inductors. Using the calculated values of equivalent circuit model and varying other parameters such as communication distance between two metal inductors, thickness/width of metal inductors, no of turns of metal inductors can be assorted. It is also possible to achieve a speed as high as È? ? ? ? ? É and reduce power dissipation up to È? ? ?*h*? ? ? ? ? [2].

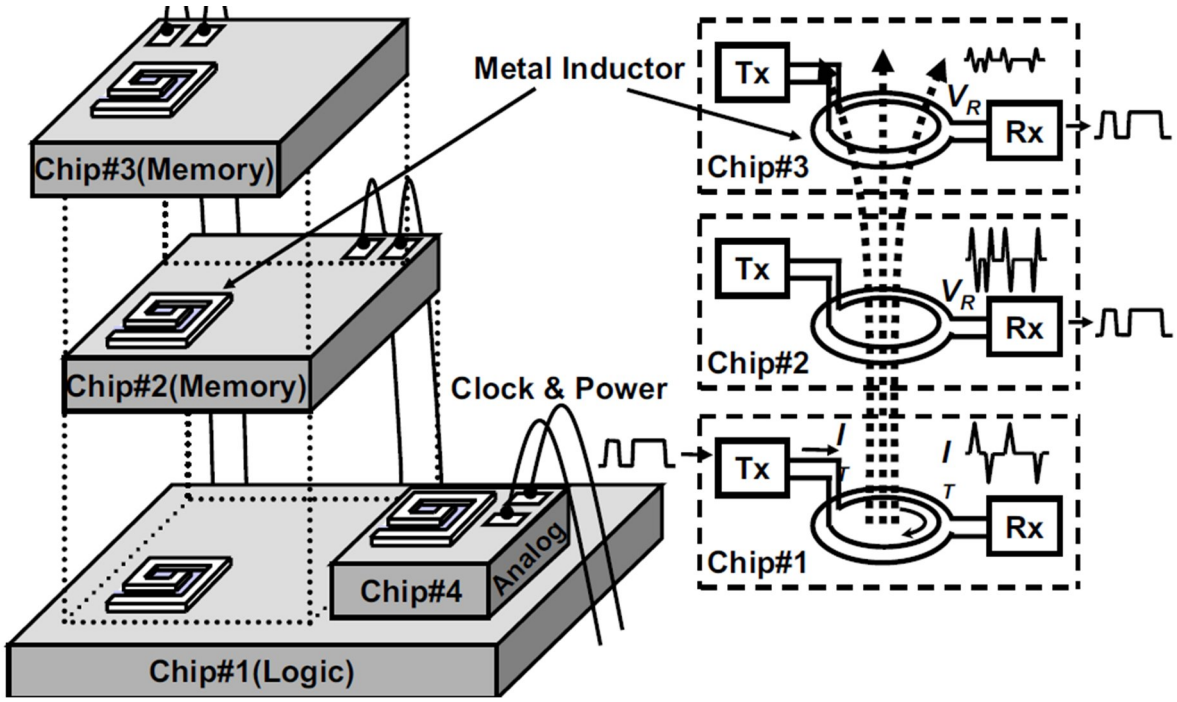

Figure 1.3: Wireless Superconnect Based on Inductive Interchip Signalling

1.3 OBJECTIVE:

From chip to chip communication, RF wireless is the emerging technology. The objective of our thesis is to analyze the gain of transmitter receiver made of metal inductors, by changing din R communication distance between two inductors and altering the number of turns. For this analysis we have used inductive coupling. We have presented our analysis with theoretical calculation and implemented it in HFSS software.

1.4 Thesis overview

This thesis paper on the design of inductors for inductive coupling, covers the entire portrayal of our work. We discussed the effect of changes in inductor parameters, on coupled data streams.

In chapter 1, we briefly discussed some ground works on the evolution of interconnect technology, both 2D and 3D NOC in CMPS and the objective of this thesis paper.

In chapter 2, various types of on-chip inter-connect technologies have been briefly described in the second chapter. Also, the merits and demerits of using them in inter-connect technologies comparing between them has been included in this chapter

In chapter 3, we discussed about the design of a spiral inductor on Ansoft HFSS software , and analyze the simulation results. Simulation of inductive coupling on CST software and the analysis of results is also discussed in this chapter.. Lastly, theoretical calculations are also observed in that chapter..

In chapter 4, the summary of this thesis paper is included along with future recommendation of our work.

Chapter two

Different methods of on-chip inter-connect technologies

2.1 Different methods of on-chip inter-connect technologies

On chip inter-connect technologies can be realized using the methods described below:

1. Wired interconnects

2. Optical inter-connects

3. RF/Wireless inter-connects

2.2 Wired Inter-connect

Copper wires are considered to be used in modern on-chip electrical interconnects. The usage of Local Inter-connect is seen for short distance communication with a delay of less than a clock cycle. Whereas, limited applications of global interconnects are seen for long distance communication, possessing a delay that spans multiple cycles. High RC constants of global inter-connects create greater propagation delay, Transition time and crosstalk noise. Even if the bandwidth is increased, it's not possible to fully ignore the delays in DSM technology. The propagation delay might be reduced to a certain limit. [4]

In DSM technologies delay, power and bandwidth are not satisfied up to the mark in case of copper based inter-connects. Again, parasitic resistance and capacitance of copper interconnects are increasing at a striking rate, due to enhanced gain boundary, surface scattering and also for highly resistive diffusion barrier layer which poses serious obstacle for inter-connect delay, reliability and power loss. [4]

Copper inter-connects are usually made of 70% of on-chip capacitance. So, new and innovative interconnect technologies should be introduced. For better performance, reliability and power requirements in long term inter-connects. Moreover, for high speed data rates (more than 100

Gbps/pin) and scalable interconnect technologies that is capable of handling hundreds of concurrent communication streams, the importance of introducing new inter-connect technologies are undeniable. [3]

2.3 Optical inter-connects

To overcome communication problems using electrical wires, we can resolve many issues using optical waveguides based on optical inter-connects. While board to board and chip to chip optical inter-connects have been proposed and are actively under development, feasibility of on-chip optical inter-connects is an open research problem. High speed, electrically driven, on-chip monolithic light source still remains to be realized. Laser source provides light to modulator in off-chip.[4]

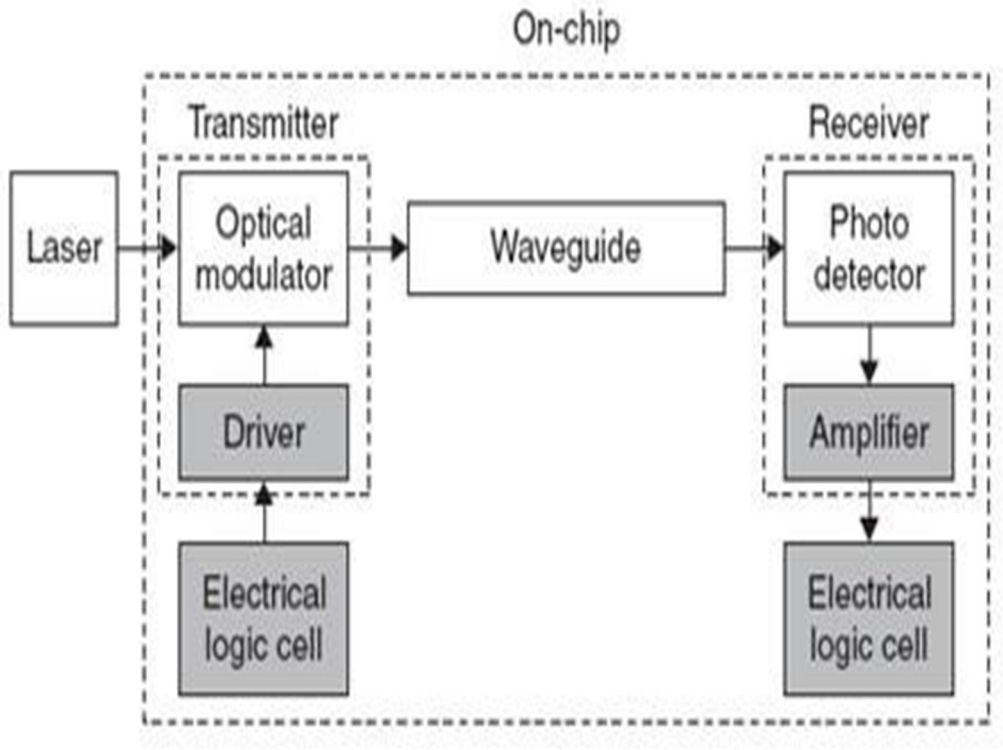

Figure 2.1: Optical Inter-connect Transmitter-Receiver model

Transmitter:

The electro optical modulator converts the data into a modulated optical signal that is supplied from electrical driver. Various high speed modulators have been proposed that change refractive index or absorption coefficient of an optical path when an electrical signal is injected. Again, some silicon modulators possess higher modulation speed, consume large power, has greater silicon footprint. In order to get smaller size, power diminution and lower modulation speed we might use micro-resonator based PI-N diode type modulators. [4]

The modulators capacitive load is driven by the modulator driver with many inverter stages.

Light is routed through the waveguide path. The bandwidth, latency and area of an optical interconnect is highly effected by the refractive index of the waveguide materials. In this case, Silicon and polymer can act as propitious replacements of the waveguide materials. [4]

Receiver:

We use receiver to convert the optical signal into an electrical signal. To compensate for the losses during this conversion the photo detector with greater value of quantum efficiency is used. Moreover, to convert the photo detector current into a threshold voltage, the trans-impedance amplifier stage is applied. [4]

As there are no RLC impedance present in optical inter-connect, it has a greater advantage of low signal propagation delay in waveguides. The inter-connect length is not responsible for the conversion delay. If only the waveguide propagation delay is higher than the overall delay, we'll get more delay advantages in optical inter-connects than the electrical. Higher bit rate through waveguides with a fixed pitch causes optical bandwidth density to increase. Wavelength division multiplexing (WDM) improves bandwidth density for optical interconnects over electrical interconnects which solves the problem that would've been caused by single wavelength optical interconnects. [4]

A few researches have described how on chip optical networks can be used for clock-tree networks. Researchers like Chen et al. [TED 2004] Ackland et al. [CICC 2005] argued on how an optical clock tree scales better than an Htree electrical clock network. loop network. [4]

Optical inter-connects have therefore, several advantages over copper based interconnects. Like-

*It supports huge essential data bandwidths using simple on-off modulation schemes.

*Free of crosstalk causing electrical interference.

*Transmission distance does not have much effect on the capacitance, inductance and power loss at the chip level.

*Easy routing and placement. [4]

Depending on the group velocity of the light in the waveguide, transmission latency is very small once the path is achieved.

There are many problems regarding optical inter-connects as well. For example-

*High efficiency of Transmitter and receiver is needed.

*Electro-optical modulators with high speed, minimal power and compact sized features are required.

*Integrated on-chip light source, polymer waveguide are also important issues that needs to be taken care of. [4]

Moreover, as optical inter-connect has high sensitivity towards temperature variations, temper management remains a big challenge. [4]

2.4 RF/Wireless Interconnects

Capacitive coupling:

Capacitive coupled is a wireless chip to chip communication technology that uses capacitive coupling to transfer signal from one chip to the neighboring chip. Wireless super-connect by capacitive coupling (WSC-C) has advantage in terms of power and speed and cost. In non-contact surface highly protective device (ESD) is removed to reduce power delays and area, for two stacked chips with in a distance of few microns. [5] Vertical integration signal processing

is used for two stacked integrated circuits. Two methods are used for vertical integration and signal transmission, Capacitive coupling (1)2D capacitive coupling (2)3D capacitive coupling. 2D integrated capacitive coupling has lower speed and bandwidth as limitation, compared to 3D integrated capacitive coupling. 3D capacitive coupling has lower transmission/propagation delay and reduced power dissipation. The propagation delay is dominated by, load capacitance (Cc).The benchmark for power dissipation considered is static power which varies with the channel length, in CMOS receiver circuits.[6] For convectional chip to chip communication by capacitive coupling includes high RC constant, also capacitive coupling for MEMS (metal chip metal) on a common substrate DIP package consume very high I/O power interface over limited bandwidth, to reduce this high overhead power dissipation, to reduce power dissipation a pulse signaling known capacitive pulse signaling method. This method proposes high speed, low power and low cost bus system method on PCB boards with MIM capacitors and WBGA package. Advantage of CCBI system is no DC balancing problem, no DC restoration and quantization feedback is required, it also reduces I/O interface power dissipation. The disadvantage of such a system is during loading effect at high frequency for any current/voltage driven interface shows a dominant loss in multi drop bus. Using CCBI with four WBGA packages the 3dB bandwidth can be improved for 2.94GHZ and 2.97GHZ. The maximum data rate or attainable could be up to 5Gb/s. [5]

Inductive coupling:

Inductive coupling is more preferable and efficient than capacitive coupling for longer distance inter-chip communications. The magnetic flux induced by such coupling is responsible behind its efficiency, as the flux can be detected hundreds of microns away.

Power and clock signals are given to multiple stacked chips by a bonding wire or inductive coupling, where the multiple chips are stacked face up and are coupled by metal spiral inductors for achieving the inductive effect. The current changes in the transmitter inductor because of the transition of the Transmitting data (Txdata), that produces a small voltage at the receiver inductors (Vr). This signal is then converted to digital signal as the receiving data(Rxdata). The equation of this small voltage can be given by,

?? =?√???? ___?? ????? ___??

K= a constant determined by distance and feature size of inductors.
nR(nT)= number of turns of the receiver (transmitter) inductors.

Device scaling is the reason behind greater efficiency of inductive coupling over capacitive coupling. From the above equation, we can state that, increasing the number of inductors results in the increase of Vr. Increment in the number of metal layers also increment the transmission gain. Only topmost layer is utilized in capacitive coupling. Another advantage is that it arises when low voltages are supplied in scaled devices. Again, in case of inductive coupling transmission power increases in current mode., whereas in the capacitive coupling it is limited by the supply voltages in voltage mode. It is important to remember that, as the permeability (μ) is almost the same where permittivity (ε) changes in the semiconductor devices, the reflection or the absorption is much smaller in inductive coupling.

The inductive coupling behaves overall as a bandpass filter as the transmitter (Tx) is considered to be corresponding to the second order low pass filter, the magnetic coupling to a differentiator and the Receiver (Rx) to first order low pass filter. The major frequency of Tx data is surrounded by the passband. It is expected that the inductive coupling tolerates noise from LSI circuits if its frequency is lower than the cutoff frequency (typically some hundreds of MHz), but it is protected from ambient noise by magnetic shielding in a package. A simple yet accurate model is developed by using Biot Savart's law to extract L and k from a layout. Calculations using the model very accurately agree with simulation using parameters extracted by FDTD (Finite Difference Time Domain) analysis.

The transmitter is implemented by an H-bridge circuit where IT flows for a period of delay (Transmit) by a delay buffer. The shorter the transmit, the smaller power dissipation in Tx, but the smaller timing margin to capture VR. With accurate timing control using DLL (Delay Locked Loop), Transmit is shortened. In the receiver VR is detected by a sense-amplifying flip-flop (SA-FF) which is activated by RX clk with appropriate timing and duration. If the rising edge of RX clk is too early or too late, Rx reads erroneously due to noise. The duration time, T Sense, should be long enough for detecting small VR. But if it is too long, Rx operates

erroneously because of noise when the same data continues in Non Return to Zero (NRZ) signaling.[2]

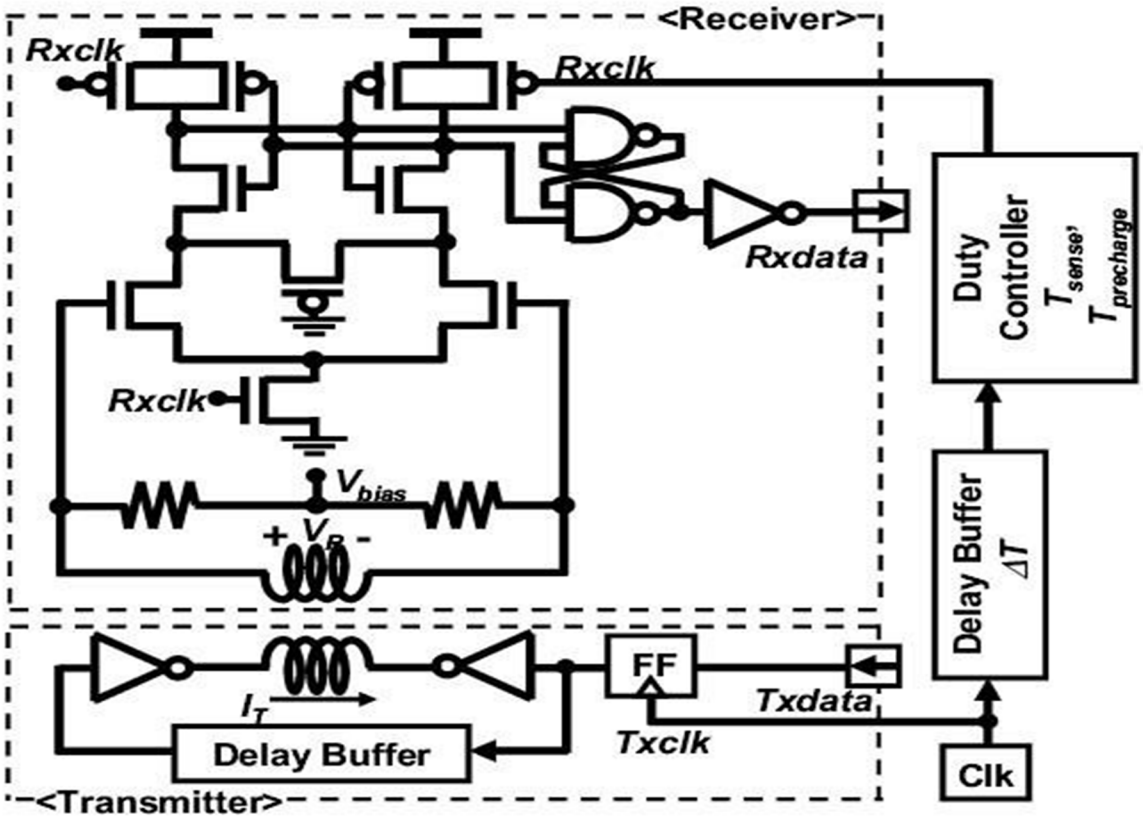

Figure 2.2: Wireless Inter-connect Transmitter-Receiver circuit design [1]

2.5 The reason of choosing inductive coupling for our analysis

From the above explanation, we see that traditional copper inter-connects have high resistivity, low reliability and susceptibility to electro-migration. So, it becomes harder for a copper wired inter-connect to satisfy design requirements like- delay, power, bandwidth. It is important to minimize these disadvantages in terms of power, speed and cost which can only be possible by wireless approaches or wireless inter-connects by capacitive or inductive coupling. As, wireless super-connect enables two chips to directly communicate through inductive or capacitive coupling, it provides high density, low power and high speed input-output communications. Again, it has more scopes and less disadvantages in case of transmitter and receiver components than the optical inter-connects. All these technologies have several issues that must be resolved before they can be adopted as on-chip inter-connect fabrics. But, considering the advantages of wireless super-connects over all other schemes and realizing better outcomes of this, we have set our objective to work on wireless inter-connects for inter and intra chip communications and continue further analysis based on that.

Chapter 3

Design and Analysis the Simulation Results

3.1 Introduction

In the chapter we will design single and multilayers inductors in 3D graphics environment and analyze the multi parameters, Quality factor, inductance of the on chip inductor by varying number of turns, width, length, radius, material properties such as bulk conductivity, substrate properties etc. For this a very organized process should be followed and a user friendly professional software is need to be used to have the most accurate simulations and results possible. We have chosen the ANSOFT HFSS software because it is very effective software for simulating 3-D, full-wave, electromagnetic fields with relatively more accurate results. We have also done some EM simulation in another software CST.

3.2 HFSS

The name HFSS stands for High Frequency structure simulator. HFSS is a high performance full wave electromagnetic (EM) field simulator for arbitrary 3D volumetric passive device modeling that takes advantage of the familiar Microsoft Windows graphical user interface. It integrates simulations, visualization, solid modeling and automation in an easy to learn where solutions of 3D EM problems are quickly and accurately obtained. HFSS employs the finite element method, adaptive meshing and brilliant graphics to give un parallel performance and insight to all 3D EM problems. HFSS can be used to calculate parameters such as S-Parameters, Resonant Frequency and fields. Typical uses includes:

Package Modeling – BGA, QFP, Flip-Chip

PCB Board Modeling-Power/Ground planes, Mesh Grid Grounds, Backplanes

Silicon/GaAs- Spiral inductors, transformer

EMC/EMI-Shield Enclosures, Coupling Near or far field Radiation

Antennas/Mobile Communications-Patches , dipoles , horns, Conformal Cell phone Antennas, Quadrafilar Helix, Specific absorption rate(SAR), Infinite arrays, Radar Cross Section(RCS), Frequency Selective Surfaces(FSS)

Connectors- Coax, SFP,/XFP, Backplane, transitions

Waveguide-Filters, Resonators, Transitions, Couplers

Filters- Cavity Filters, Micro strip, Dielectric

Using HFSS one can compute:

- Basic electromagnetic field quantities and for open boundary problems radiated near and far fields.
- Characteristic port impedances and propagation constant
- Generalized S-parameters and propagation constant
- The eigen mode or resonance of a structure

HFSS continues to lead the industry with innovations such as Modes-to-Nodes and Full-wave Spice. HFSS has evolved over a period of years with input from many users and industries. In industry, HFSS is the common tool of choice for high productivity, research, development and virtual prototyping

3.2.1 HFSS terms:

An Ansoft HFSS window has several optional panels:

- **A project Manager** which contains design tree which lists the structure of the project
- **A Message Manager** that allows viewing any errors or warning that occur before beginning a simulation.
- **A Property window** that displays and allows changing model parameters or attributes
- **A Progress Window** that displays solution process
- **A 3D Modeler** Window which contains the model and model tree for active design

3.2.2 HFSS Desktop

The HFSS desktop provides an intuitive, easy-to-use interface for developing passive RF device models. Creating designs, involves following:

1. Parametric Model Generation-creating the geometry, boundaries and Excitations
2. Analysis setup-defining solution setup and frequency sweeps
3. Results- Creating 2D reports and field plots
4. Solve loop-the solution process is fully automated

To Understand how the process co-exist, examine the illustration shown below:

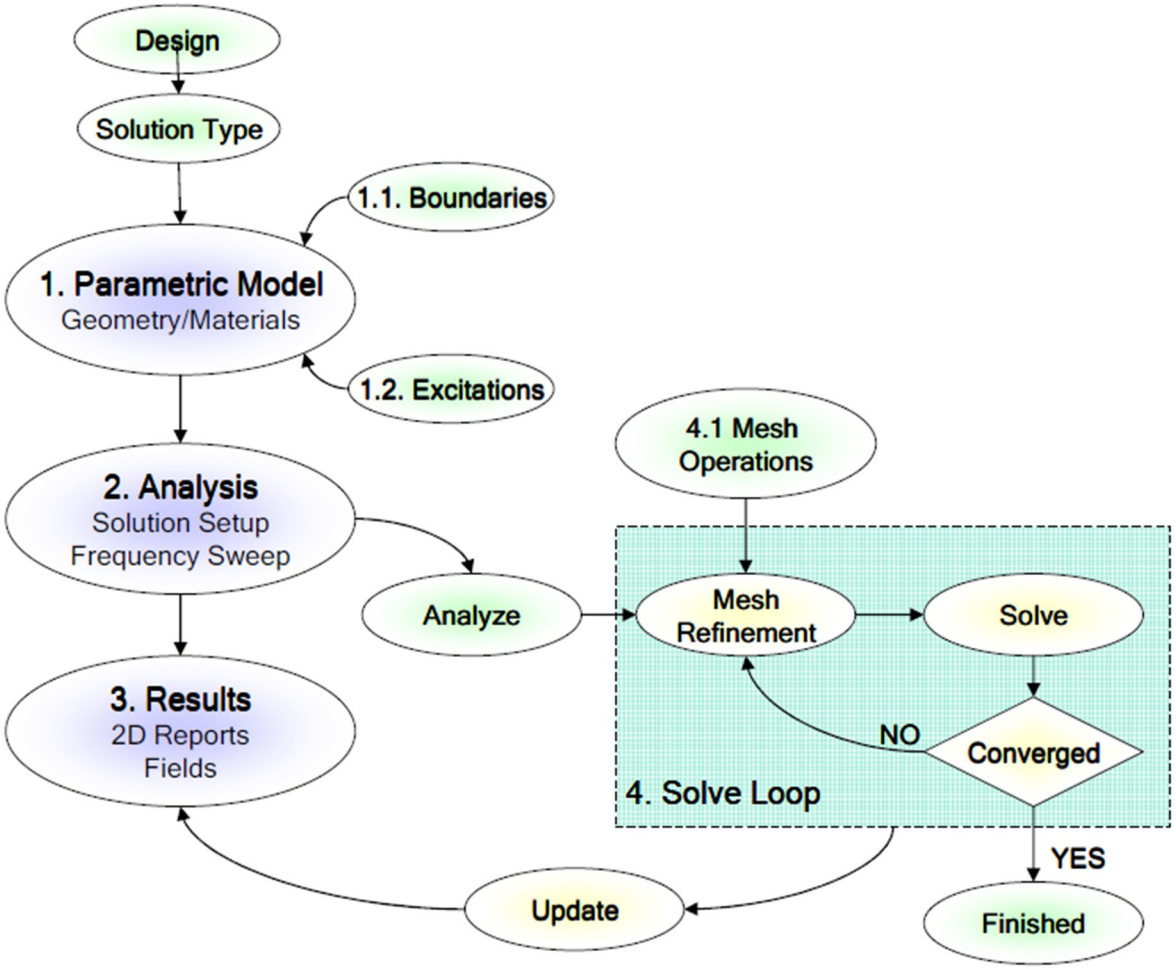

Figure 3.1: Flow chart of HFSS

3.3 Simulation Process:

The step by step the simulation process is discussed below

3.3.1 Drawing the Model:

The first step is to draw the model of the electromagnetic structure. The general strategy is to build the model as a collection of 3D objects. Each material type is selected as a separate object.

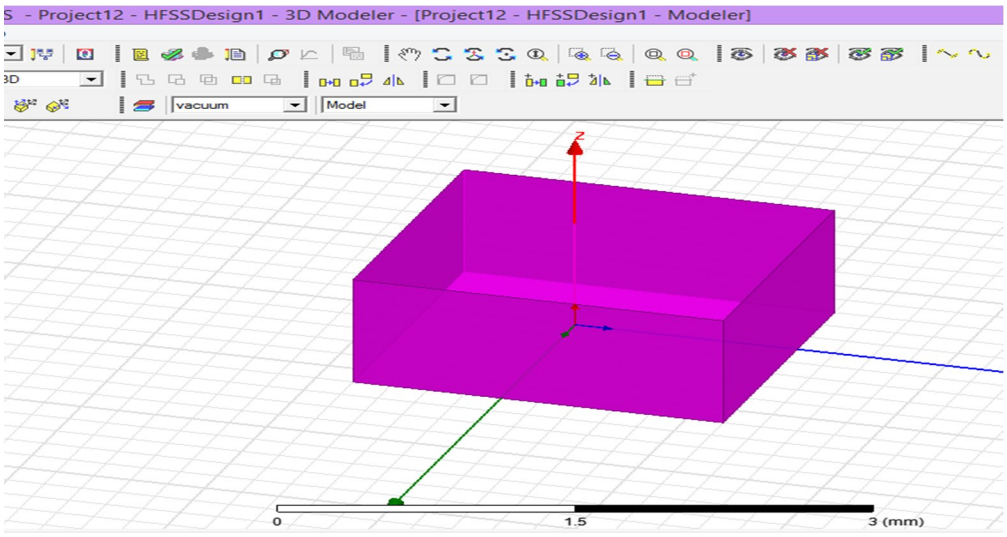

Figure 3.2: 3D modeler window

3.3.2 Assigning materials and their Properties:

It is necessary to define materials and Properties (i.e Conductivity and resistivity)

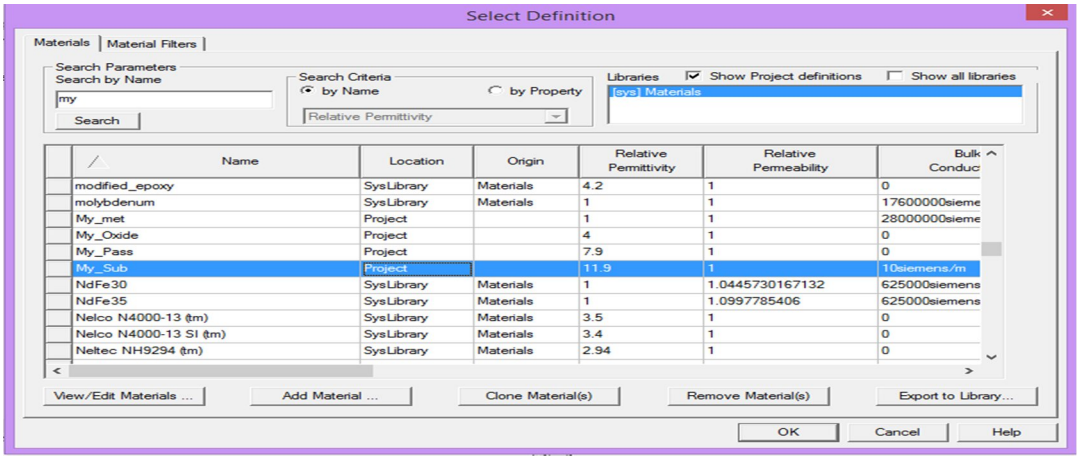

Figure: Edit material window

3.3.3 Assigning Boundaries

Boundaries conditions specify the field behavior at the edges of the problem region and the object interfaces. In this design perfect E is used which represents a perfectly conducting surface and radiation represents an open surface from which energy can radiate.

3.3.4 Assigning Excitations:

Excitations in HFSS are used to specify the sources of electromagnetic fields and charges, currents or voltages on objects or surfaces in the design. In this design Lumped port is used which represents an internal surface through which a signal enters or exists the geometry.

3.3.5 Modifying the Model view:

One can modify the view of contents in the 3D modeler window without changing their actual dimensions or positions.

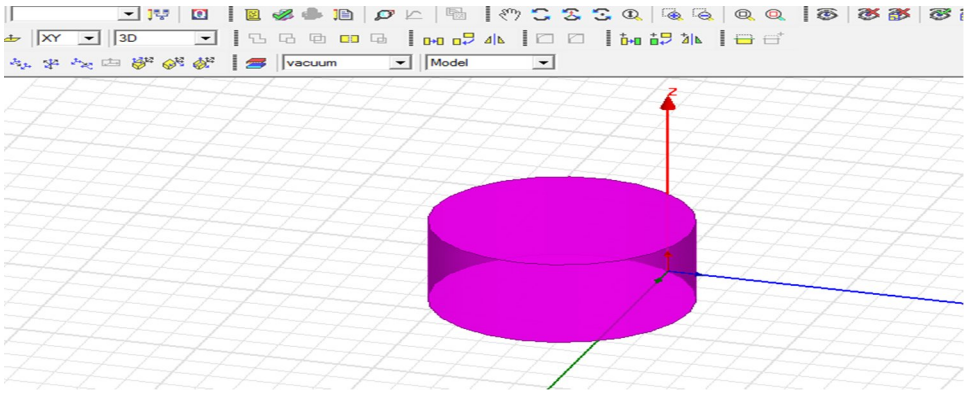

Figure 3.4: Modifying the view of model

We can also modify the model by changing its position or size:

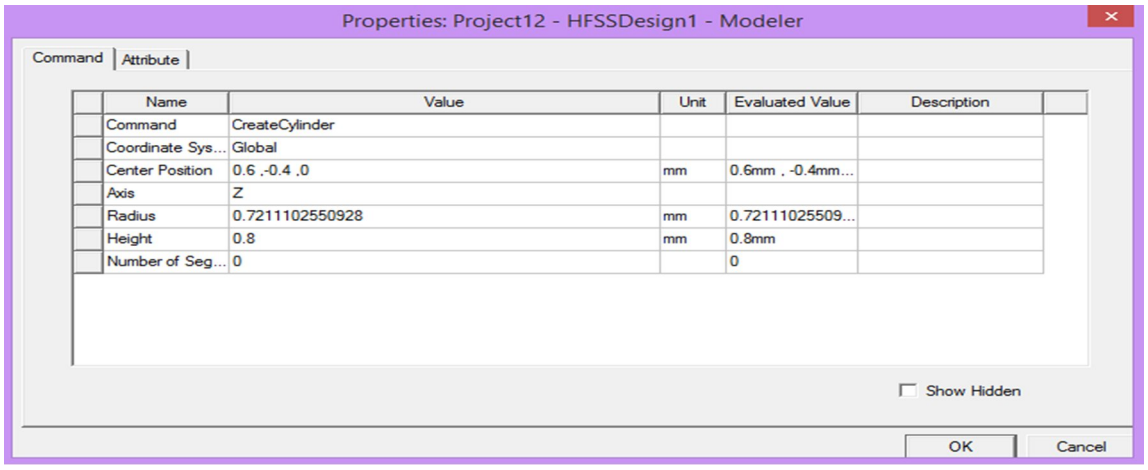

Figure 3.5 : Modifying the size of model

3.3.6 Specifying solution settings

Specify how HFSS will compute a solution by adding a solution setup to the design Each solution setup includes the general data about the solution's generation and frequency sweep parameters.

3.3.7 Validation check

It is necessary to check the validity where 3D model, Boundaries and excitations, Mesh operation, Analysis setup, Radiation are included.

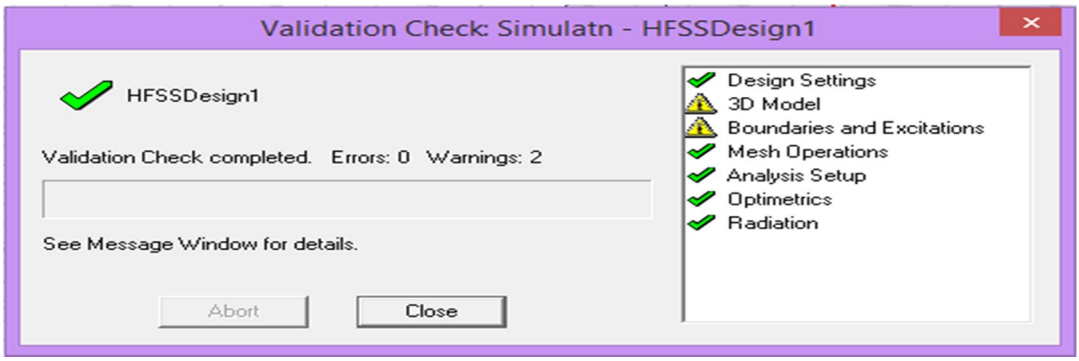

Figure 3.6:Validation Check window

3.3.8 Running Simulation

After all the above steps have been completed finally simulation program is run.

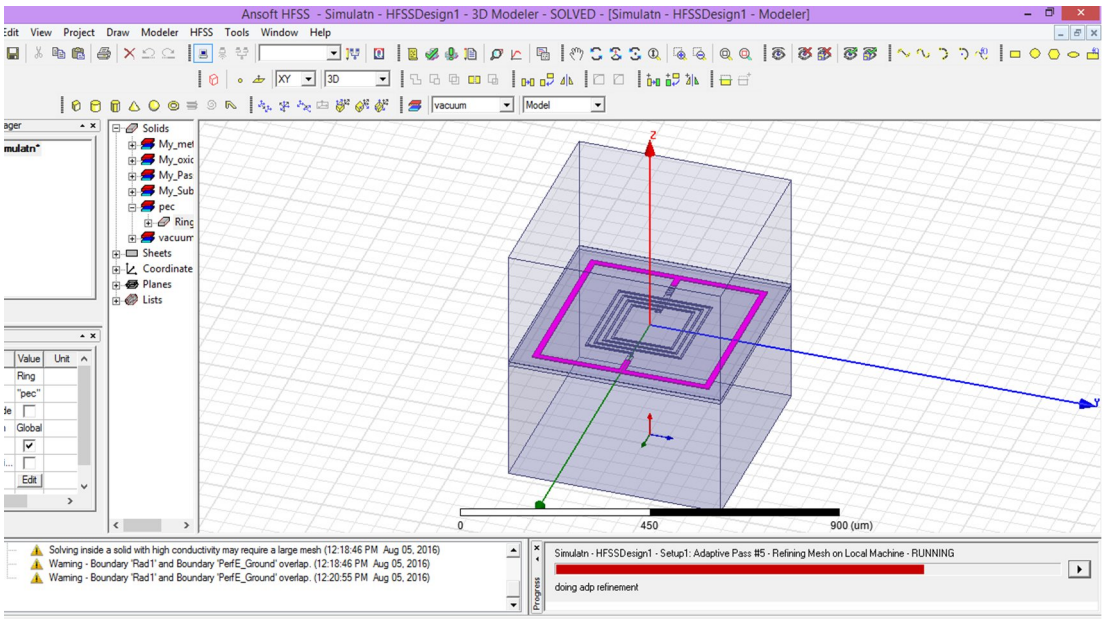

Figure 3.7: Simulating the Model

3.3.9 Generating Report

After HFSS has generated a solution, all of the results for the solutions are available for analysis. One of the two ways to analyze the solution details to create a 2D or 3D report or graphical representation that displays the relationship between a design's values and the corresponding analysis results. As example a S parameter vs frequency plot is below:

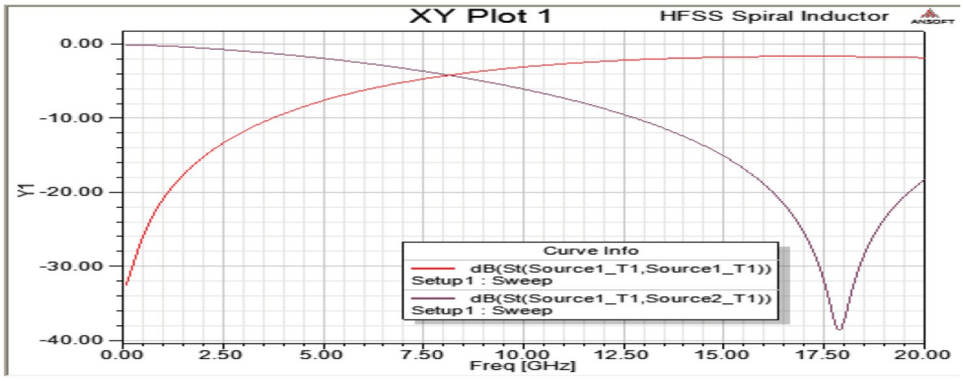

Figure 3.8 : S parameter vs Frequency plot

The simulation technique used to calculate the full 3D electromagnetic field inside a structure is based on the finite element method. Although its implementation is largely transparent, a general understanding of the method is useful in making the most effective uses of HFSS.

3.4 Design of on chip inductor

An inductor is formed by placing a spiral conductor between two ports in two different metal layers where two metal layers are insulated from each other. Here we implemented Si-substrate fabrication process. An oxide layer is implemented on silicon substrate. For further insulation a passivation layer is used. Two metal layer M1 and M2 are insulated from each other by oxide layer.

3.4.1 Design Specifications:

We have designed a single layer on chip spiral inductor with:

Number of turns: 4

Width: 5um

Bulk conductivity: 10(Substrate)

2.8e7(Spiral)

Height: 2 um

After that we have varied the number of turns, width, bulk conductivity and analysis the report and compared the quality factor, inductance, S parameter vs frequency graph. Then we have create a multi layer inductive coupling and analyze it with our analytical report.

3.4.2 Design segments, Materials, and their properties

Selection of the right material is a very important issue because the efficiency and loss factor of on chip inductor depends on these parameters. So we have assign various material properties for substrate, passivation, oxide layer, metal radiation boundaries etc .

Segments	Material assigned name	Relative Permittivity	Bulk conductivity S/m	Position X, Y, Z S/m	Size X, Y, Z um	Co-ordinate plane
Substrate	My_sub	11.9	10	-270,-270,0	540,540,300	Global
Oxide Layer	My_oxide	4	0	-270,-270,300	540,540,9.8	Global
Passivation	My_pass	7.9	0	-60,7.5,309.8	540,540,0.7	Global
Conductor(spiral)	My_met	1	2.8e7	-67.5,7.5,1	-14.7,0,1	Relative Cs
Ring	Pec	1	le30	-225,-225,0	450,450,2	Relative Cs
Ring Ext 1	Pec	1	1e30	-180,7.5,0	-30,-15,2	Relative Cs
Ring Ext 2	Pec	1	1e30	166,7.5,0	44,-15,2	Relative Cs
Underpass	My_met	1	2.8e7	-60,7.5,-0.8	-92,-15.5,-0.5	Relative Cs
Via 1	My_met	1	2.8e7	-60,7.5,0	-23,-15.5,-0.8	Relative Cs
Via 2	My_met	1	2.8e7	-140,7.5,0	-20,-15.5,-0.8	Relative Cs
Feed	My_met	1	2.8e7	-140,7.5,0	-27,-15,2	Relative Cs
Source1	-	-	-	-167,7.5,1	-14,-15,0	Relative Cs
Source2	-	-	-	147.5,7.5,1	18.5,-15,0	Relative Cs
Vacuum	Air	1	0	-270,-270,0	540,540,600	Global
Ground	-	-	-	-270,-270,0	540,540,0	Global

Table 3.1: segments drawing and materials properties

3.4.3 Some segments and their roles

Perfect conductor Perfect conductor is assumed as the material of the ring. Its bulk conductivity is 1e30S s/m

Raditation boundary and ground

Air is assign as radiation boundary. Ground is also assigned. Radiation is assigned fpr keeping the whole system safe from outside interference

Underpass:

Underpass is used as the M1 bmetal layer orlower layer. It is connected with spiral port and feed

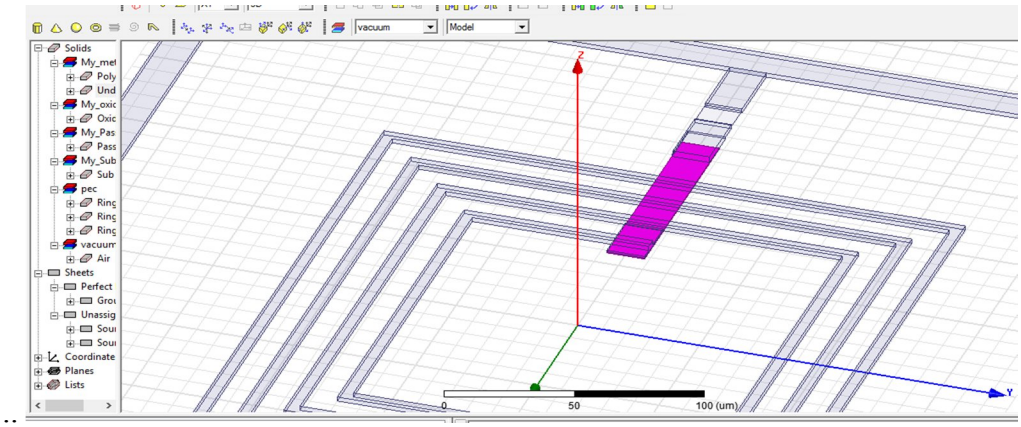

Figure 3.9 Underpass

Vias: Vias are used to connect two metal layers.

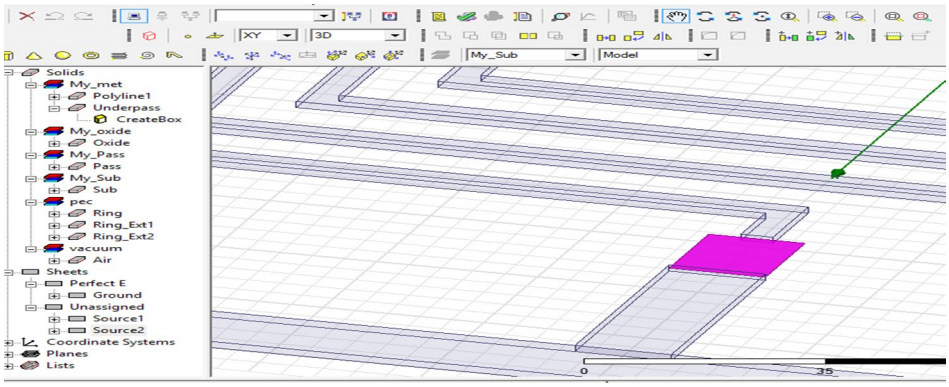

Figure 3.10: Vias

Spiral conductors:

The spiral metal is worked as an inductor. The value of this inductor is depend on number of turns. Diameter, material properties. This is the most important part.

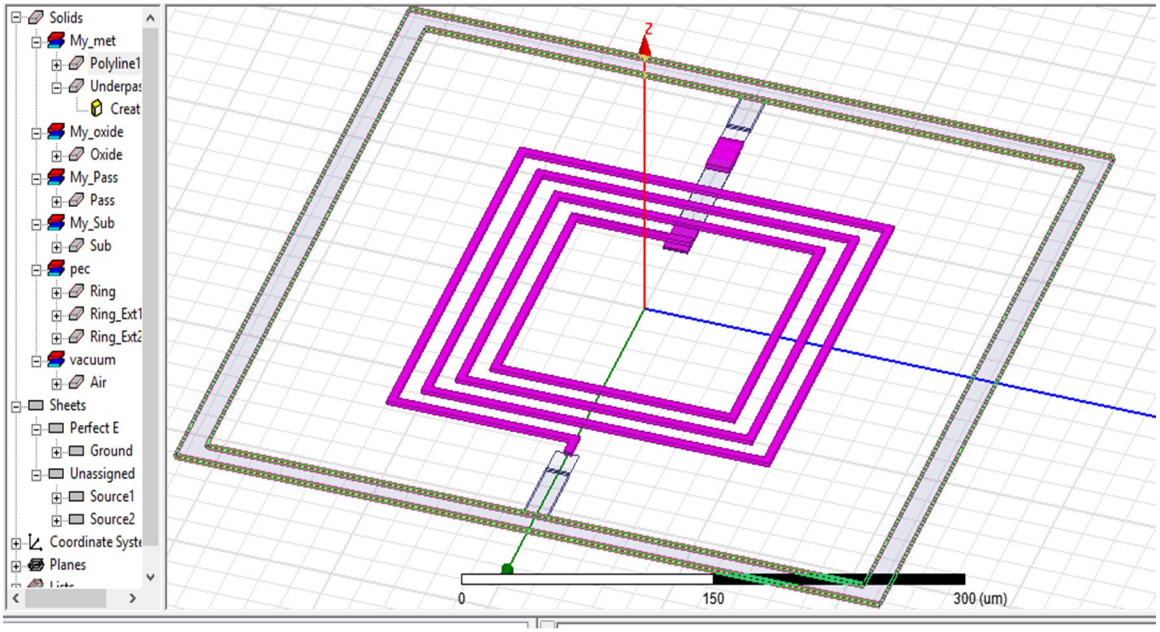

Figure 3.11: Spiral conductor acting as a inductor

Feed:

Feed is one kind of metal structure used for connecting with the source lumped ports.

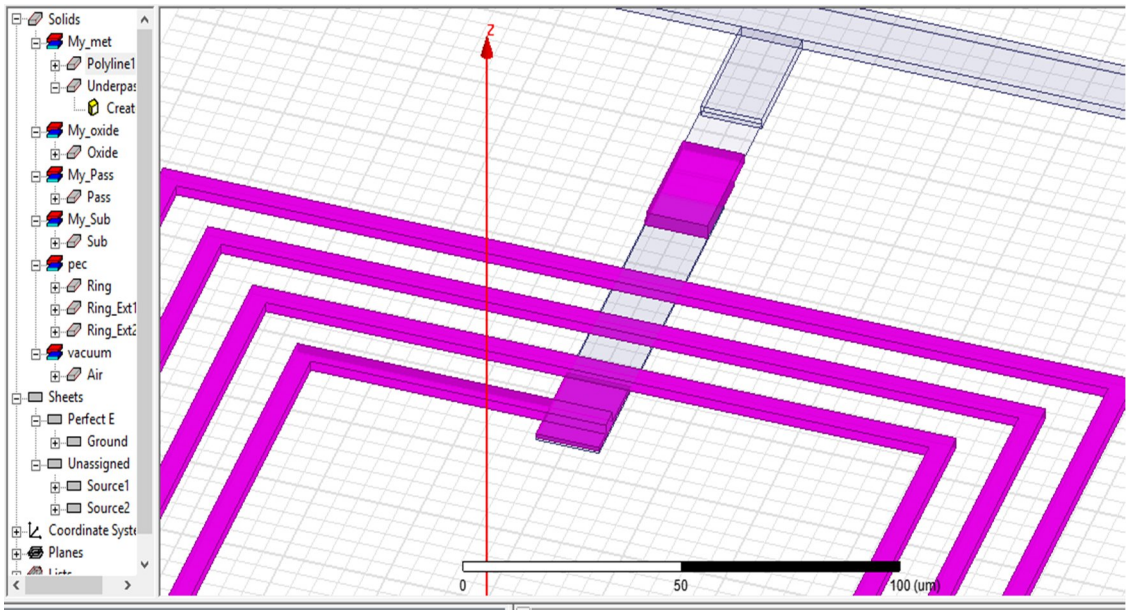

Figure 3.12: Feed

3.4.4 Validation check

A validation check is must before start analyze setup. If any error occurs it is shown in the message manager box. And the error must be solve before simulations because the simulations can not be run if there is any kind of errors occurs.

In HFSS we choose solve inside for the inductors conductive segments. For this reason HFSS gives a warning because ‘solve inside’ requires a large mesh which slows down the simulation. But it is necessary for the accuracy.

3.4.4 Analyze setup:

a) Solution Setup:

Parameter	**Value**
Solution frequency	12GHz
Maximum no. of passes	20
Maximum delta	.02

Table 3.2:Solution Setup

b) Frequency Sweep:

Parameter	**Value**
Maximum Solution	20
Error tolerance	0.5%
Start	0.1GHz
Stop	20GHz
Step	0.1 GHz

Table 3.3 Frequency Sweep

3.5 Simulations results

3.5.1 S parameters

In electrical system S parameter describe the input output relationship between terminals or ports. If there is two ports then S12 represents the power transfers from port 2 to port 1.and S21 represents the power transfer between port 1 to port . S11 - Forward Reflection (input match – impedance)

S22 - Reverse Reflection (output match - impedance)

S21 - Forward Transmission (gain or loss)

S12 - Reverse Transmission (leakage or isolation)

3.5.2 Quality factor:

A series resistance is created on the inductor by the copper or other electrically conductive metal wire that forms the coils. The electrical current that is flowing through the coils is converted into heat by this series resistance. So there creates a loss of inductive quality. The higher the Q the lower the rate of energy loss.

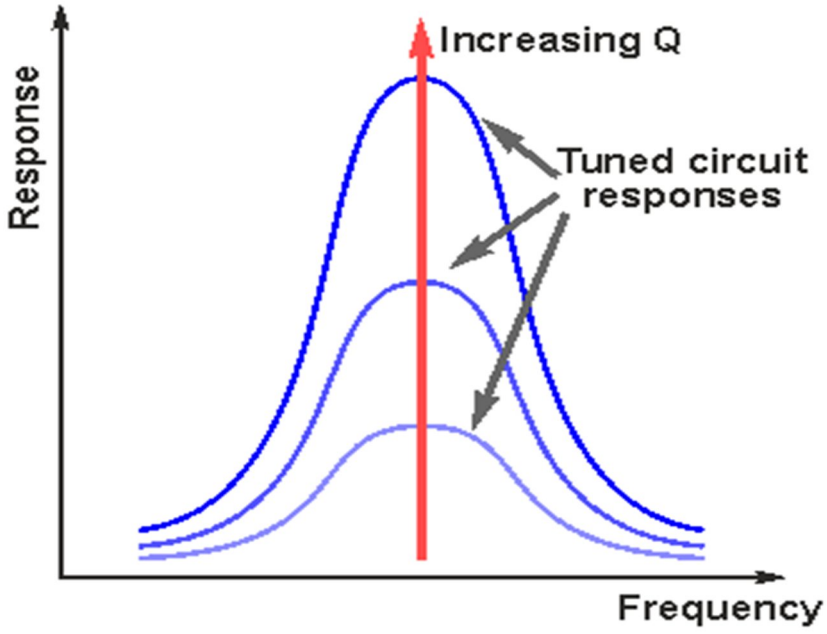

Figure 3.12: Quality factor Curve

3.5.3 Comparison between S parameters by changing no. of turns

a) S parameter VS frequency curve when the no. of turns is 4:

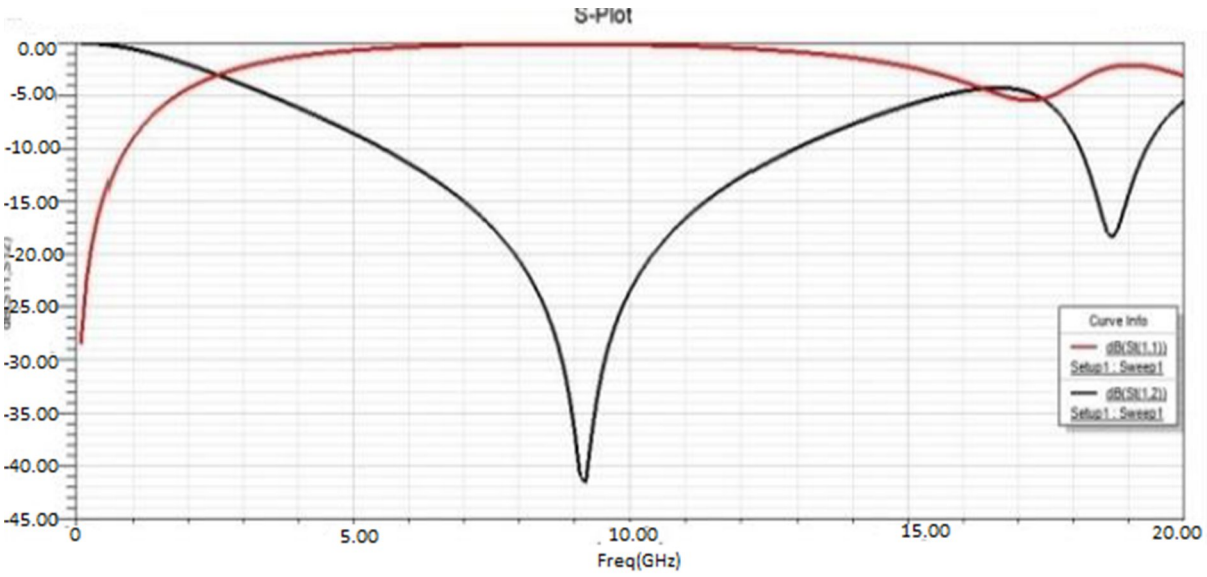

Figure 3.14 (a): S parameter Vs Frequency Graph when no. of turns 4

b) S parameter VS frequency curve when no. of turns is 5:

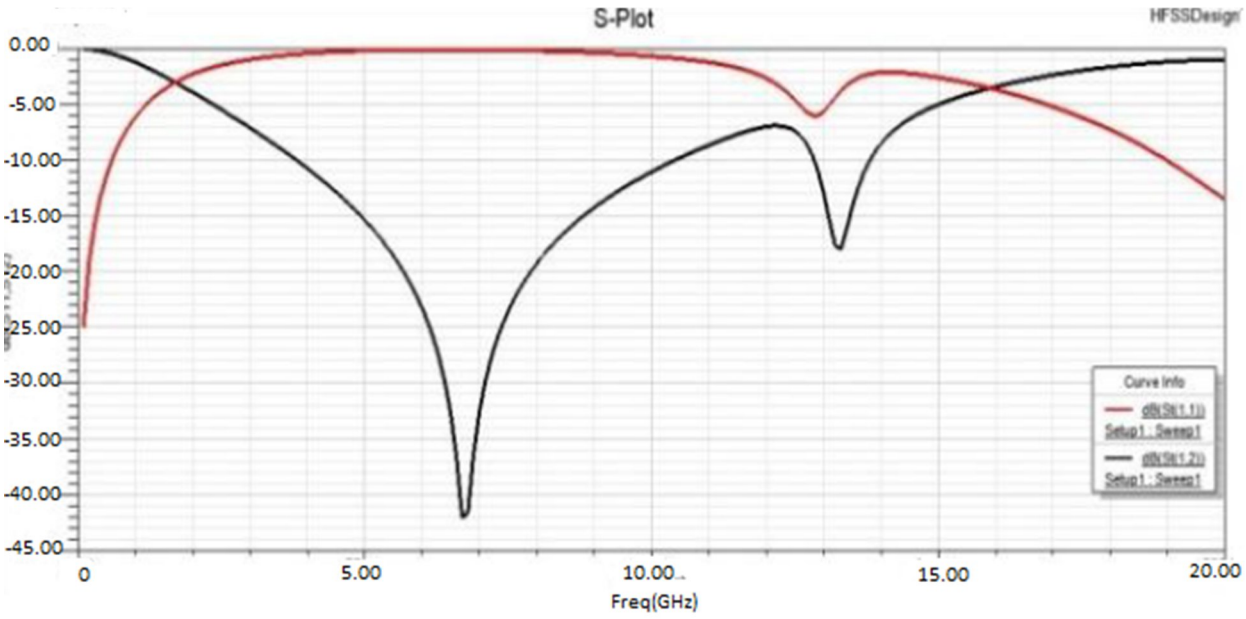

Figure 3.14 (b): S parameter VS Frequency Graph when no. of turns 4

So if we increased the number of turns the SRF falls down from 9.1 GHz to 6.9 GHz.

3.5.4 Comparison between Quality factor by changing bulk conductivity of substrate

a) when the bulk conductivity is 10 S/m:

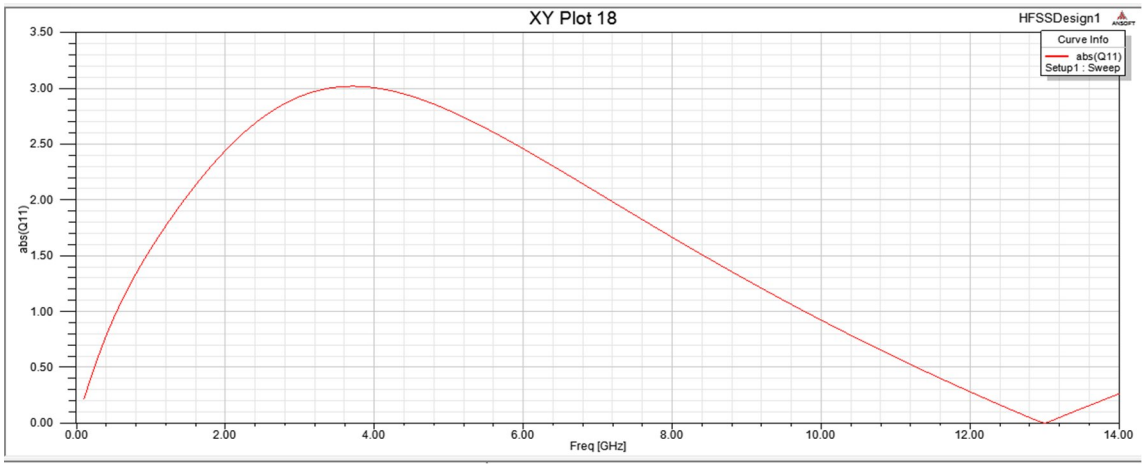

Figure 3.15 (a) : Quality Factor for substrate conductivity=10S/m

b)When the bulk conductivity is 60 S/m:

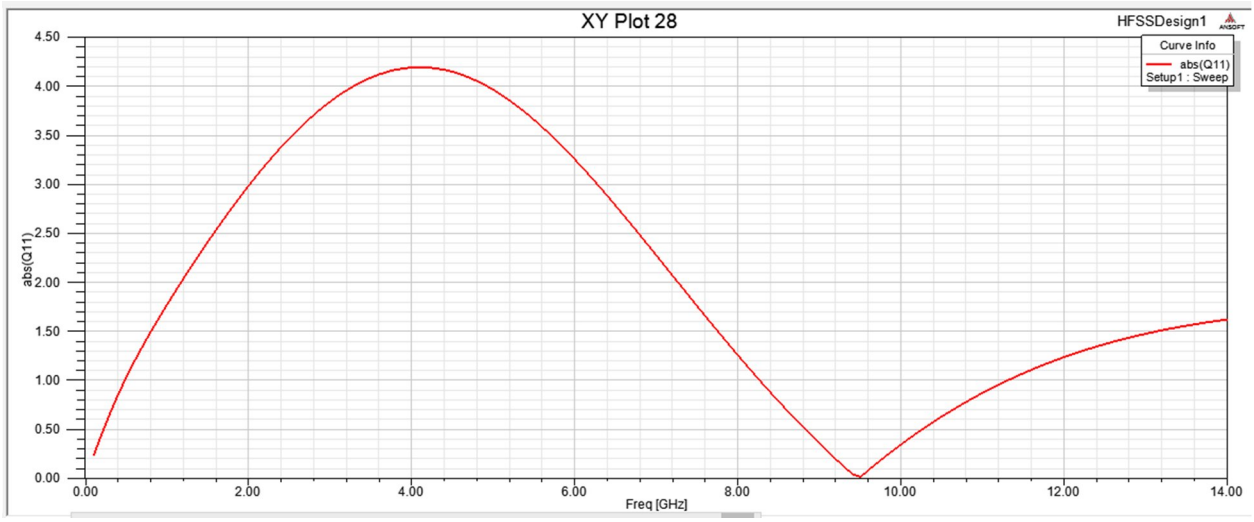

Figure 3.15 (b) : Quality Factor for substrate conductivity=70S/m

So, if we change the bulk conductivity of the substrate the quality factor will increase from 3.10 to 4.20. so the quality factor depends on the bulk conductivity.

3.5.5 Quality factor VS frequency curve varying no. of turns:

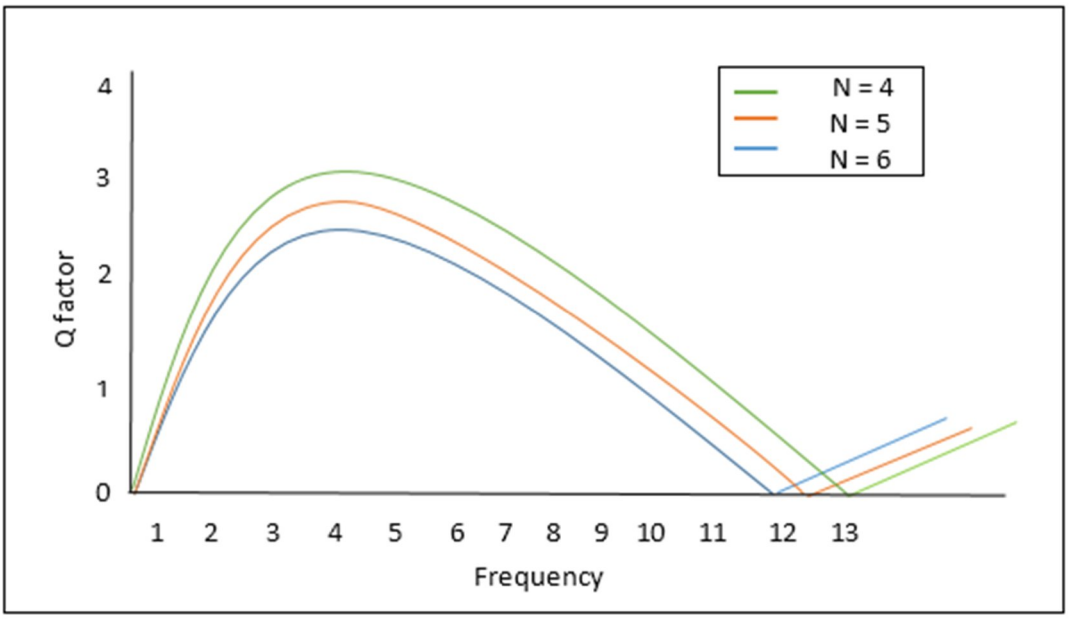

Figure 3.16 Quality Factor VS frequency curve varying the width

if we vary the no. of turns by 4, 5,6, where the width and spacing remains same we found that the quality factor becomes decreasing. So there is a energy loss if we increase the no. of turns.

3.5.5 Quality factor vs frequency curve varying the width:

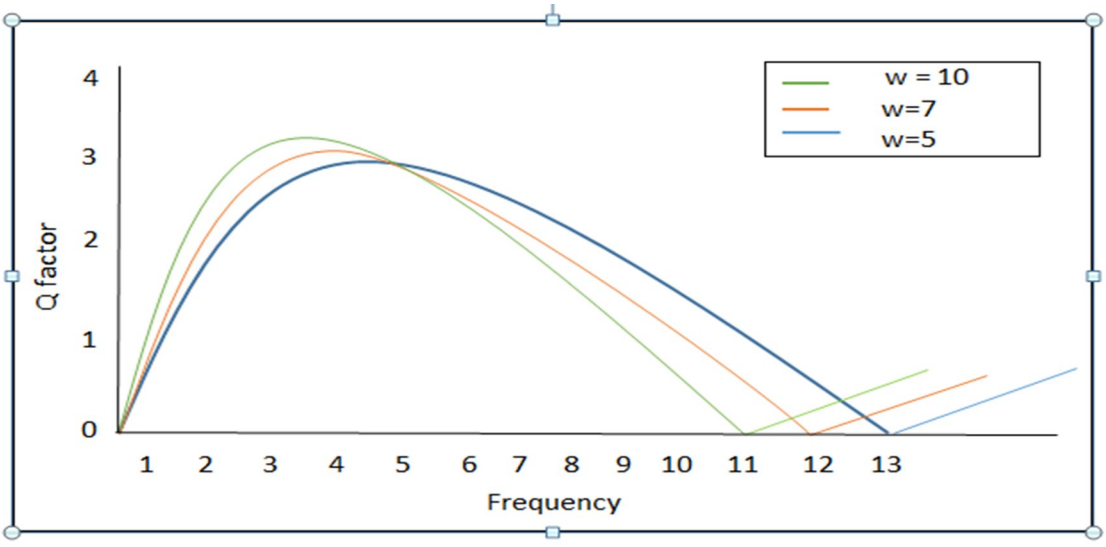

Figure 3.17: Quality factor VS frequency curve varying the width

Again if we vary the width the Quality factor become that is by increasing the width the Quality Factor become high. So, it is recommended to have a greater width for high gain. An increase in the width w of the spiral results in a decrement in the inductance value. There is decrease in the SRF values as well.

3.5.6Quality factor vs frequency curve varying the spacing:

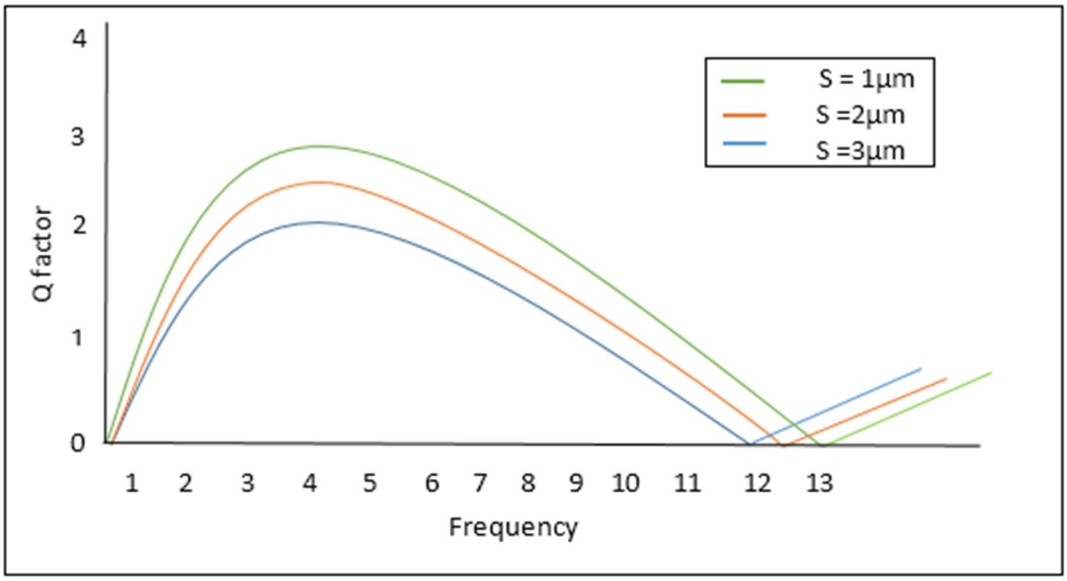

Figure 3.18: Quality factor VS frequency curve varying the spacing

It is observed that if we increase the spaces there is high energy loss as the Quality Factor decreasing

3.6 CST

CST stands for computer simulation technology. It is efficient for the accurate solution of the electromagnetic design and analysis in a wide range of frequencies. In CST we have design a two layer spiral inductor which is separated by dielectric. Then we have design a 3D model and analysis the result of the S parameters of it.

3.6.1 Design of inductive coupling:

We have design a inductive coupling by placing two spiral conductors in parallel and isolated by dielectric material.

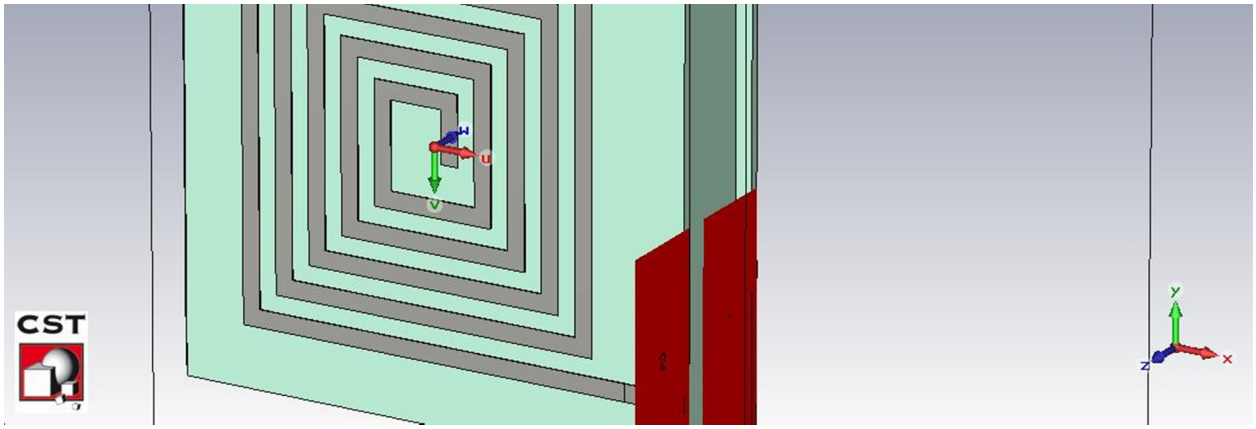

Figure 3.19: 3D view of inductive coupling

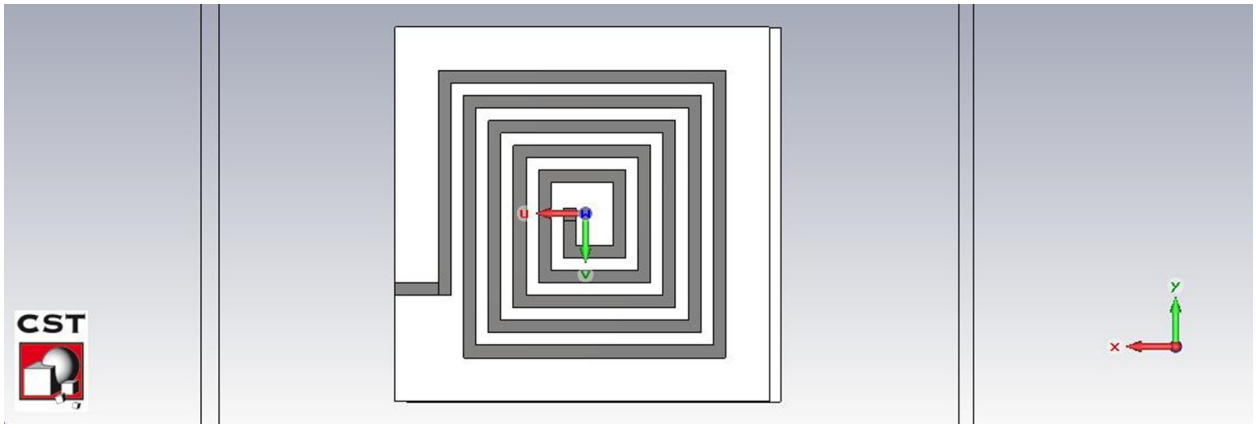

Figure 3.20 : Front view of inductive coupling

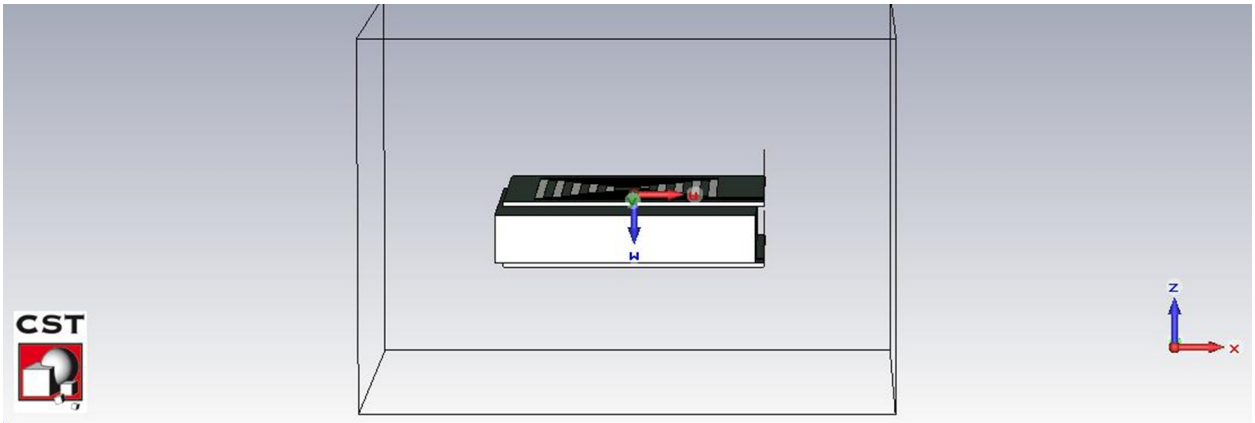

Figure 3.20 : Cross section of inductive coupling

3.6.2 Simulations Results and Analysis:

a) S parameters S11 and S22:

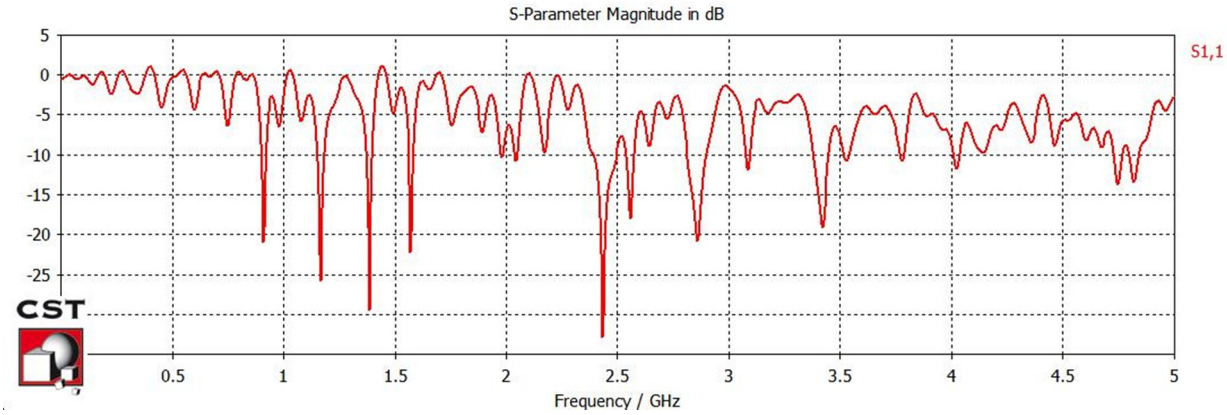

Figure 3.22 : S11 input reflection co-efficient

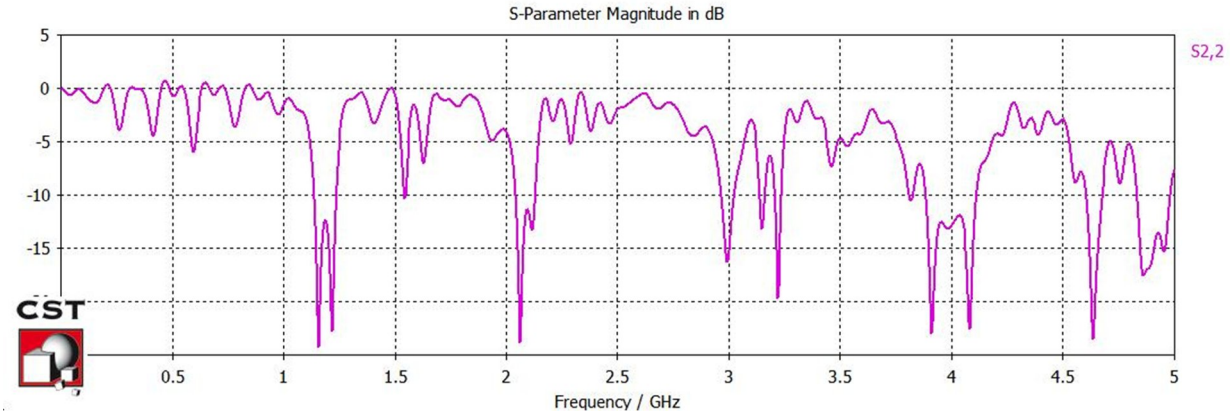

Figure 3.23: output reflection co-efficient

By simulating we have found the S parameters graphs . where, S11 is the input reflection co-efficient and S22 are the output reflection co-efficient. By seeing S11 we see that there is a very powerful resonance mode around 2.4GHz indicating by sharp peak but there are also four resonance as well as in band roughly o.8GHz to 1.6 GHz . Resonance occurs when a system can able to transfer or stored energy easily between two or more storage mode. We can explain S22 – the output reflection co-efficient in the same way.

b) S Parametrs S21 and S12:

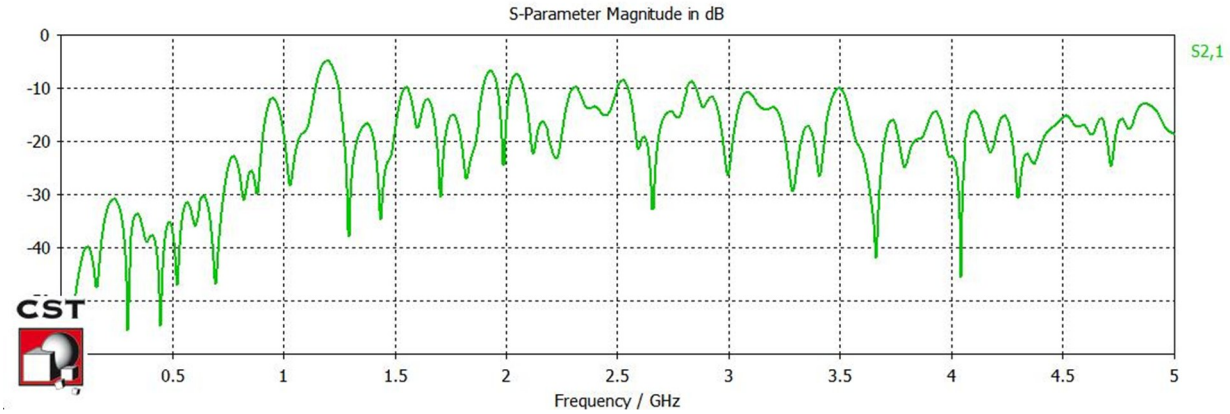

Figure 3.24: Forward transmission gain

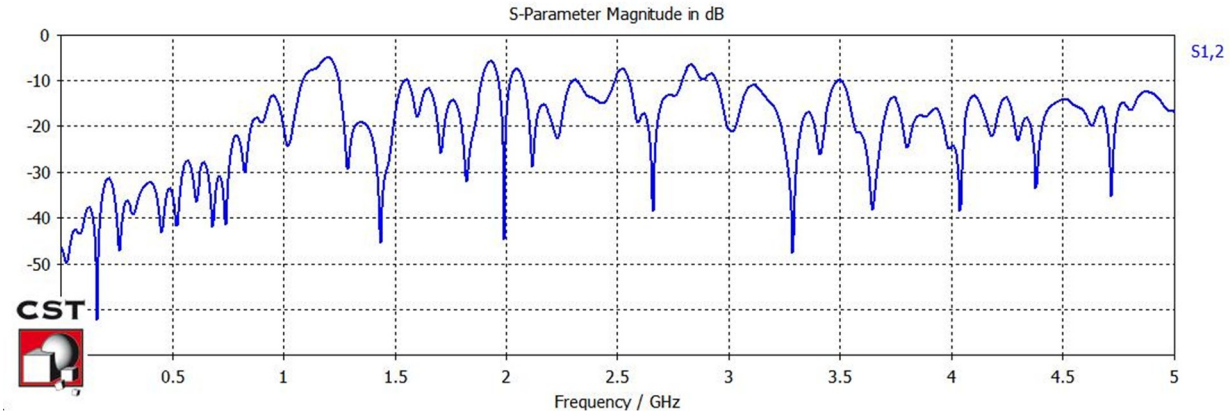

Figure 3.25: Reverse transmission gain

S21 and S12 which are transmission coefficient indicating that transmission is better at lower frequency but at that resonance it is not good. S21 is measure of transmitted power from Port 1 to Port 2. So there is a power transmitting but at a very low rate.

3.12 Analytical Calculations:

Transmitter

w = 8μm

n_T = 3 μm

Receiver

dinR = 100 μm

w = 5 μm

n_R = 4 μm

L_o = 6.31 nH/mm

C_o = 10.1 pF/mm^2

S = 1.0 μm

R_o = 0.832 Ω

C_{out} = 500 pF

X = 200 μm

R_{out} = 50 Ω

d_T = dinR – 25

= $100X10^{-3}$-$(2X1X10^{-3})$

= 0.098 mm

dint = d_T + 25 – 2nT(w_T+5)

= $0.098(2X1X10^{-3})$-$[(2X3)(8X10^{-3}+1X10^{-3})]$

= 0.046 mm

$d_{inR} = d_R + 25 - 2n_R(w_R+5)$

$\Rightarrow d_R = d_{inR} - 25 + 2n_R(w_R+5)$

$= (100X10^{-3})-2X(1X10^{-3})+2X4X(5X10^{-3}+1X)$

= 0.146 mm

$K = \frac{?}{?}$

$= \frac{?}{?}$

K = 0.0114

(1) For f= 2,4,6,8 GHz find out $\frac{?_?}{?_?}$

For f=2 GHz = $2x10^9$ Hz

$\frac{?_?}{?_?} = \frac{?}{?}$ X $j^w k?$ X $\frac{?}{?}$

$= \frac{?}{?}$ X $j^{2\pi f} k?$ X $\frac{?}{?}$

$= \frac{?}{?}$ X $\frac{?}{?}$

$\frac{?_?}{?_?} = ?$

$= 7.9101X10^{-3}$

= 0.0079

≈ 0.01

(2) for f = 4GHz = $4X10^9$ Hz

$\frac{?_?}{?_?} = \frac{?}{?}$ X $j^w k?$ X $\frac{?}{?}$

$$= \frac{??Ç???Æ?Ç??????Ç??}{Æ?Ç??????Ç??\ Æ?Ç??????Ç??}$$

$$= \frac{???Ç??\,??Ç???}{(??Ç??)^{?}?\,(??Ç??)^{?}}$$

= 0.0147

(3) for f = 6GHz = $6X10^9$ Hz

$$\frac{?_?}{?_?} = \frac{?}{???^{?}\,?_?\,?_?}\ X\ j^{w}k?\ \overline{?_?\,?_?}\ X\ \frac{?}{?_{???}(???\ ^{?}?_?\,?_?)?\,?_?\,?\,?^{?}\ Æ_?\,?_?\,?_{???}?\,?_?}$$

$$= \frac{?}{???^{???}?_?\,?_?}\ X\ j^{2\pi f}k?\ \overline{?_?\,?_?}\ X\ \frac{?}{?_{???}(??Æ???^{?}?_?\,?_?)?\,?_?\,?\,?^{???}Æ_?\,?_?\,?_{???}?\,?_?}$$

= 0.0172

(3) for f = 8GHz = $8X10^9$ Hz

$$\frac{?_?}{?_?} = \frac{?}{???^{?}\,?_?\,?_?}\ X\ j^{w}k?\ \overline{?_?\,?_?}\ X\ \frac{?}{?_{???}(???\ ^{?}?_?\,?_?)?\,?_?\,?\,?^{?}\ Æ_?\,?_?\,?_{???}?\,?_?}$$

$$= \frac{?}{???^{???}?_?\,?_?}\ X\ j^{2\pi f}k?\ \overline{?_?\,?_?}\ X\ \frac{?}{?_{???}(??Æ???^{?}?_?\,?_?)?\,?_?\,?\,?^{???}Æ_?\,?_?\,?_{???}?\,?_?}$$

$$\frac{?_?}{?_?} = ?\ \overline{(\ ÇÈ\ \ )^{?}\ \ (\ Ç\ \ É\ ?È\ ^{??})^{?}}$$

= 0.0158

Varying no. of turns:

When n=4:

f(GHz)	Vr/Vt
2	0.0079
4	0.0147
6	0.017
8	0.0157

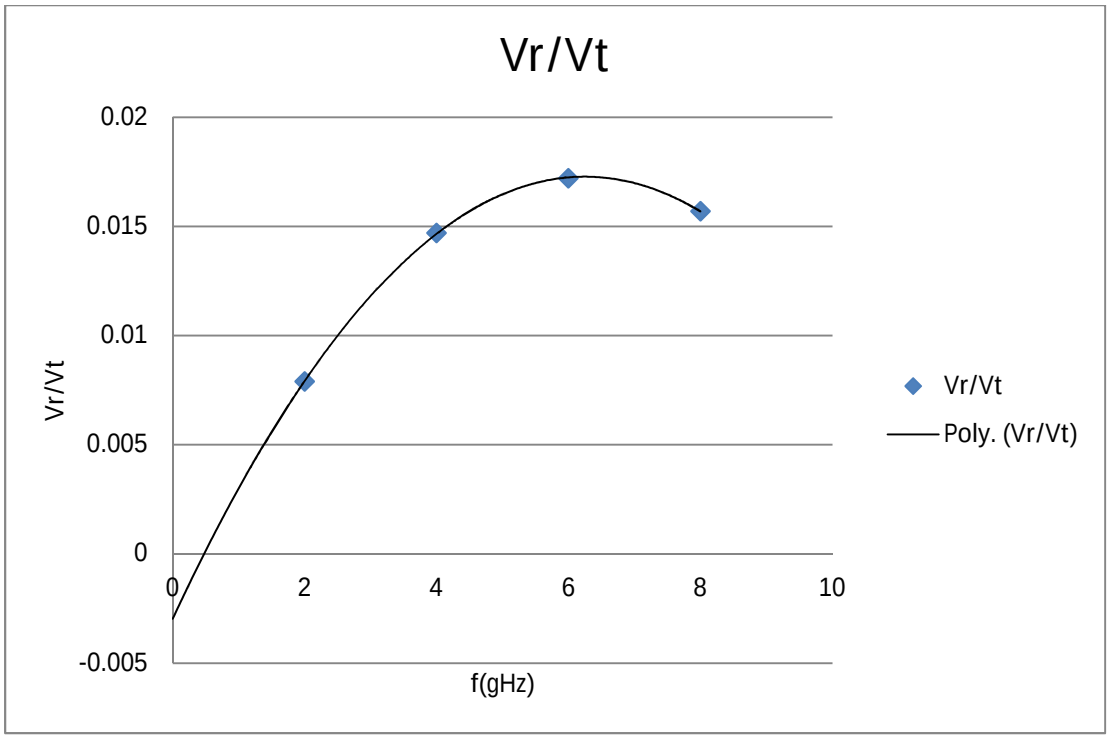

Figure 3.26: Analytical analysis of no. of turns 4

When n=5:

f(GHz)	Vr/Vt
2	0.0034
4	0.0062
6	0.0072
8	0.0065

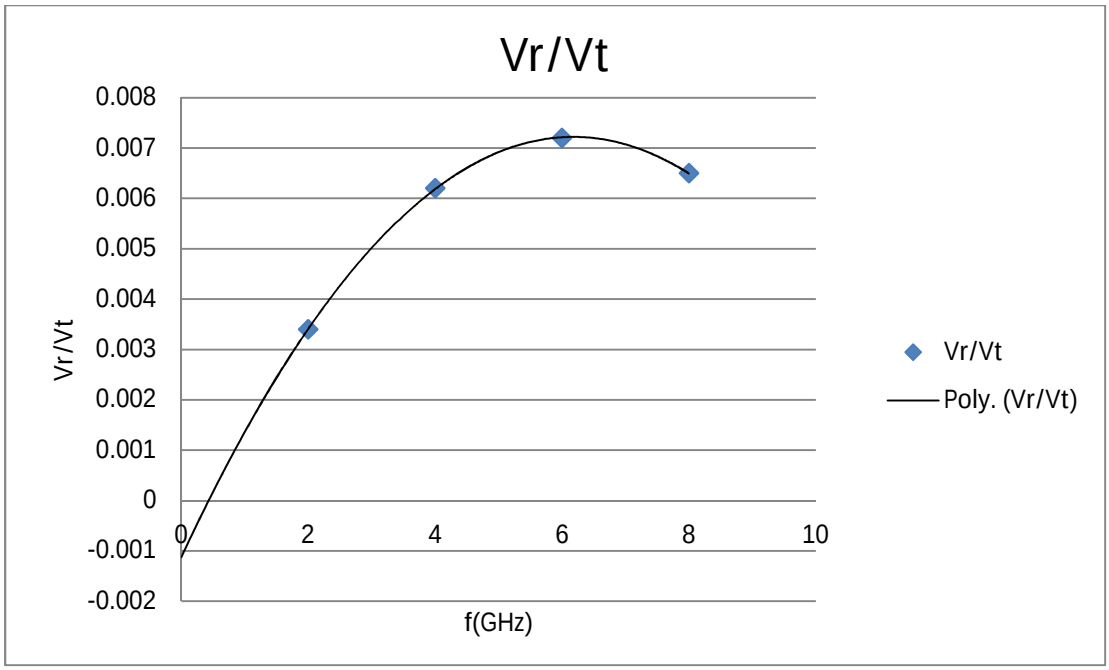

Figure 3.27: Analytical analysis of no. of turns

When n=6:

f(GHz)	Vr/Vt
2	0.0126
4	0.0233
6	0.0275
8	0.0217

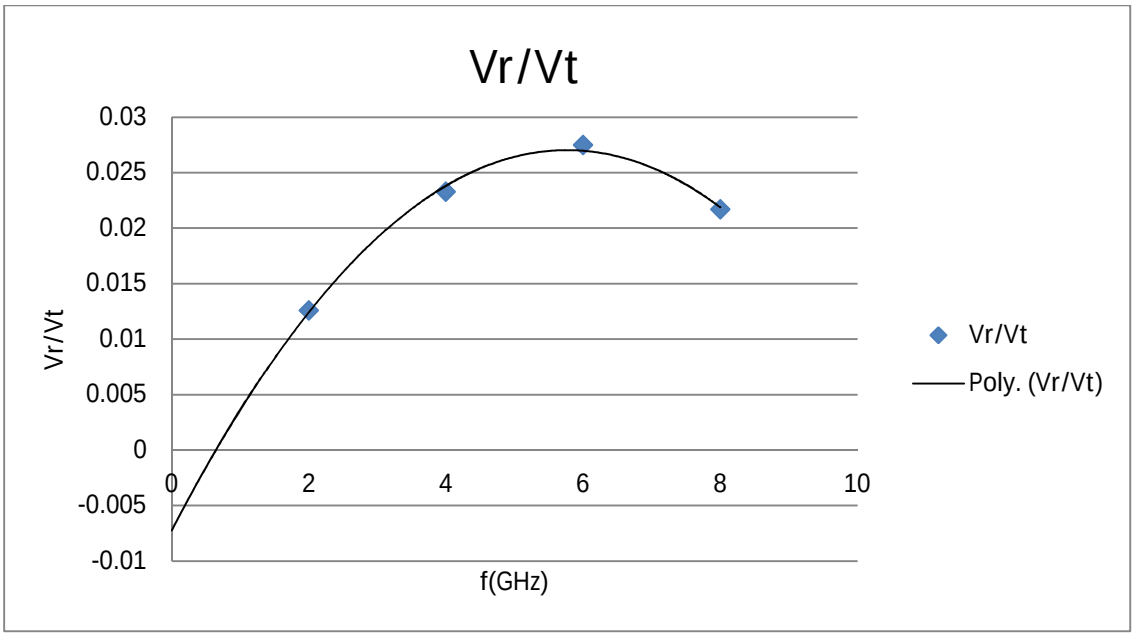

Figure 3.28: Analytical analysis of no. of turns 6

Varying w(width) : When w=5 micro meters:

f(GHz)	Vr/Vt
2	0.0079
4	0.0147
6	0.017
8	0.0157

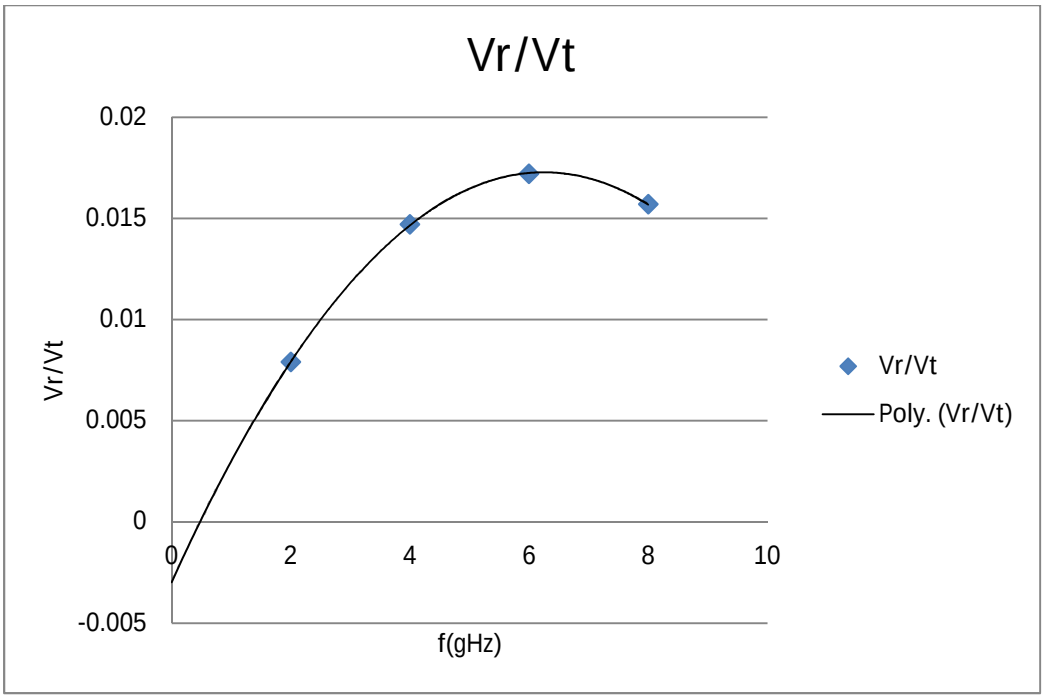

Figure 3.29: Analytical analysis of width 5 um

When w=7 micro meters:

f(GHz)	Vr/Vt
2	0.00852
4	0.0159
6	0.0186
8	0.0176

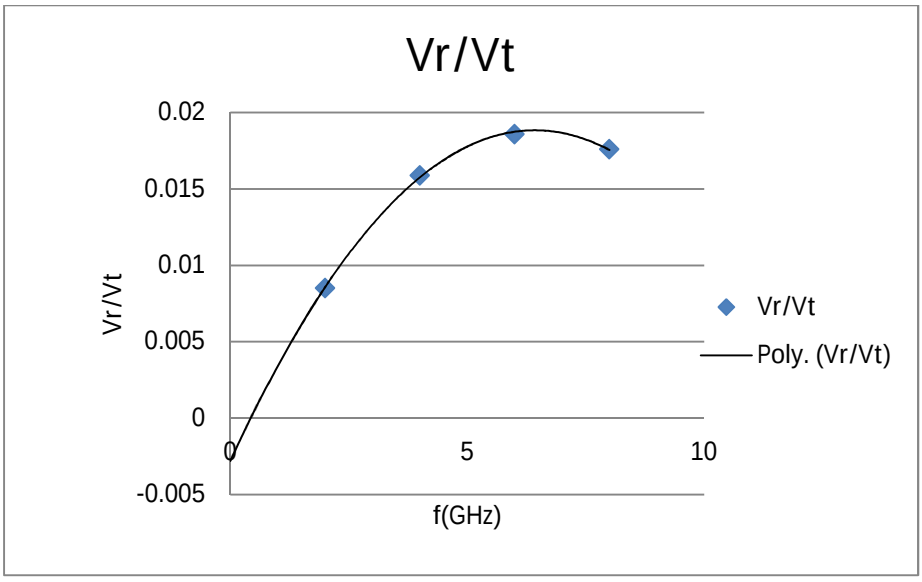

Figure 3.26: Analytical analysis of width 7 um

When n=10 micro meters:

f(GHz)	Vr/Vt
2	0.00944
4	0.0176
6	0.0205
8	0.0187

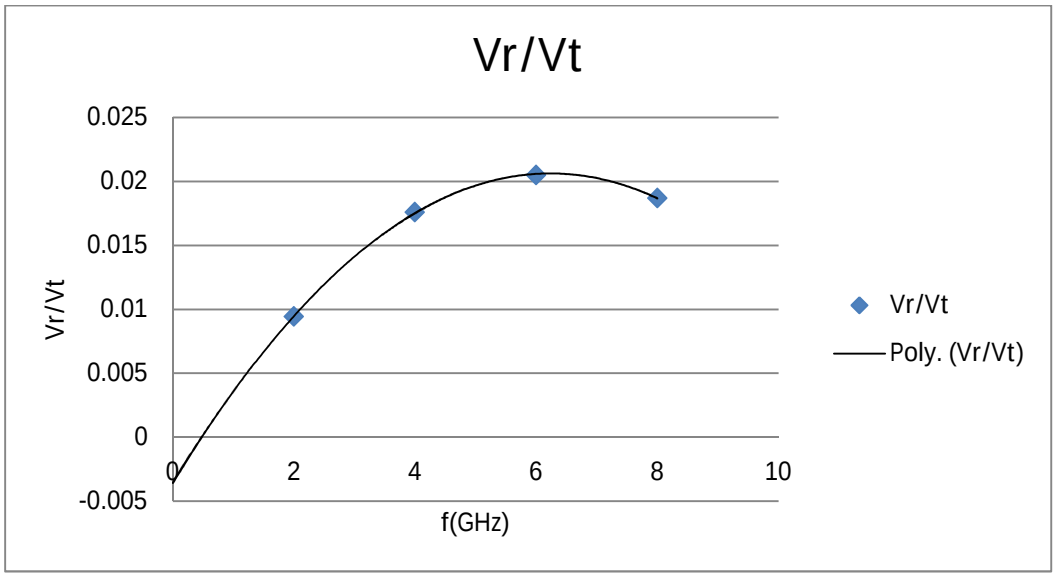

Figure 3.26: Analytical analysis of width 10um

3.8 Brief Discussion about Results:

The simulation results of the inductor depends on various materials and properties. The Quality factor is depend on the bulk conductivity of the substrate. It is also depends on the no. of turns, width and spacing of the inductors. It is recommended to use fewer turns in single layer which means lower n. By changing the area and width of the spiral the inductance and SRF can be tuned. Again a Bigger area means more parasitic currents presence into the substrate resulting in more high frequency losses in the substrate. In CST simulation the S-parameters shown that there is a signal transmission in inductive coupling but at a very low rate.

Chapter 4

Conclusion

4.1 Summery of Our Work

Our aim was to study or to do analysis on wireless inter-connect for future ULSI and also to explain recent advances of wireless interconnect in different potential applications.

In the first chapter we have described the basic concepts of wireless inter-connects, it's background and our objective to choose this interconnect technology over the traditional copper interconnect schemes. Moreover, we also provided a brief description of various evolutions of interconnect technologies over the time for better performance with the help of ITRS roadmap. In our second chapter, we talked about different methods of on-chip inter-connect technologies along with their advantages and disadvantages. We concluded this chapter by observing through comparisons that, wireless inter-connect gives us much more advantages on the basis of delay, power and bandwidth than traditional ones.

In third chapter we have designed single and multilayer inductors in 3D graphics environment and analyze the multi-parameters, Quality factor, inductance of the on chip inductor by varying number of turns, width, length, radius, material properties such as bulk conductivity, substrate properties etc. with the help of a user friendly software HFSS. By analyzing we have seen that by increasing the width and bulk conductivity of the substrate the Q factor will increase so there is low energy loss. Again, it is recommended to use fewer turns and fewer spacing among turns to have a high gain.

Again we have design a inductive coupling through multilayers where the layers are isolated by dielectric and we have analyze that there is a power transmission in inductive coupling but the transmitted power is very low.

Recommendation for future work:

In this research paper, wireless on chip interconnect advances over the years, different types of interconnect schemes have been described briefly. Moreover we chose to work on the wireless interconnect using inductive coupling as it opens various new paths and new technologies with better future. We use different software to analyze our work but still some other work can be done for the betterment of the research and design it on chip devices to diminish power loss and increase noise free data transmission in the near future.

After designing multi-layer inductive coupling in CST we observed that though we are getting advantages over power speed and cost but that has to achieved by scaling the devices. That means if we can scale the inductors in terms of thickness and width the power transmission can be increased. Again, also increasing the bulk conductivity of the substrate the Q factor can be improved and that can be done by proper substrate doping**.**

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