Characterization of Carbon Nanotube Field Effect Transistor

By

Sabbir Ahmed Khan (09221159)

Mahmudul Hasan (09221040)

A Thesis

Submitted as the partial Fulfillment for the Degree of

BACHELOR OF SCIENCE IN ELECTRICAL AND ELECTRONIC ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONICENGINEERING

BRAC UNIVERSITY

66, MOHAKHALI, DHAKA, BANGLADESH

CERTIFICATE OF APPROVAL

The thesis entitled **"Characterization of Carbon Nanotube Field Effect Transistor "** submitted by **Sabbir Ahmed Khan** and **MahmudulHasan** has been accepted satisfactorily in partial fulfillment of the requirement for the degree of Bachelor of science in Electrical and Electronic Engineering on September, 2012.

04/09/2012

Supervisor ----------

Dr. Sharif Mohammad Mominuzzaman

Abstract

From the concept of material science, any materials having an individual structure andcharacteristics have their own limitations. Due to the call for technological advancement,silicon-based integrated circuits and the scaling of silicon MOSFET design faces highcomplications like tunneling effect, short channel effect, gate oxide thickness effect etc. Tosolve these problems, new material alternatives are needed with such characteristics.

Recently, carbon nanotube has caught the attentions with promising future to replace silicon-based materials due to its superior electrical properties and characteristics. Simulation studies of carbon nanotube field-effect transistors (CNFETs) are presented using models of increasing rigor and versatility that have been systematically developed. The studies and modeling of carbon nanotube, which includes band structures and current-voltage graphical plots, are covered in this thesis.Also, analysis has been made to see the effect of gate oxide thickness change,temperature change, dielectric constant change, gate control coefficient, drain control coefficient and chirality changing effect on the device performance, in particular on the drain current.

The purpose of this paper is to study the behavior of CNFET and the main focus is on the simulation of its current-voltage (I-V) characteristic and observes the parameter changing effect on it. The simulation study is carried out using MATLAB program and the result obtained is used to compare the device performance with MOSFET. Besides, further analysis has been done through the comparison of the simulation result of the other groups to justify result.

ACKNOWLEDGEMENT

First of all both of we are very much grateful to the almighty ALLAH for directing us on the right path in perusing the requirement of the full thesis work.

Then we wish to express our deepest gratitude to our respected thesis supervisor Professor Dr. Sharif Mohammad Mominuzzaman for his sheer guidance and supervision throughout the entire period of work. His guidance, encouragement and invaluable suggestions are gratefully acknowledged.

Since our work is based on the Characterization of carbon nanotube field effect transistor we are also very much thankful to Mr. Jahangir Hossain and Mr. Sourav Mahmud for helping on this work, in particular on the MATLAB simulator.

Both of us are very much thankful to our beloved parents for their continuous encouragement towards a good work.

Last of all, we want to thank everyone who helped us to complete this work in various ways.

The Authors

Table of Contents

LIST OF FIGURES

pages

Chapter 3

Figure 3.16 I-V characteristics by changing chirality by Zhau Xu *et al.* This result Justifies the accuracy of our result 43

Chapter 1

INTRODUCTION

This research propose an enormous discussion of ballistic carbon nanotube field effect transistor and effects on transfers characteristics(I-V characteristic) by changing different parameter on input and comparing the result with other research group results and also verify the deviation from fabricated data. As an introduction this chapter presents the objective, background and the scope of this research work. This chapter also gives the outline of the thesis and as well as the summery of the content for each chapter.

1.1 Research Objectives

In recent years, the interest in novel device structures able to surmount the miniaturization limits imposed by silicon-based transistors has led researchers to explore alternative technologies such as those originated in the field of carbon nanotubes. Carbon nanotubes are a very promising material for future nanoelectronics, both as interconnects and as critical elements for field-effect transistors because of their low dimensionality and resulting impressive electronic properties [1]. So, the main interest of this research is to study the electrical properties of carbon nanotube and use it for analyzing the characteristics of nanoelectronic device. Nowadays ballistic carbon nanotube field-effect transistor (CNFET) is treated as one of nanoelectronic devices that have great potential to be the switching device for future. Let's focus on some of the core objectives of our research work:

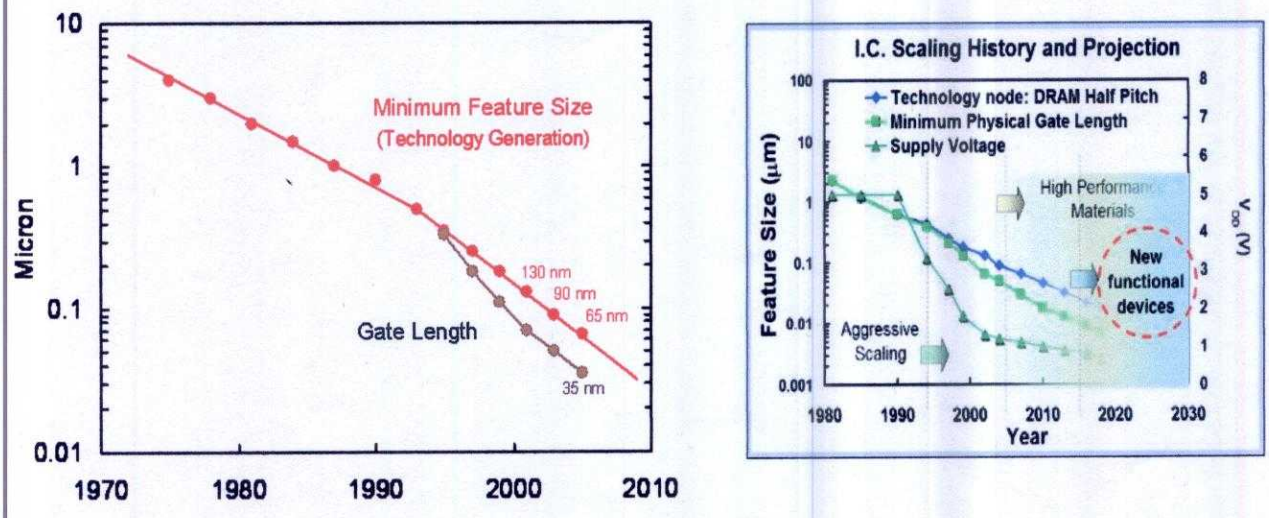
- Understand the basic of carbon nanotube physics and focus on their electrical properties.
- Analyze the carbon nanotube device model and the limitation of Si MOSFET.
- Realize theoretical difference between carbon nanotubes based FET and silicon FET.
- Understand the device characteristics, fundamental equation and mathematical model of CNFET.
- Using mathematical model simulation investigate the I-V characteristics of CNFET by varying different parameters and make an unalloyed comparison with different research group result.

By analyzing those objectives we can delineate total CNTFET Characterization and introduce same new important parameters which can be vital for device simulation and their significant changing effect on transfer characteristics.

1.2 Background and Research Motivation

The progress in silicon technology continues to outpace the historic pace of Moore's Law *[1], but the end of device scaling now seems to be only 10-15 years away. Therefore, it is of intense interest to find new, molecular-scale devices that might complement a basic silicon platform by providing it with new capabilities - or that might even replace existing silicon technology and allow device scaling to continue to the atomic scale. As device sizes approach the nanoscale, new opportunities arise from harnessing the physical and chemical properties at the nanoscale. Chemical synthesis, self-assembly, and template self-assembly promise the precise fabrication of device structures or even the entire functional entity. Quantum phenomena and dimensional transport may lead to new functional devices with very different power/performance tradeoffs. New materials with novel electronic, optical, and mechanical properties emerge as a result of the ability to manipulate matter on a nanoscale. It is now feasible to contemplate new nanoelectronic systems based on new devices with completely new system architectures, for examples: nanotubes, nanowires, molecular devices, and novel device concepts for nanoelectronics [2].

Of the various material systems and structures studied so far, carbon nanotubes have shown particular promise owing to their nanoscale size and unique electronic properties. Due to their low dimensionality, nanostructures such as quantum dots, carbon nanotubes (CNTs) possess unique properties that make them promising candidates for future technology applications [3]. Significant efforts have devoted to understand how a carbon nanotube transistor operates and to improve the transistor performance [4] [5]. Recently carbon nanotube field effect transistors (CNTFETs) have been fabricated successfully. It is reported that they have shown better performance than present silicon transistors of equivalent size.



(a) (b)

Figure 1.1: (a) Moore's law and (b) IC technology projection.

*[1]. "Moore's Law" is initiated by Gordon Moore, the Intel's founder. It is predicted that the performance of integrated circuit will double in every 18 months.

In this work, we developed physical simulation approaches to treat CNTFETs. However, to truly harness the potential of nanostructures, it is essential to develop a fundamental understanding of the basic physics that governs their behavior in devices. This is especially true for CNTs, where several researches has showed that the concepts learned from bulk device physics do not simply carry over to nanotube devices, leading to unusual device operation [3]. That's why this research includes the basics characterization of carbon nanotube especially electrical transport characteristics of CNTs.

1.3 Scopes of Work

Based on available resources, limited time frame and expertise, this research project is narrowed down to the following scope of work:

- Carrying out simulation study of carbon nanotube field-effect transistor using MATLAB program based on the mathematical model.
- Considering MOSFET like CNTFET rather than Schottky-Barrier CNTFET (SB-CNTFET) due to its better structure performance.
- Simulate the transfer characteristic by changing different parameters (like gate oxide thickness, chirality (leads to diameter), temperature, dielectric constant, gate and drain control coefficient) and collecting data.
- Comparing this simulation data with other research group data and notify the deviation from the practical fabricated data.
- Also analyze the simulation result and compared to conventional MOSFET transistor performance and conclude the output.

1.4 Outline of the Research Report

Including this chapter the report is organized into four chapters. Each chapter is organized precisely so that reader can identify the ultimate goal of the total work. The background and motivation, objectives and the scopes of this research has already been discussed.

Chapter 2 presents an overview of MOSFET and its growing limitation in CMOS technology. After that there is a gigantic discussion about carbon nanotube basic structure, chirality, Single wall CNT (SWNT), Multiple wall CNT (MWCNT) and electronic properties of CNT. So the chapter is going to give some brief introduction on physic of Carbon Nanotube and the reason of why Carbon Nanotube is chosen for the FET technology. At the end we discussed about the overview of CNTFET which includes different types of CNTFET their operation and difference between conventional FET.

Chapter 3 is our result analysis part. In this we are going to discuss the overall simulation result and analysis of all those results. Our results include oxide changing effect, dielectric constant changing effect, effect due to the chirality , effect due to the temperature changing and finally effect due to the gate and drain control coefficient.

Finally Chapter 4 is the conclusion of the whole projects and our future proposal.

Chapter 2

SCALING LIMITATIONS OF MOSFET AND INTRODUCTION TO CARBON NANOTUBE

2.1 Limitation of MOSFET Scaling

In 1930, Lilienfeld [6] patented the basic concept of the field effect transistor (FET). After thirty years in 1960, it was finally reduced to practice in Si-SiO_2 by Kahng and Atalla [7] [8]. Since that time it has been incorporated into integrated circuits and has grown to be the most important device in the electronics industry. Progress in this field for at least last 25 years has followed an exponential behavior that has come to be known as Moore's Law. Many reviewers have been written about current state and future prospects for Si MOS field effect transistors (MOSFETs). In particular, many different scaling limits for MOSFETs has been discussed and proposed [8]. In this portion current state of this scaling limit describes clearly. There are several effects that appear as the MOSFET size reaches nanometer scale and becomes the limiting factor that affect the performance of the MOSFET itself.

I. Short Channel Effect:

The short channel introduces several leakage current in MOSFET such as reverse bias p-n junction current, weak inversion current, Drain Introduced Barrier Lowering (DIBL) current [9].

- Reverse bias p-n junction current occurs due to the minority carrier. Diffusion near the depletion region and also electron-hole pair generation causes this leakage current.
- Weak reverse current occurs when gate voltage is less than threshold voltage.
- Drain induced barrier lowering (DIBL) current exists when source's potential barrier is reduced as a result of the drain's depletion region interacts with the source. The existence of DIBL will lower the threshold voltage.
- Gate-induced drain lowering (GIDL) current occurs in high electric field between gate and drain, and it also occurs along the channel width between gate and drain.
- Another leakage current mechanism, punchthrough, occurs when drain and source depletion regions touch deep in the channel.
- Narrow-width current arises when the channel length is reduced to less than 0.5μm.
- Gate-oxide tunneling current occurs when the oxide layer is made very thin and also causes gate leakage current tunneling through oxide bands.

- Hot-carrier injection occurs when hot carriers is injected into the oxide.

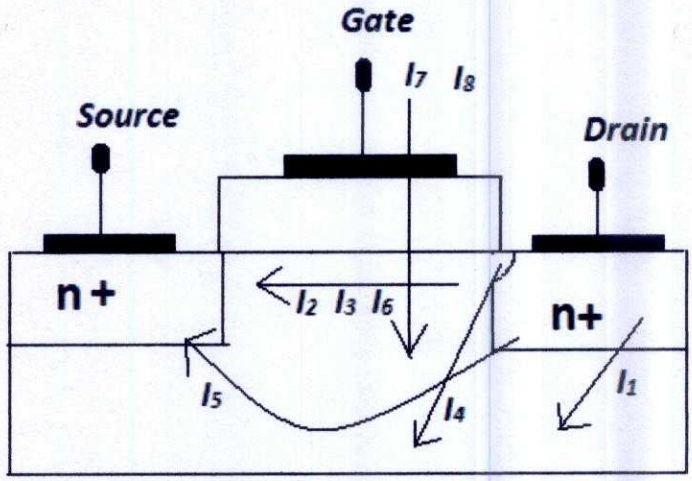


Fig 2.1: Short-channel-transistor leakage current mechanisms: reverse-bias p-n junction leakage (I_1), weak inversion (I_2), drain-induced barrier lowering (I_3), gate-induced drain leakage (I_4), punch-through (I_5), narrow-width effect (I_6), gate oxide tunneling (I_7), and hot-carrier injection (I_8).

II. Tunneling Limit:

Normally in an operating or computational system integrated transistors are separated sufficiently enough so that operation of one transistor does not affect another transistor. The separation is made by inserting a material that acts as a barrier between two transistors. However, the barriers are also becoming small when MOSFETs are scaling down. So there is a possibility that carrier of one MOSFET crossing over another and making distortion of the performance. This effect increases exponentially as the barrier distance decrease [10].

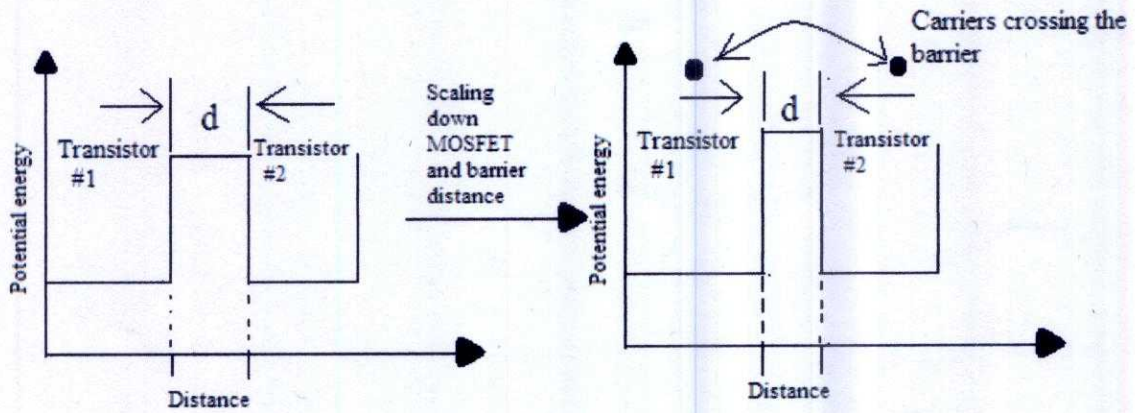


Fig 2.2: Potential barrier between two transistors.

III. Threshold Voltage Effect:

A notable limitation to MOSFET is that the threshold voltage is not proportionally decreasing with respect to transistor scaling. The threshold voltage held constant when the channel length is between 1μm-0.1μm and it deviates further when the channel length is below 0.1μm [10] [11]. If the transistor is scaled below 0.1μm, below the threshold voltage current does not drop to zero immediately but it decreases exponentially inversely proportional to the thermal energy [10]. There are some thermally distributed electrons at source terminal that have enough energy to overcome potential barrier controlled by gate terminal. This behavior is independent of channel length and power supply. So, higher threshold voltage causes higher leakage current. Denoting leakage current as I_{off} gives:

$$I_{off} = I_0(-\frac{qV_t}{mKT})$$

Here, I_0= Extrapolated current per width at threshold voltage.

m= Dimensionless ideality factor (typically 1.2)

V_t= Threshold voltage.

Lower leakage current is essential for a transistor due to reduce the power loss. However lower threshold voltage can reduce the leakage current. So, designing a transistor should be such a way so that its threshold voltage is very low. According to Sanudin, leakage current is reduced ten times for every 0.1V reduction of threshold voltage [10].

IV. Oxide Thickness:

As the size of the MOSFET is reduced, both the voltage and gate-oxide thickness must be reduced [11]. The gate oxide thickness is reduced in proportional with the channel length in order to ensure more effective gate control than drain terminal. Gate-oxide thickness causes two kinds of limitations. Firstly, the thin layer of oxide eventually increases leakage current. This effect is also related to quantum effect tunneling that dominates in MOSFET as the oxide thickness is reduced. The tunneling current due to thick oxide layer may look negligible in compare with on state current. But it has major effect when the chip is at standby mood. Secondly, due to the oxide thickness there is a loss of inversion charge and also the transconductance as a result of inversion-layer quantization and polysilicon gate depletion effect [12].

Some other limitation factors also seem in terms of scaling down of MOSFET:

2.1.1 Theoretical Limitation:

Thermal limit, quantum limit and power dissipation these are three important limitations usually count as a theoretical limitations. Amount of energy need to write a bit must be greater than the thermal function in order to avoid the bit error to occurs. This is called thermal limit. Currently CMOS need 10^{-13} J to write a bit and the trend is to reduce it in

order to reduce power dissipation as well [10]. Quantum limit is associated with E/f where, E is the thermal energy and f is the frequency. Currently CMOS is operating higher than the quantum limit and if the scale reaches to 100nm than it is expected the limit is approached as E is decreased and f is increased. Power dissipation limit is given by $p=EfnP$ where, n is device density and P is the probability of device switches in a clock cycle. Power dissipation limit is found to be around 100W/cm² [10]. As the size MOSFET is scaled down, the frequency increases, thus high density and low energy per bit are needed in order to ensure CMOS is operating within power dissipation limit.

Design Limitation:

Scaling down MOSFET discover its limitation of current design. Present MOSFET does not work effectively when it is scaled only around 30nm. The limit is only because of the fact of Zener breakdown at source/substrate junction [10]. Leakage oat gate is also starts surface and it becomes very difficult to have a control over channel. Dual-gate design can be an effective solution, but this is not our concern in the report.

Power Consumption and Dissipation:

Power consumption and heat dissipation is one of the obstacles for further advancement in Si-based transistors. For the past three years power density has grown with the rate of $S^{0.7}$ for every generation [13]. Large amount of power consumption boosts up the heat generation, increasing danger that transistors interfere with each other. As MOSFETs are scaling down so these small transistors are consume small amount of power but IC chip become denser because of large number of transistors on it. So it uses large amount of power to driven all transistors and therefore generates more heats. In November, 1971, Intel publicly introduced the world's first single chip microprocessor, the Intel 4004 with 2,300 Transistors at 10 µm, used tenths of watt while one of modern processor a 3.2 GHz Pentium IV extra edition consumes 135 watts [14]. Now in last few years increment in the number of transistors as 167 Million in dual core 2.8GHz Pentium D increased the power consumption to 244 watts.

Heat dissipation, Power consumption is major limitation with which traditional silicon-based MOSFET are suffering. Therefore, there is need of searching for new alternative Medias, which can overcome the limitations of conventional Si based MOSFET [15]. Here comes the idea of using carbon nanotube instead of silicon.

2.2 Introduction to Carbon Nanotube

Carbon nanotubes, long, thin cylinders of carbon, were discovered in 1991 by S. Iijima. These are quasi-one-dimensional molecular structures and can be considered as a result of folding graphite (a hexagonal lattice of carbon) layers into cylinders. They may be composed of a single shell namely single wall nanotube (SWNT) or of several shells namely multi wall nanotube (MWNT). Carbon nanotubes have shown a surprising array of properties. They can conduct heat as efficiently as most diamond (only diamond grown by

deposition from a vapour is better), conduct electricity as efficiently as copper, yet also be semiconducting (like the materials that make up the chips in our computers). They can produce streams of electrons very efficiently (field emission), which can be used to create light in displays for televisions or computers, or even in domestic lighting, and they can enhance the fluorescence of materials they are close to. Their electrical properties can be made to change in the presence of certain substances or as a result of mechanical stress. Perhaps the most exciting characteristics of carbon nanotubes are their unusual electronic properties. Carbon nanotubes can be metallic, semiconducting, or insulating depending on their length, diameter and rolling helicity, and do not requiring any doping. Again the energy gap of semiconducting carbon nanotubes can be varied continuously by varying the nanotube diameter. Here the band gap of semiconducting nanotubes decreases with increasing diameter. Individual carbon nanotubes are able to carry electrical current at significantly higher densities than most metals and semiconductors (maximum current density ~1013 A/m2). Another important property is nanotubes are also inert and have no surface states, making them very compatible with other materials such as oxides. These properties make carbon nanotubes a better choice than other molecular devices. Cutting edge research is focused on developing various devices from carbon nanotubes and on utilizing their unique properties in semiconductor technology for minimum possible feature sizes. Carbon nanotube field effect transistor is a novel outcome of this research. In our next section we will discuss in detail on the carbon nanotube physical structure, electrical properties and with the explanation. We strongly believe that Carbon Nanotube FET can provide better devices characteristics compared to the conventional MOSFET [16] [17] [18].

2.2.1 Physical structure of Carbon Nanotube:

As we said before there are two types of carbon nanotube which are single wall carbon nanotube and multiple wall carbon nanotube are shown in figure 2.3 and 2.4.

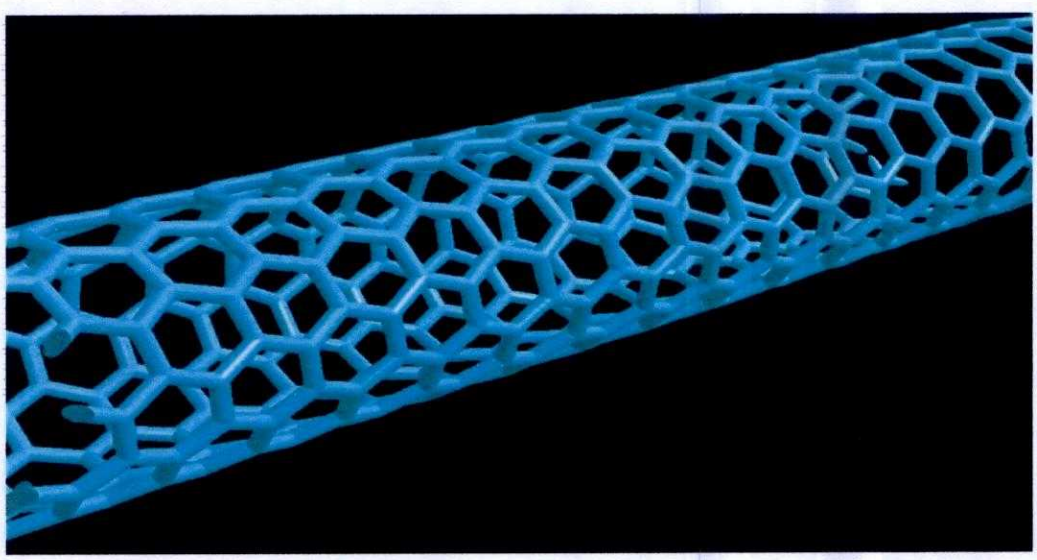


Fig 2.3: Single-wall Carbon nanotube

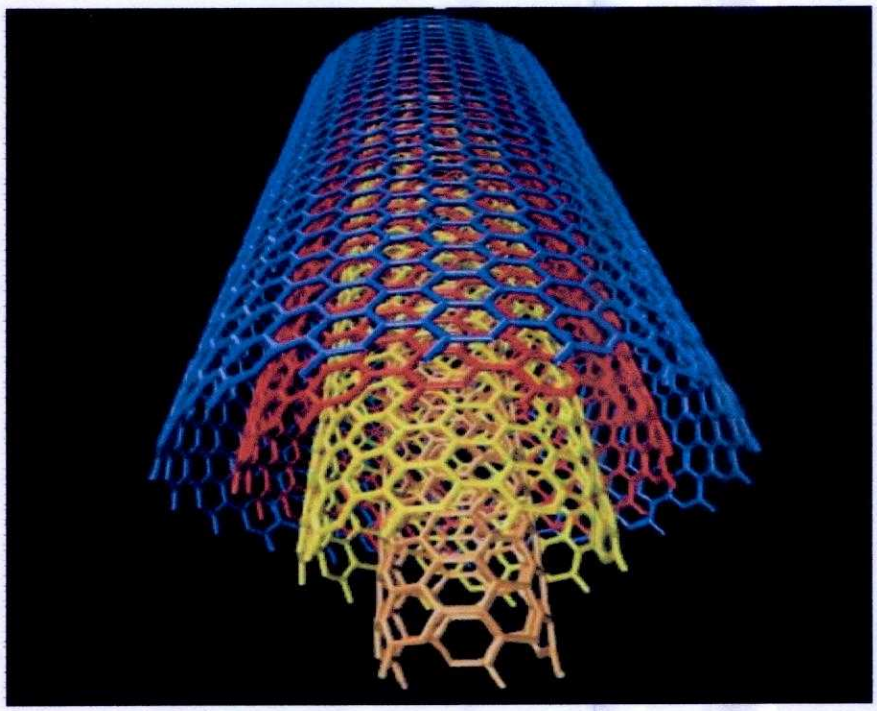


Fig 2.4: Multiple wall carbon nanotube [19].

SWNTs are more pliable than their multi-walled counterparts and can be twisted, flattened and bent into small circles or around sharp bends without breaking. They can be conducting, like metal (such nanotubes are often referred to as metallic nanotubes), or semiconducting, which means that the flow of current through them can be stepped up or down by varying an electrical field. On the other hand Multi-walled carbon nanotubes are basically like Russian dolls made out of SWNTs—concentric cylindrical graphitic tubes. In these more complex structures, the different SWNTs that form the MWNT may have quite different structures (length and chirality). MWNTs are typically 100 times longer than they are wide and have outer diameters mostly in the tens of nanometers. Although it is easier to produce significant quantities of MWNTs than SWNTs, their structures are less well understood than single-wall nanotubes because of their greater complexity and variety. Multitudes of exotic shapes and arrangements, often with imaginative names such as bamboo-trunks, sea urchins, necklaces or coils, have also been observed under different processing conditions. The variety of forms may be interesting but also has a negative side—MWNTs always (so far) have more defects than SWNTs and these diminish their desirable properties [19].

A SWNT is described as a graphene sheet rolled up into a cylindrical shape with axial symmetry, exhibiting a spiral conformation called chirality [20]. As Fig. 1.1 shows, graphene has a hexagonal structure, and rolling up the graphene sheet in different directions and diameter would yield the nanotubes with different symmetries, which induces different electronic structures.

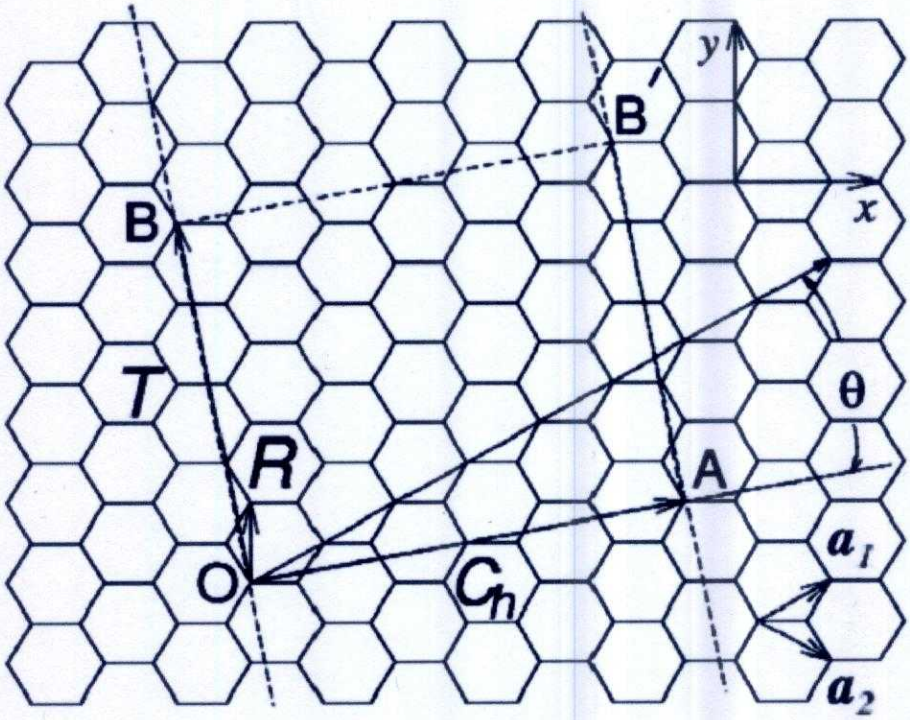


Fig: 2.5: (4,2) carbon nanotube as a graphene sheet.

Since electronic properties of SWNTs depend on their structures, it is very important to find a way to specify the geometric structure of a SWNT. As shown in Fig. 2.5, we can roll up the graphene sheet alone vector OA, which is perpendicular to the nanotube axis in the direction of OB. Here, we can see that O, A, B and B' are four crystallographically equivalent sites. By rolling up the paper plane and making OB overlap with AB', we get a seamless single-walled tubular structure. Then it would be straightforward to define the vectors $C_h = OA$ as chiral vector and $T = OB$ as translational vector. If we use a_1 and a_2 as the base vectors of graphene 2-dimentional crystal lattice, we can have the chiral vector as:

$$C_h = na_1 + ma_2 \equiv (n, m)$$

Where, n and m are integers and $0 \leq m \leq n$.

SWNT structure can be exclusively specified by chiral vector, we can use the integer pair (n,m) to specify a SWNT. The single-walled carbon nanotubes can be divided into 3 groups: zigzag nanotubes (n, 0), armchair nanotubes (n, n) and all other chiral nanotubes. For CNT, the length of base vectors is a = 2.49 Å, and then the length of chiral vector is:

$$C_h = a\sqrt{n^2 + m^2 + nm}$$

And thus the diameter of the SWNT is:

$$d_t = a\sqrt{n^2 + m^2 + nm}/\pi$$

The chiral angle can be obtained as:

$$\theta = \arccos\frac{2n + m}{2\sqrt{n^2 + m^2 + nm}}$$

In summary, with the index (n, m), we can exclusively specify the structure of a SWNT and obtain the important geometric parameters such as diameter and chiral angle [21][22].

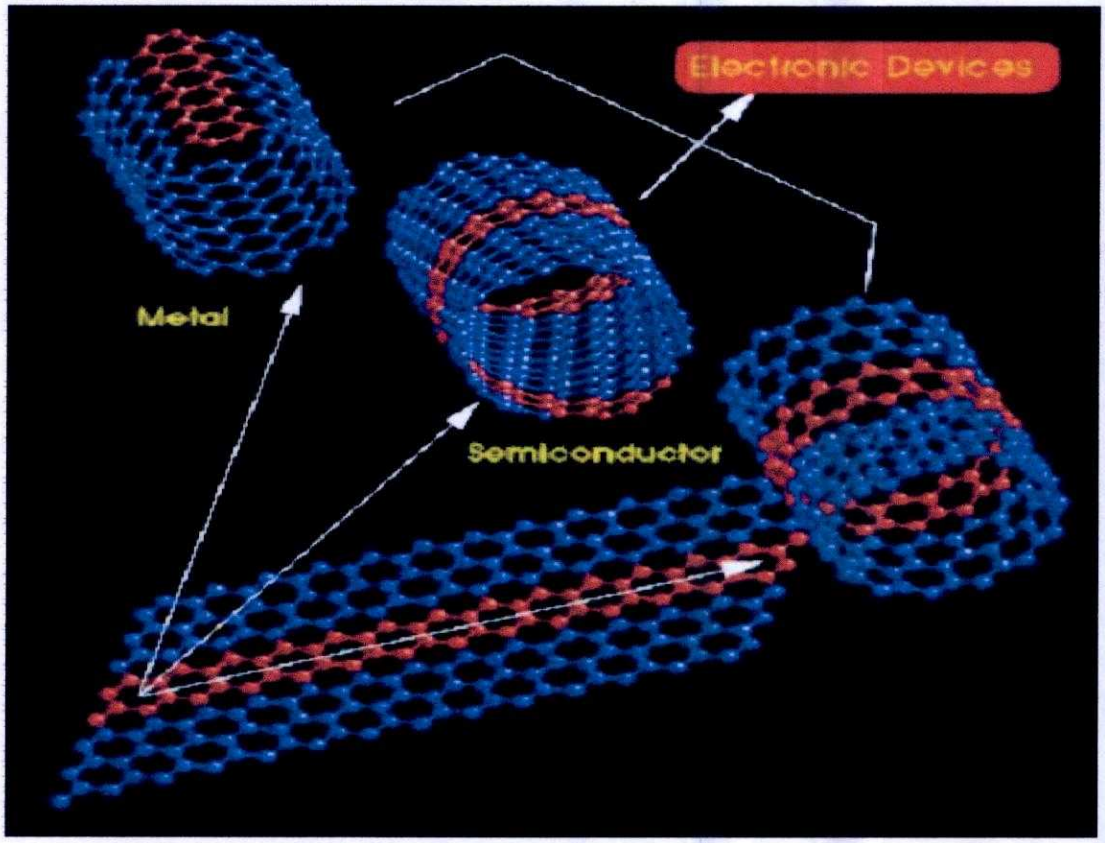


Fig: 2.6: Rolling graphene sheet to create Carbon Nanotube.

2.2.2 SWNT Characteristics of Electrical Transport:

A determination of the band structure allows for the calculation of an energy dependent Drude conductivity for the graphene sheet that constitutes a nanotube surface, as:

$$(\frac{2e^2}{h})\frac{E}{hv_F}l_e$$

Here, the elastic scattering length (le) of the carriers is proportional to the electron-phonon scattering and generally increases with decreasing temperature .One characterize the electrical conductivity in two regimes:

(1) Low temperatures ($k_BT<E_F$), where in the conductivity equation above, the energy (E) replaced by E_F (the Fermi energy).The conductivity in this regime is metallic. A finite zero-temperature value, the magnitude of which is determined by the static disorder, is obtained.

(2) High temperatures (kBT>EF), where in the conductivity equation, the energy (E) is replaced by k_BT. The conductivity, and the carrier density, is then directly proportional to T.

At the very outset, it is not trivial to measure the intrinsic resistance of a SWNT. Any contact in addition to those at the two ends of the tube can destroy the one-dimensional nature of the SWNT and make a true interpretation difficult. Theoretically, for a strictly one-dimensional system the Landauerm formula predicts an intrinsic resistance, independent of the length is equal to $h/e^2 (1/T(E_f))$. Assuming perfect transmission through ideal Ohmic contacts, i.e., T(E_F) equal to one. This contact resistance arises from an intrinsic mismatch between the external contacts to the wire (which are of higher dimensionality) and the one-dimensional nanotube system and is always present. When one takes individually into account both the two-fold spin and band degeneracy of a nanotube the intrinsic resistance (R_{int}) now becomes: $(R_{int})= h/4e^2 (1/T(E_f))$, which again seems length independent.

However, in the above discussion, we have not yet considered the contribution of the external contacts. When we consider the transmission (T) through the contacts into the one dimensional channel and then to the next contact, $T= le/ le+L$, where le is the mean free path length for scattering and L is the length of the one-dimensional conductor. The resistance is now equal to

$$\frac{h}{4e^2}\frac{l_e+L}{l_e} \equiv \frac{h}{4e^2}\left(1+\frac{l_e}{L}\right)$$

The first term represents R_{int} while the second term denotes an Ohmic resistance (R_{Ohmic}) associated with scattering. In the presence of dynamically scattering impurities, such as acoustical or optical phonons, which are inevitably present at any temperature above 0 K, the Ohmic resistance should definitely be considered. It is interesting to consider the limiting cases of a large mean free path ($le \rightarrow$ infinity) or a small tube (L$\rightarrow$ 0) i.e., in the

ballistic regime, when the Ohmic resistance is seen to vanish. Finally, the material resistance of the contacts contributes an additional term: R_c. The total resistance as measured in an external circuit would now be: $R = R_{int} + R_{Ohmic} + R_c$. These considerations imply that a minimum resistance of $h/4e^2$ (~6.5 k ohm) is present in a SWNT with a single channel of conduction. In practice however, imperfect contacts (which lead to T<1) and the presence of impurities lead to larger resistance values, while deviations from strict one-dimensionality or multiple channels of conduction (as in a MWNT) could lead to smaller numbers for the resistance.

2.3 Carbon Nanotube field effect Transistor:

2.3.1 Structure of CNTFET:

The first carbon nanotube field-effect transistors were reported in 1998. These were simple devices fabricated by depositing single-wall CNTs (synthesized by laser ablation) from solution onto oxidized Si wafers which had been prepattemed with gold or platinum electrodes. The electrodes served as source and drain, connected via the nanotube channel, and the doped Si substrate served as the gate. A schematic of such a device is shown in Fig. 2.7 Clear p-type transistor action was observed, with gate voltage modulation of the drain current over several orders of magnitude. The devices displayed high on-state resistance of several MQ, low transconductance ($-I_{ns}$) and no current saturation, and they required high gate voltages (several volts) to turn them on.

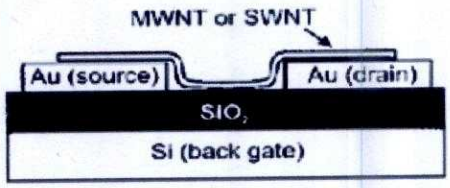


Fig 2.7: Early CNTFET structure.

Following these initial CNTFET results advances in CNTFET device structures and processing yielded improvements in their electrical characteristics. Rather than laying the nanotube down upon the source and drain electrodes, relying on weak van der Waals forces for contact, the electrodes were patterned on top of previously laid down CNs. In addition to Au, Ti and CO were used, with a thermal annealing step to improve the metal/nanotube contact. In the case of Ti, the thermal processing leads to the formation of TiC at the metal/nanotube interface, resulting in a significant reduction in the contact resistance - from several MΩ to – 30 kΩ. On-state currents ~1 μA were measured, with transconductance - 0.3 μS. All early CNTFET were p-type, i.e., hole conductors. Whether this was due to contact doping or doping by the adsorption of oxygen from the atmosphere was initially unclear. N-type conduction was achieved by doping from an alkali (electron donor) gas and by thermal annealing in vacuum. Doping by exposure to an alkali gas involves charge transfer within the bulk of the nanotube, analogous to doping in

conventional semiconductor materials. On the other hand, annealing a CNTFET in vacuum promotes electron conduction via a completely different mechanism: the presence of atmospheric oxygen near the metal/nanotube contacts affects the local bending of the conduction and valence bands in the nanotube by way of charge transfer, and the Fermi level is pinned close to the valence band, making it easier for injection of holes. When the oxygen is desorbed at high temperatures, the Fermi level may line up closer to the conduction band, allowing injection of electrons. Contrary to the case of bulk doping, there is no threshold voltage shift when going from p-type to n-type by thermal annealing. In addition, it is possible to achieve an intermediate state, in which both electron and hole injection are allowed, resulting in ambipolar conduction. The ability to make both p-type and n-type CNTFETs enabled the first carbon nanotube CMOS circuits. These were demonstrated by Derycke et al., who built simple CMOS logic gates, including an inverter in which the two CNTFETs were fabricated using a single carbon nanotube. Subsequently, more complex CN-based circuits have been built as well. Carbon nanotube field effect transistor (CNTFETs) uses semiconducting carbon nanotube as the channel. Both p-channel and n-channel devices can be made from nanotubes. The physical structure of CNTFETs is very similar to that of MOSFETs and their I-V characteristics and transfer characteristics are also very promising and they suggest that CNTFETs have the potential to be a successful replacement of MOSFETs in nanoscale electronics. Of course, there are some distinct properties of CNTFETs, such as:

- The carbon nanotube is one-dimensional, which greatly reduces the scattering probability. As a result the device may operate in ballistic regime.
- The nanotube conducts essentially on its surface where all the chemical bonds are saturated and stable. In other words, there are no dangling bonds which form interface states. Therefore, there is no need for careful passivation of the interface between the nanotube channel and the gate dielectric, i.e. there is no equivalent of the silicon/silicon dioxide interface.
- The Schottkey barrier at the metal-nanotube contact is the active switching element in an intrinsic nanotube device.

Because of these unique features CNTFET becomes a device of special interest. The field effect transistors made of carbon nanotubes so far can be classified into two types:

a) Back gate CNTFET

b) Top gate CNTFET

Other than these 2 biggest classes, some semiconductor companies have been proposed their own new/next generation Carbon Nanotube FET such as Infineon introduced their vertical carbon nanotube FET (VCNTFET) concept in year 2003.

2.3.2 Back-gated CNFET:

CNFET was first demonstrated in 1998 by Tans et. al. [28] to show a technologically exploitable switching behavior and this work marked the inception of CNFET research progress. Experimental work by Tans et. al. managed to modulate the conductivity more than five orders of magnitude by applying electrical field to the nanotube [24]. Majority of the early CNFET devices were back-gated with very thick gate insulators made of silicon oxide approximately around 100-150nm [16]. This structure used a non-local back-gate with the carbon nanotube side is bonded to noble metal electrodes [33]. Noble metal is a type of metal that resists the attack of acids and other reagents and does not corrode. Fig:2.8 shows the structure of back gated CNTFET.

Fig 2.8: Back gated CNTFET transistor.

This premature formation results poor characteristics such as low drive current, low transconductance (10-9S) and large contact resistances (>1MΩ) [26]. The unsatisfactory characteristics are due to the bad contacts since the carbon nanotube is just simply laid on the gold electrodes and held weakly by the van der Waals force [16]. The performance can be improved by increasing the gate capacitance by reducing the insulator thickness or increasing the dielectric constant. However, the calculation for gate capacitance of CNFET is different from MOSFET. The introduction of Al2O3 layer on top of patterned Al gate is able to lower the gate voltage and increases the transconductance [24]. Further improvement is followed by the inauguration of top-gated structure. It is needed that each CNFET to be gated individually in order to have a complex integrated circuit.

2.3.3 Top-gated CNFET:

The next generation of CNFET came in top-gated structure to improve the device performance. Since the performance in back-gated structure is rated quite poor in terms of the device operation, thus this new structure is expected to bring better result. This structure is fabricated by dispersing the carbon nanotube on an oxidised wafer [16]. Atomic force microscopy (AFM) image is used to identify the single carbon nanotube and then the source and drain terminals, which made of Ti, are fabricated on top of the carbon nanotube. A 15-20nm gate dielectric film is deposited at 300°C through chemical vapour deposition (CVD) process. Finally, a 50-nm-thick gate electrode is patterned by lithography. Figure 2.9 depicts the structure of top-gated CNFET.

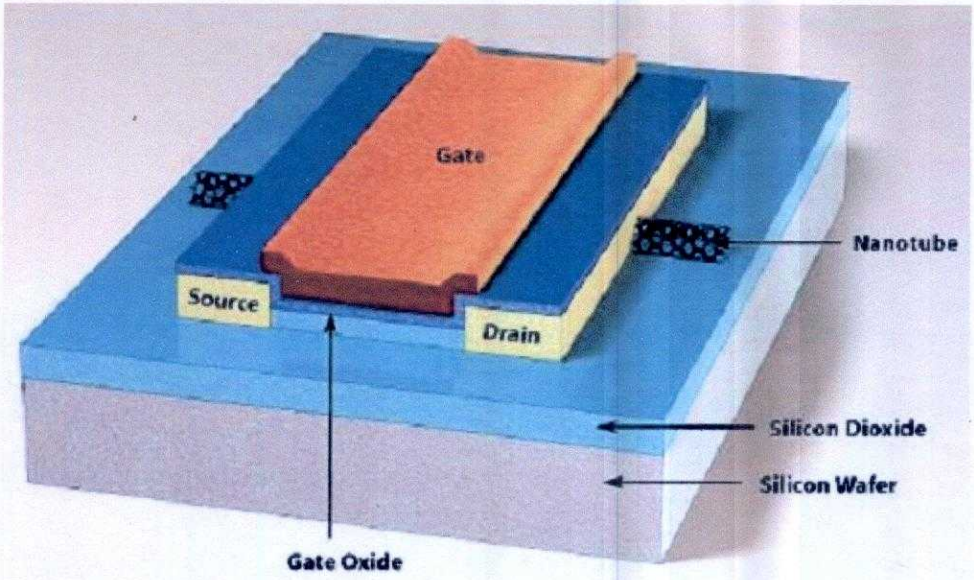


Fig: 2.9: Structure of Top-gated CNTFET.

This structure gives better out-turn than early structure. The improvement comes from the scaling of the dimension and the adoption of better device geometry as well as the device performance [33]. For example, the electrical field is increased due to the device geometry and contact resistance is reduced by choosing a suitable of contact material. Besides, the threshold voltage is significantly lower than back-gated structure, drive current is much higher and transconductance is similarly high (3.35μS per nanotube).

2.3.4 Vertical CNFET:

The latest development in CNFET progress could be the initiation of vertical CNFET. This structure with surround-gated is suggested by Choi et. al. in 2004 [34]. The transistor size can be as small as the diameter of carbon nanotube which corresponds to tera-level CNFET and density of 1012 elements per cm-2. The vertical CNFET is prepared through the following steps: nano-pore formation by anodization followed by synthesizing the carbon nanotube, metal-electrode formation, oxide deposition and patterning and finally gate electrode formation. The silicon oxide was deposited at the top of aligned carbon nanotube by electron gun evaporation and followed by holes formation of e-beam patterning and chemical etching. The silicon oxide deposition process is then followed by deposition of top gate electrode. The structure of vertical CNFET is illustrated in Figure 4.10. In this structure, each carbon nanotube is electrically attached to bottom electrode, source, upper electrode (drain) and gate electrode is put around the carbon nanotube. Each cross point of source and drain electrodes corresponds to a transistor element with a single vertical carbon nanotube. The number of carbon nanotube in transistor depends on the hole-diameter of gate oxide. The vertical CNFET allows higher packing densities that can be achieved since source and drain areas can be arranged on top of each other [24]. On the other hand, real 3-D structures can be made possible because the active devices are no longer bound to the surface of mono-crystalline silicon wafer.

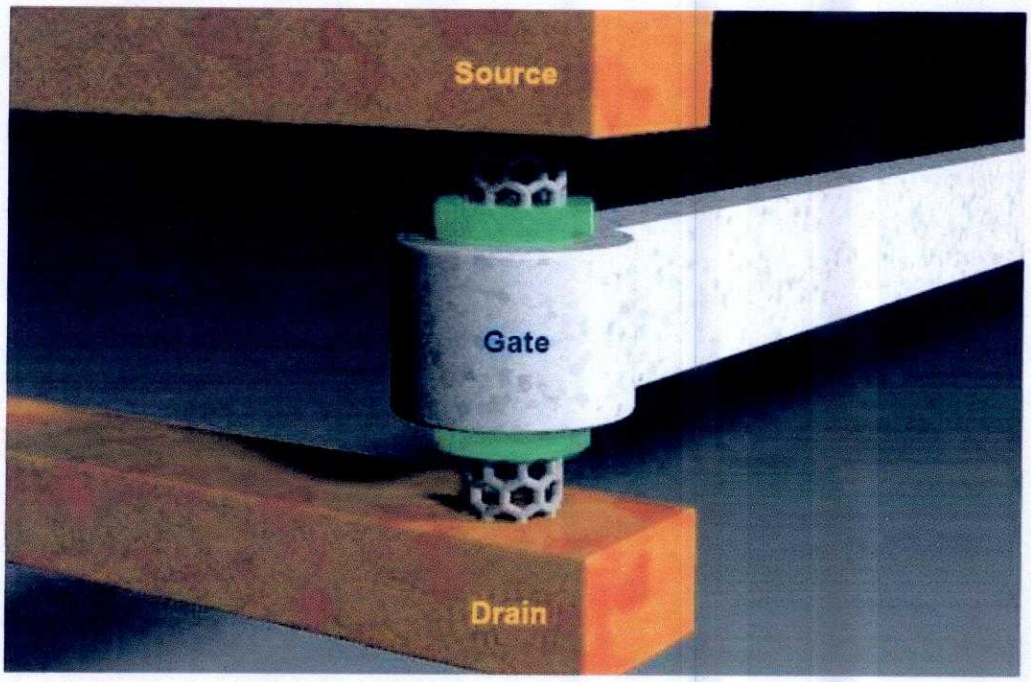


Fig 2.10: Structure of Vertical CNTFET.

2.3.5 Operation of CNFET:

Basic principle operation of CNFET is the same as MOSFET where electrons are supplied by source terminal and drain terminal will collect these electrons. In other words, current is actually flowing from drain to source terminal. Gate terminal controls current intensity in the transistor channel and the transistor is in off state if no gate voltage is applied. In this section, the operation of two different structures is discussed. The first structure is known as Schottky-barrier CNFET and the other one is MOSFET-like CNFET. The structure between these two CNFET is only slightly different but results in different transistor operation.

- **Schottky-barrier CNFET:**
  Normally, a potential barrier known as Schottky barrier (SB) exists at every contact between metal and semiconductor. The barrier height is determined by the filling of metal-induced gap states. These states become available in the energy gap of semiconductor due to interface formed with the metal. The SB is controlled by the difference of the local work functions of the metal and the carbon nanotube. SB is also extremely sensitive to changes of local environment at the contact [35]. For example, gas adsorption changes the work function of metal surfaces. Since this device employs metal as its source/drain terminals and has Schottky barrier at its terminal contact between nanotube and metal, therefore it is called Schottky-barrier CNFET (SB-CNFET). Diagram of SB-CNFET is shown in Figure 2.11 below.

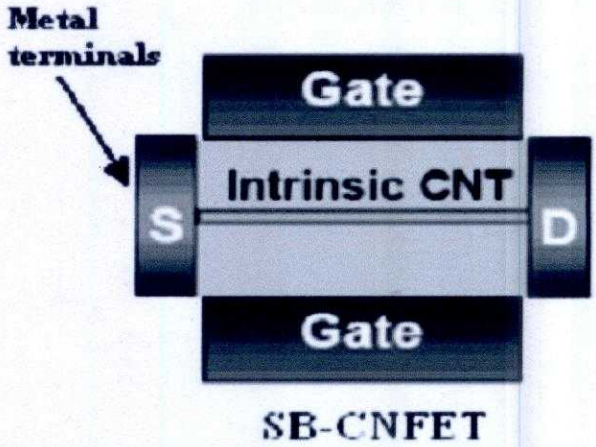


Fig 2.11: Diagram of a SB-CNTFET.

SB-CNFET works on the principle of direct tunneling through the Schottky barrier at the source-channel junction. The barrier width is controlled by the gate voltage and hence the transconductance of the device depends on the gate voltage. At low gate bias, large barrier limits the current in the channel. As gate bias is increased, it reduces the barrier width, which increases quantum mechanical tunneling through the barrier, and therefore increases current flow in transistor channel. In SB-CNFET, the transistor action occurs by modulating the transmission coefficient of the device.

SB-CNFET shows very strong ambipolar conduction particularly when the gate oxide thickness is reduced even the Schottky barrier is zero [36]. This type of conduction causes leakage current to increase exponentially with supply voltage especially when the nanotube diameter is large, which results in limiting device potential. Thus, ambipolar conduction must be reduced in order to improve the performance of SB-CNFET. One of the solutions is to increase the gate oxide thickness. If the gate oxide thickness is high, there is no ambipolar conduction exists when Schottky barrier is zero. Hence, the leakage current is reduced and as a result, the transistor performance is improved. Another alternative is to build asymmetric gate oxide, which is has been proposed recently, in order to suppress the ambipolar conduction [37].

Another issue regarding on SB-CNFET is that this type of transistor suffers from metal-induced-gap states which limit minimum channel length and thus increases source to drain tunneling. SB-CNFET is also unable to place gate terminal close to source because it can increase parasitic capacitance.

- **MOSFET-Like CNFET:**

The structure of this device is slightly different than SB-CNFET since it used heavily doped terminals instead of metal. This device is formed in order to overcome problems in SB-CNFET by operating like normal MOSFET. Unlike SB-CNFET, source and drain terminals are heavily doped like MOSFET and hence it is called as MOSFET-like CNFET. This device, as shown in Figure 2.11, operates on the

principle of modulation the barrier height by gate voltage application. The drain current is controlled by number of charge that is induced in the channel by gate terminal.

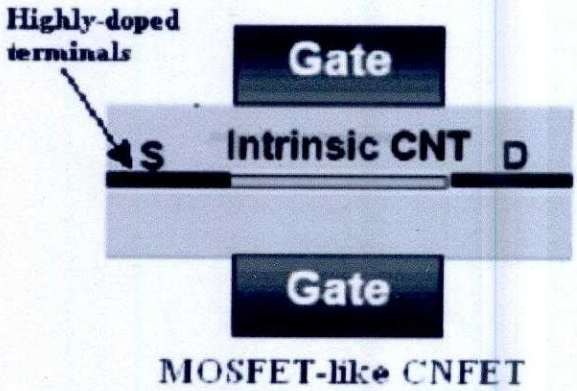


Fig 2.11: MOSFET- like CNTFET Structure.

This type of transistor has several advantages over SB-CNFET. This device is able to suppress ambipolar conduction in SB-CNFET. It also provides longer channel length limit because the density of metal-induced-gap-states is significantly reduced. Parasitic capacitance between gate and source terminal is greatly reduced and thus allows faster operation of the transistor. Faster operation can be achieved since length between gate and source/drain terminals can be separated by the length of source to drain, which reduces parasitic capacitance and transistor delay metric. It operates like SB-CNFET with negative Schottky barrier height during on-state condition and thus it delivers higher on-current than SB-CNFET. Previous work has shown that this type of device gives higher on-current compared to SB-CNFET and therefore it can justify the upper limit of CNFET performance. Based on the device performance, it is obvious that this device can be used to investigate the ballistic transport in CNFET.

2.3.6 P-type versus N-type CNFET:

CNFET are typically p-type, which means they are modulating current in the channel when negative gate voltage is applied to the device. For p-type operation, when negative gate voltage is applied, it will conduct current in the channel from source to drain and this current is due to holes movement. In contrast, an n-type CNFET conducts whenever a positive gate voltage is applied to the device, which is the current flow in the channel from source to drain is due to the conduction of electrons. In short, CNFET delivers current either a positive or negative gate voltage is applied. This characteristic, allowing both holes and electrons conduction in the same device, is called ambipolar characteristic. Thus, CNFET is an ambipolar device since it conducts current either in negative or positive supply voltage. Normally, when CNT is used to produce CNFET without any further processing, the devices are invariably p-type. Thus, in order to produce n-type CNFET, another process is needed. There are two ways of producing n-type CNFET from p-type CNFET. The conversion process can be made possible either annealing or doping process.

Annealing is a process of converting p-type CNFET into n-type CNFET through vacuum annealing. In this process, p-type CNFET is heated under vacuum to desorb any adsorbed gas such as oxygen and at the end of this process, the p-type CNFET is converted into n-type CNFET. This conversion process is reversible because if n-type CNFET is exposed to air, the device will return to its original p-type characteristic. The process of annealing is graphically shown in Figure 2.12 below.

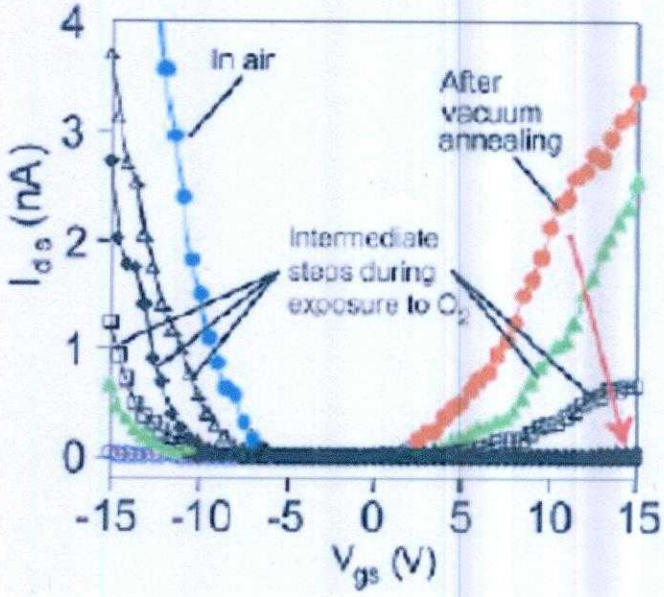


Fig 2.12: Characterization of CNTFET due to annealing process [10].

Another process is called doping process, which the p-type CNFET is doped using electron donors such as alkali metals is depicted in Figure 4.9. Alkali metals, such as potassium, will give the same result as in annealing process with p-type CNFET is transformed into n-type CNFET. Conversion process from p-type to n-type and vice versa is very important especially to develop nanotube complementary logic circuits. Since both p-type and n-type CNFET are needed to build complementary logic circuits, thus this conversion process gives a solution to build nanotube-based logic circuit.

2.4 Summery:

From this chapter we studied the limitation of conventional Si-MOSFET, properties of carbon nanotube, different types of carbon nanotube, and a brief discussion on Carbon nanotube based field effect transistor. And we found the performance properties of the transistor are given a higher performance properties compared to conventional properties. Each type transistor is modeled in difference way based on the structure of the transistor. This discussion includes different types of CNTFET from starting CNT technology, operation of CNTFET and types of CNTFET based on this operation. So this chapter tries to include small basic regarding CNTFET.

Chapter 3

RESULTS AND CHARACTERIZATIONS OF CNTFET USING MATLAB SIMULATION

This is the core chapter of our whole research work and it will explain the methodology used in this project, simulation model used for simulation study, simulation result obtained, comparing those results with other reliable research group's results and finally making summery, analysis and discussion on the result.

3.1 The Model

This research implicates simulation based study to investigate the effect on I-V characteristic by changing different parameters of CNTFET. This MATLAB based simulation study is carried out based on surface-potential model described by Rahman *et al.* [31]. Based on this analytical model I-V characteristics of CNTFET can easily describe. The model is build for MOSFET-like structure in order to investigate ballistic transport in CNTFET since this structure is proved experimentally that it could achieve near ballistic transport [31]. Our goal is to modify the MATLAB code such a way that we can investigate the effect on I-V characteristics by changing major parameters of CNTFET and we also focused our result on 3D plot along with three different views so that very small change can also be identified.

3.1.1 Model Physics and the Process of Calculation:

The analysis starts at the top of the energy barrier since current remains the same throughout the channel and all scattering mechanism is neglected. At any specified drain/gate voltage, the drain current is calculated based on the total charge that occupied first subband in the nanotube. The process is repeated for all drain/gate voltage in the specified range before all the drain current values are plotted within a single graph. The model for ballistic CNFET consists of three capacitors, which represents three transistor terminals on potentials at top of barrier. As shown in Fig. 3.1, the shaded circular region indicates mobile charge at top of the barrier. The mobile charge is determined by the local density of states at top of the barrier, location of source and drain levels, E_{F1} and E_{F2}, and self-consistent potential at top of the barrier, U_{scf} [31] [10].

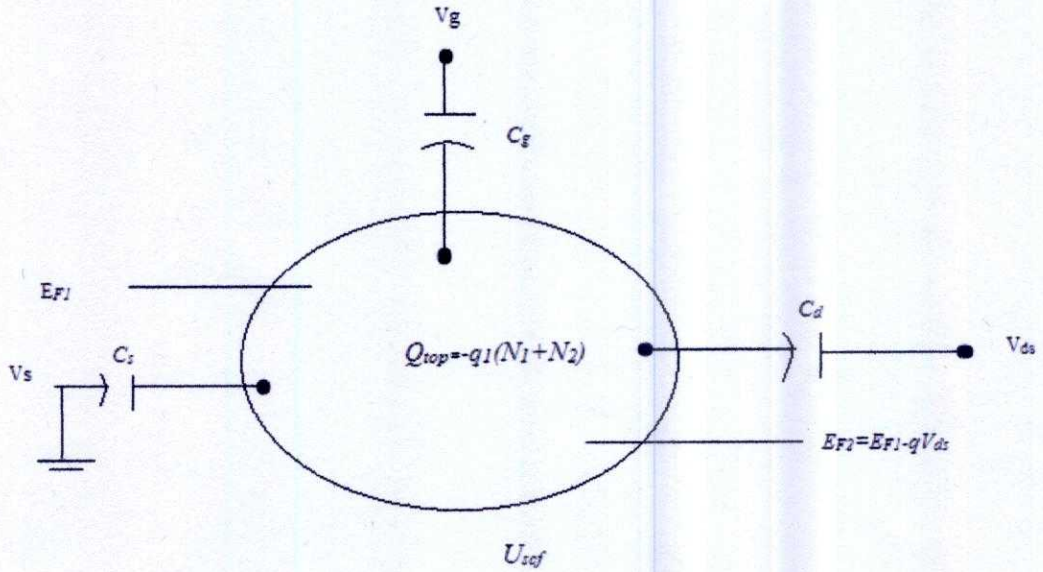


Fig 3.1: Simulation model for ballistic CNTFET

Steps of calculating the drain current summarized from Rahman *et al*:

i) Consider a value of V_G, VD, VS and EF1. For simplicity, V_S is grounded as potential reference.

ii) Compute the total charge on nanotube channel. The charge at top of the barrier contributed from source and drain are given as

$$N_1 = \frac{D(E)}{2}\int_{-\infty}^{\infty} f\left(E + U_{scf} - E_{F1}\right)dE$$

$$N_2 = \frac{D(E)}{2}\int_{-\infty}^{\infty} f\left(E + U_{scf} - E_{F2}\right)dE$$

Where, N_1 represents positive velocity states filled by source and N_2 represents negative velocity states filling by drain, $E_{F1(F2)}$ is the source (drain) Fermi level, $f(E)$ is the probability that a state with energy E is occupied (Fermi-Dirac probability), D(E) is the nanotube density of states (DOS) at top of the barrier and U_{scf} is self-consistent potential at the top of the barrier. For simplicity, assume source Fermi level as the reference, thus $E_{F1} = 0$ and $E_{F2} = -qV_{DS}$ where q is electronic charge.

iii) Uscf must be evaluated in order to solve for charge density at top of the barrier. Uscf can be solved by using superposition. First, Laplace potential is calculated using the following equation:

$$U_L = -q\left(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S\right)$$

Where,

$$\alpha_G = \frac{C_G}{C_\Sigma}, \alpha_D = \frac{C_D}{C_\Sigma}, \alpha_S = \frac{C_S}{C_\Sigma}$$

Now, potential due to mobile charge calculated as

$$U_P = \frac{q^2}{C_\Sigma}(N_1 + N_2) - N_0$$

Where,

$$N_0 = \int_{-\infty}^{\infty} D(E) f(E - E_F) dE$$

Now, U_{scf} can be found by adding U_L and U_P:

$$U_{scf} = U_L + U_P$$
$$= -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + \frac{q^2}{C_\Sigma}(N_1 + N_2) - N_0$$

iv) Now, Drain current can be computed by using following formula:

$$I_D = \frac{4qk_B T}{h}\left[\ln\left(1 + \exp\left(E_{F1} - U_{scf}\right)\right) - \ln\left(1 + \exp\left(E_{F2} - U_{scf}\right)\right)\right]$$

Where, k_B is Boltzmann constant, T is operating temperature and h is Planck's constant.

v) By repeating step (i)-(iv) for a set of (V_G, V_D) points, the I_D (V_G, V_D) characteristics can be determined.

Detail discussion about the physics and mathematical calculation of Rahman *et al.* modeling is provided in Appendix B. Table 3.1 describes the total calculation procedure that we have done in our MATLAB simulation. In our modeling there is option of choosing particular parameter by maintaining other parameter set as default or giving other value to observe effect on I-V characteristics. The unique part of our simulation code is anyone observe parameter changing effect over a range of value at a time whereas in Rahman *et al* modeling only one set of figure can observe at a time and if anyone ones to see the effect over a range of value than code have to be simulated several times which is not time consuming and sometimes leads to error. We also maintain chirality effect in our simulation method so that the effect of changing diameter over chiral axis can also be observed.

Table 3.1: Detail simulation procedures and corresponding parameter of our MATLAB simulation.

Input parameters:	***List of values (Physical parameters):***
Gate insulator thickness t (m); " " Dielectric constant (€); Tube diameter (d); Temperature (T); Number of bias point (NV); Initial voltage (V_i); Final „ (V_f); Source Fermi level (E_f)eV; Gate control parameter alphag (α_g); Drain control parameter alphad (α_d); Chiral axis(n,m);	q (Electron charge): $1.6 * 10^{-19}$ C T: 300k Boltzmann constant K_b: $1.3* 10^{-23}$ j/k K: 8.62*10^-5 (ev/k) Plank constant h: 6.63*10^-34 ħ(hbar) :1.05*10^-34(ev-s) (Permittivity of free space)$€_0$: $8.85*10^{-12}$ (Relative permittivity of dielectric cons.)€:3.9 C-C bond length (a_{c-c}): 1.42*10^-10 Oxide thickness(Default) t= 1.5*10^-9 No. of bias point NV(Default)= 11 Range (VI-Vf) :(0-1) v (Fermi level for source) (Default)E_f=-0.32 v α_g (Default)= .88 α_d(Default) = .035 C-C bond energy: (Default) 3ev
Equations : **1.Calculating Diameter:** $d=a(m^2+mn+n^2)^{.5}/pi$ **2. Calculating Thermal voltage** : KT= K_bT/q **3. Calculating Sum of capacitor :** $C_{ins} =2pi€€_0/log\ (2t/d)$ $C_{sum} = C_{ins}/\alpha_g$ **5. Calculating Charging energy :** $U_0 =q^2 / C_{sum}$ **6. Calculating Density of states:** *DOS* : $D_0 = 8/(3 * pi * a_{c-c} * bonding\ energy)$ **7.Band gap:,** $E_g= 2* a_{c-c} * bonding\ energy/\ tube\ diameter(d)$ **8.Electron concentration of the top of barrier :** N_0 (called N_CNT) N_0 = N_CNT system : ***Step 1***: E_{lim} : $max\ [10*kT, (8*KT + E_f)] + E_g/2$ ***Step 2***: $Z_{lim} = [E_{lim}^2 - (E_g/2)^2]^{.5}$ ***Step3***: Z_i : 0+ ((Zlim -0)/1000)i; whereas 0<=i<=1000; ***Step 4***: $f_{zi} = 1/[1 + (e(Z_i^2 + (E_g/2)^2)^{.5}) - E_g/2 - E_f)/KT]$ ***Step 5***: $N_0 = D_0 (\sum(i=0\ to\ 1000) f_{zi}) * \Delta z$	**9.Calculating Current:** $I_o = (2 * q * k_b * ħ / 2 * pi)$ $mu_1 = E_f$; $mu_2 = mu_1 - v_d$ **Laplace potential:** $U_L = - q\ (\alpha_g * v_g + \alpha_d * v_d + \alpha_s * v_s)$; $[\alpha_g = C_g / C_{sum}, \alpha_d = C_d / C_{sum}, \alpha_s = C_s / C_{sum}]$ **Potential due to mobile charge:** $U_p = Q^2 * \Delta N / C_{sum}$ **Self-consistence potential:** $U_{scf} = U_L + U_p$ $\Delta N = N\_CNT\ (D_0/2, E_g, KT, mu_1 - U_{scf}) + N\_CNT\ (D_0/2, E_g, KT, mu_2 - U_{scf}) - N_0$ **Fermi Flag:** $Fermi\_flag\ 1 = log(1 + e^x)$ $Fermi\_flag\ 0 = e^{\infty}$ I_{temp1}: $log(1+e^{(eta1)})$; $Fermi\_flag=1$ $e^{(eta1)}$; $Fermi\_flag=0$ $[eta1 = (mu_1 - U_{scf}) / KT]$ I_{temp2} $log(1+e^{(eta2)})$; $Fermi\_flag=1$ $e^{(eta2)}$; $Fermi\_flag=0$ $[eta2 = (mu_2 - U_{scf}) / KT]$ ➢ $I = I_o * [I_{temp1} - I_{temp2}] * 10^6$

The flowchart of overall simulation process of our simulator is given bellow:

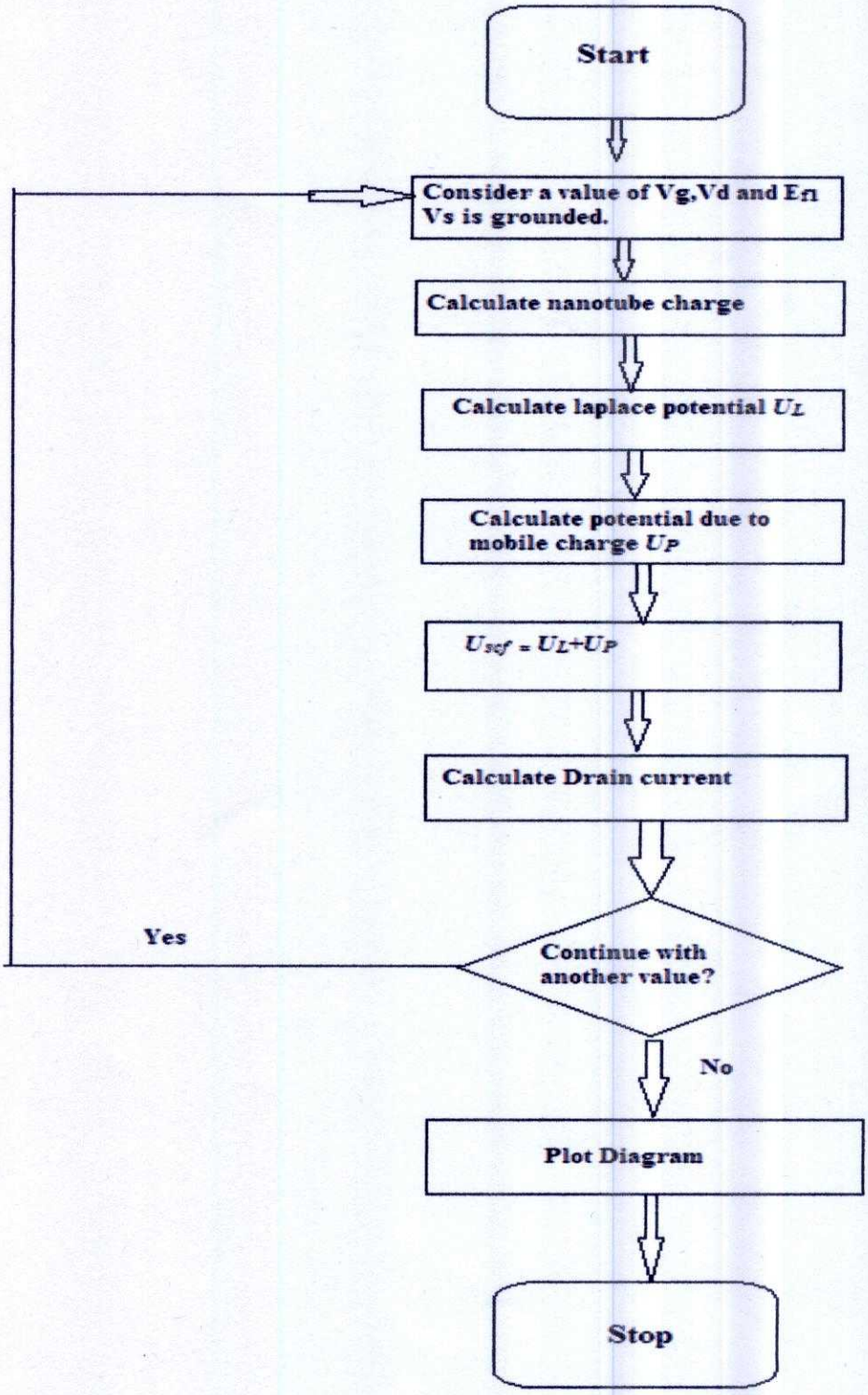


Fig3.2: Flowchart of theoretical simulation process from Rahman *et al.*

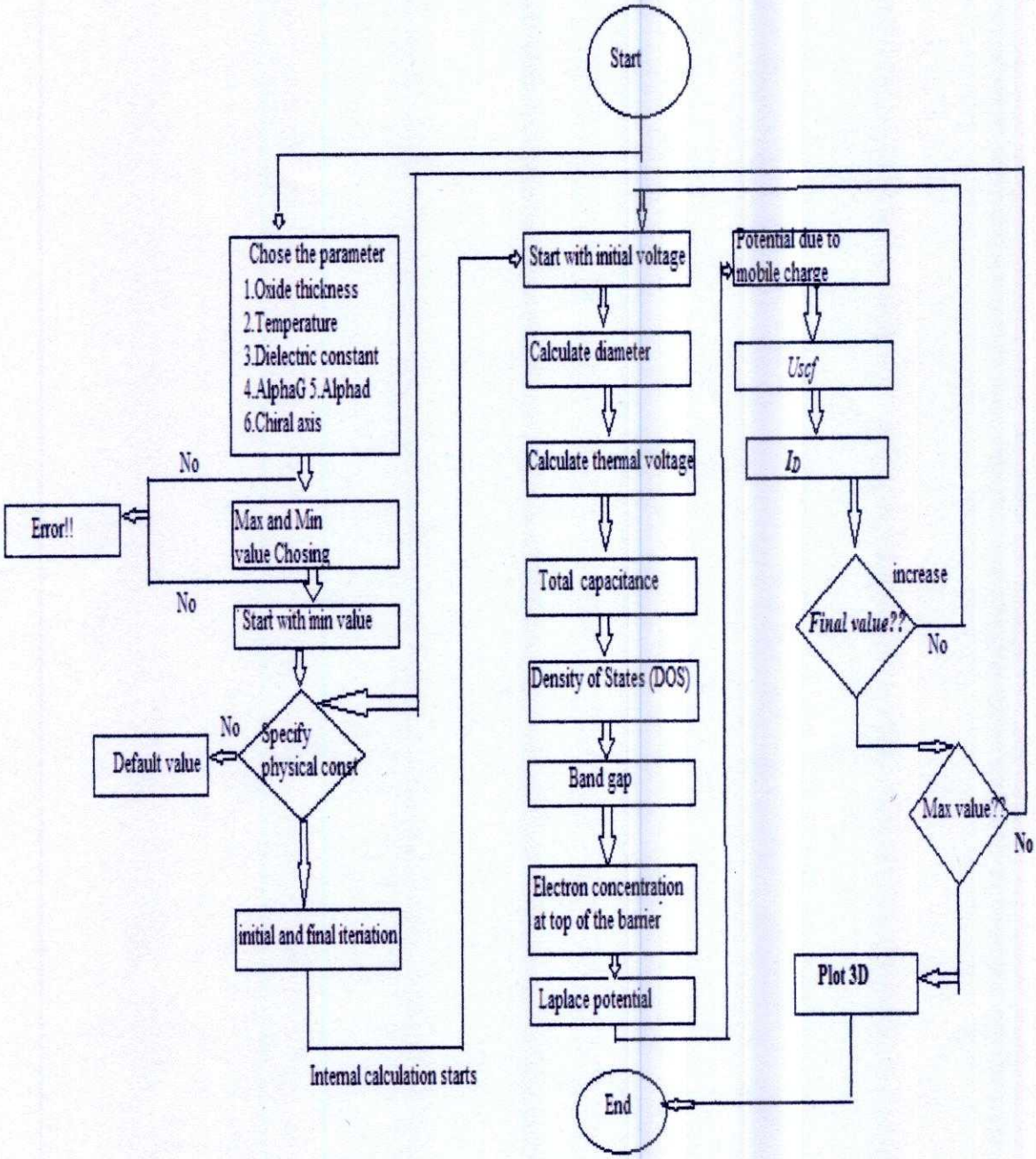


Fig 3.3: Flow chart of our new MATLAB simulation operation based on the physics of Rahman *et al.*

3.2 Results and Analysis:

From the simulation we got different parameter changing effect on I-V characteristics of CNTFET. There are seven results obtained and each result has individual effect on CNTFET. We started with gate oxide thickness and gradually improved our work by identifying temperature effect, dielectric constant effect, gate and drain control parameter effect and also chirality changing effect on Carbon nanotube based field effect transistor. The CNTFET structure we considered for our simulation is MOSFET-like ballistic CNTFET is drawn in figure .

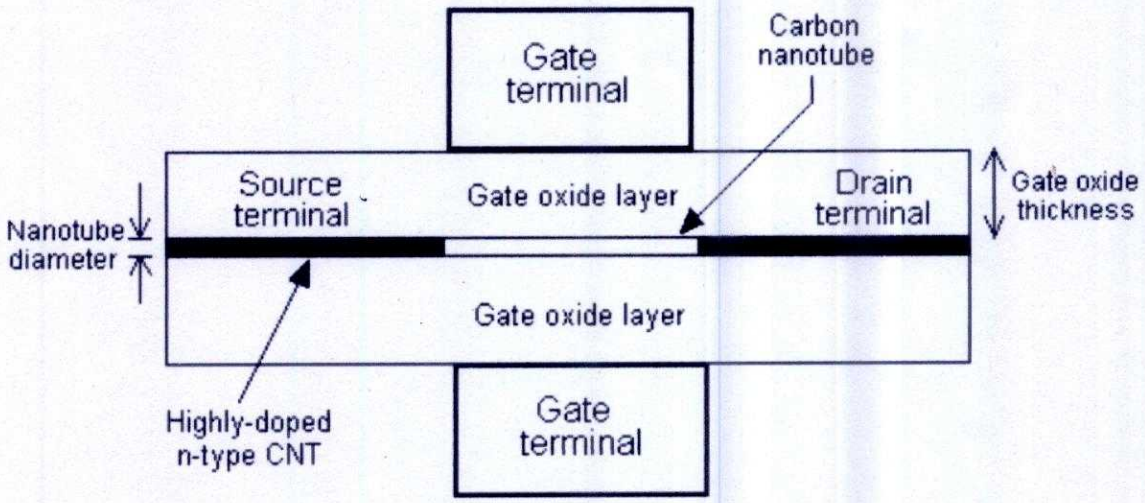
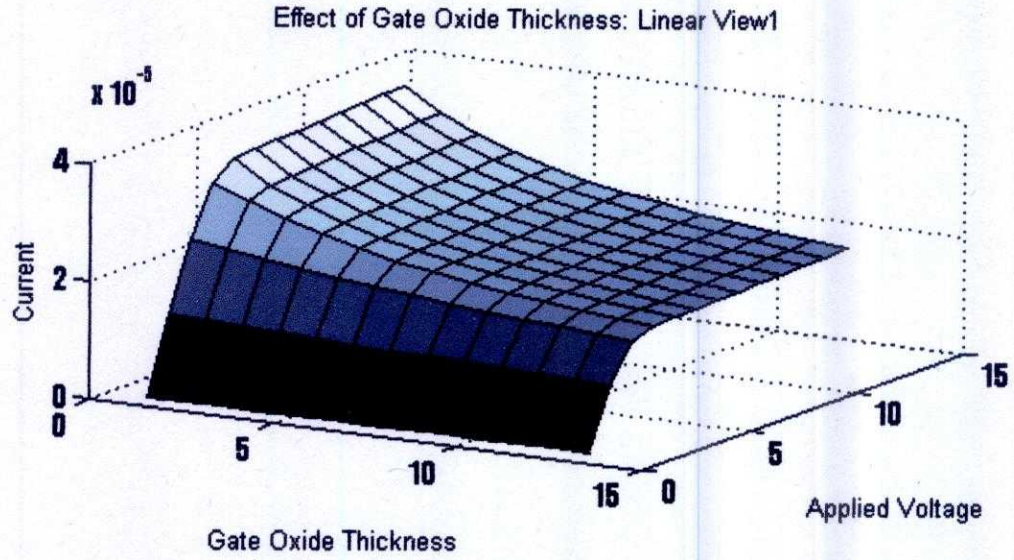
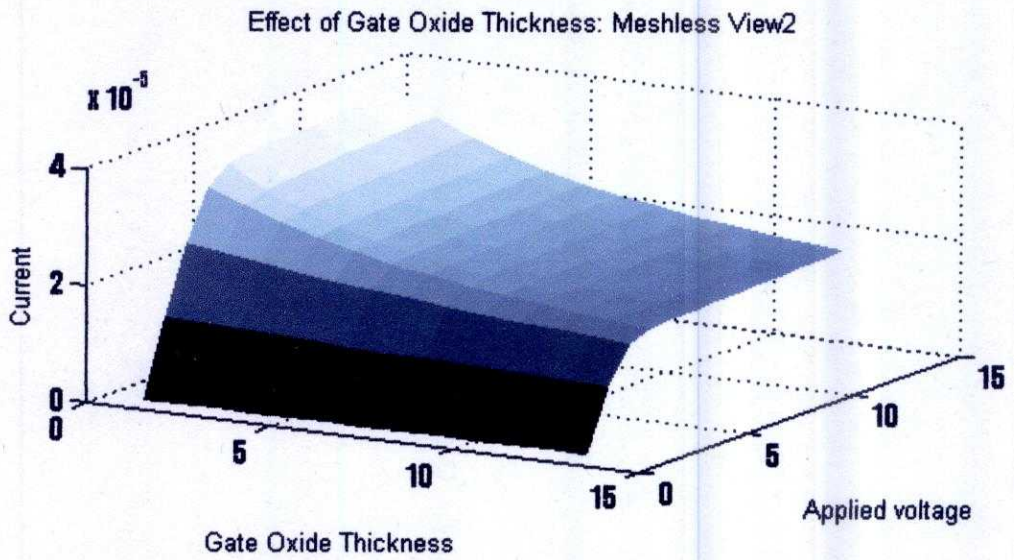


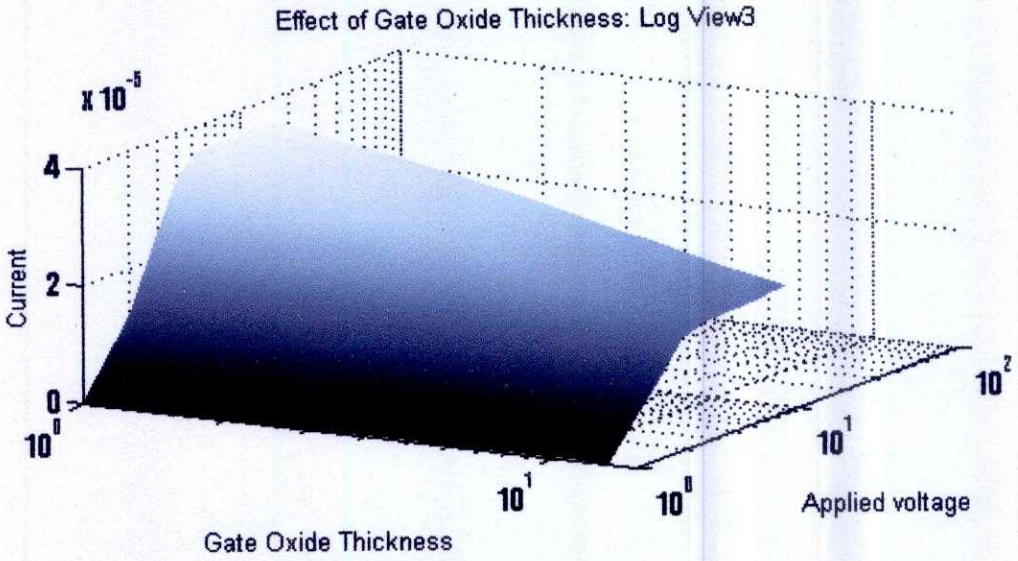
Fig 3.2: Structure of Ballistic CNTFET.

3.2.1 Effect of Gate Oxide thickness:

Gate oxide thickness has strong effect on CNT transistor performance. In our result analysis part, at first we are going to observe gate oxide thickness changing effect. We change the oxide thickness from 1nm to 4nm and perform the simulation by keeping other parameters constant of default value. In that simulation part diameter was kept 1.1084nm (13,0) though out the calculation and other parameter value like temperature was 300K, source Fermi level was -0.32, gate and drain control coefficient was 0.88 and 0.035 and finally dielectric constant was 3.9. Output characteristic is shown in figure 5.5. The output is showing three different 3D view for better understanding, initial one is linear 3D view, after that there is without mesh and finally a logarithmic view. From the following figure we can visualize that there is a linear changing of output current characteristics with respect to oxide thickness. We took 12 different gate oxide thickness values using intermediate difference of 0.25nm each. Here 1nm has the largest amount of current which is near about 3.75×10^{-5}. After that it is gradually decreasing with every increment of gate oxide thickness. At the end for 4nm oxide the current decreases significantly which is 1.8×10^{-5}. Based of the output characteristic, the thinner oxide (1nm oxide thickness) will provide better I_D gain compared to the 4nm oxide thickness transistor. Another trade-off from this experiment is thinner oxide transistor will have high leakage current compared to the transistor which have thicker oxide


Effect of Gate Oxide Thickness: Linear View1
x 10^-5
4
2
0
Current
0
5
10
15
Gate Oxide Thickness
0
5
10
15
Applied Voltage


Effect of Gate Oxide Thickness: Meshless View2
x 10^-5
4
2
0
Current
0
5
10
15
Gate Oxide Thickness
0
5
10
15
Applied voltage



3D View1(shading faceted)
3D View2(shading flat)
3D View3(shading interp)
"Current is inversely proportional to Gate Oxide Thickness"

Fig 3.5: Gate oxide Thickness changing effect on Carbon Nanotube field effect Transistor.

In conventional MOSFET, the gate oxide thickness has already entered the nanometer range; channel scattering from the rough oxide interface and tunneling through the thin oxide are becoming prevalent problems [32]. Carbon nanotube transistors do not have these difficulties; all chemical bonds are satisfied in a carbon nanotube and thus, there is less oxide to channel interface problem. A multitude of oxide can be placed on the nanotube and thus, many high-k dielectrics can be incorporated into CNTFET to reduce the tunneling current [32].

The accuracy of our result can be proved by comparing other research group work which is identical. Gate oxide thickness effect was also observed by Heng Chin Chuan which result is given bellow (Fig: 5.6) and the result is close enough to ours. Another simulation was carried out by Rahmat Bin Sanudin [10] which is provided in Fig: 5.7. His targeted value is 1nm to 2.5 nm and the obtained results support our simulation results from which we can also summarize that lower oxide thickness contains more on current. According to Rahmat Bin Sanudin the level of leakage current, I_{OFF}, is not considerably affected by gate oxide thickness [10]. Therefore, we can conclude that the I_{ON}/I_{OFF} ratio will increase as the gate oxide thickness is reduced. So, at the end considering all the discussion we can say that on-current is inversely proportional to gate oxide thickness.

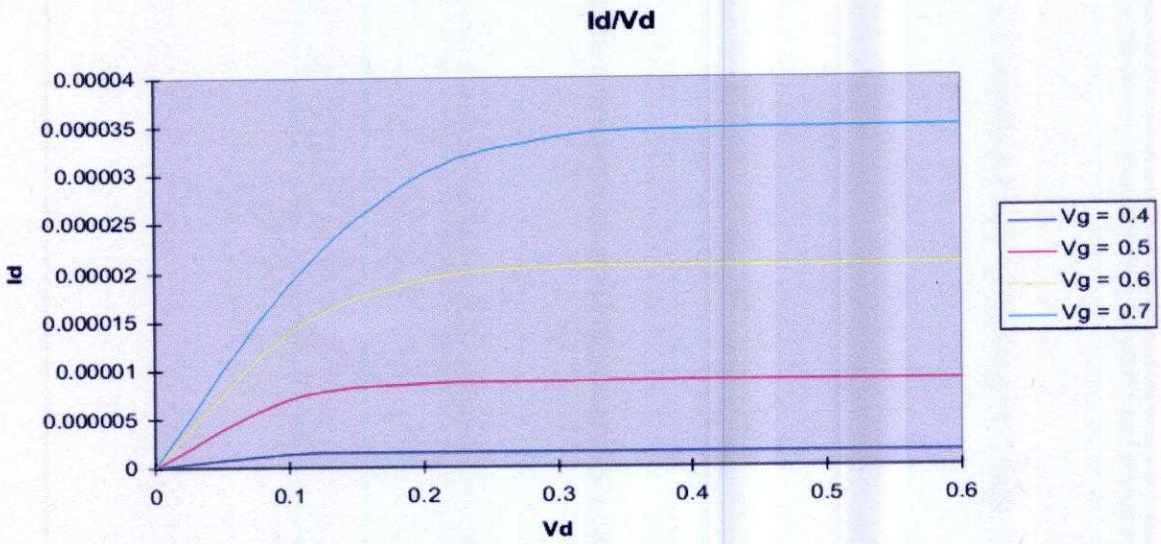


Fig3.6: Analysis of oxide thickness changing effect by Heng Chin Chuan (result for 2nm) [32].

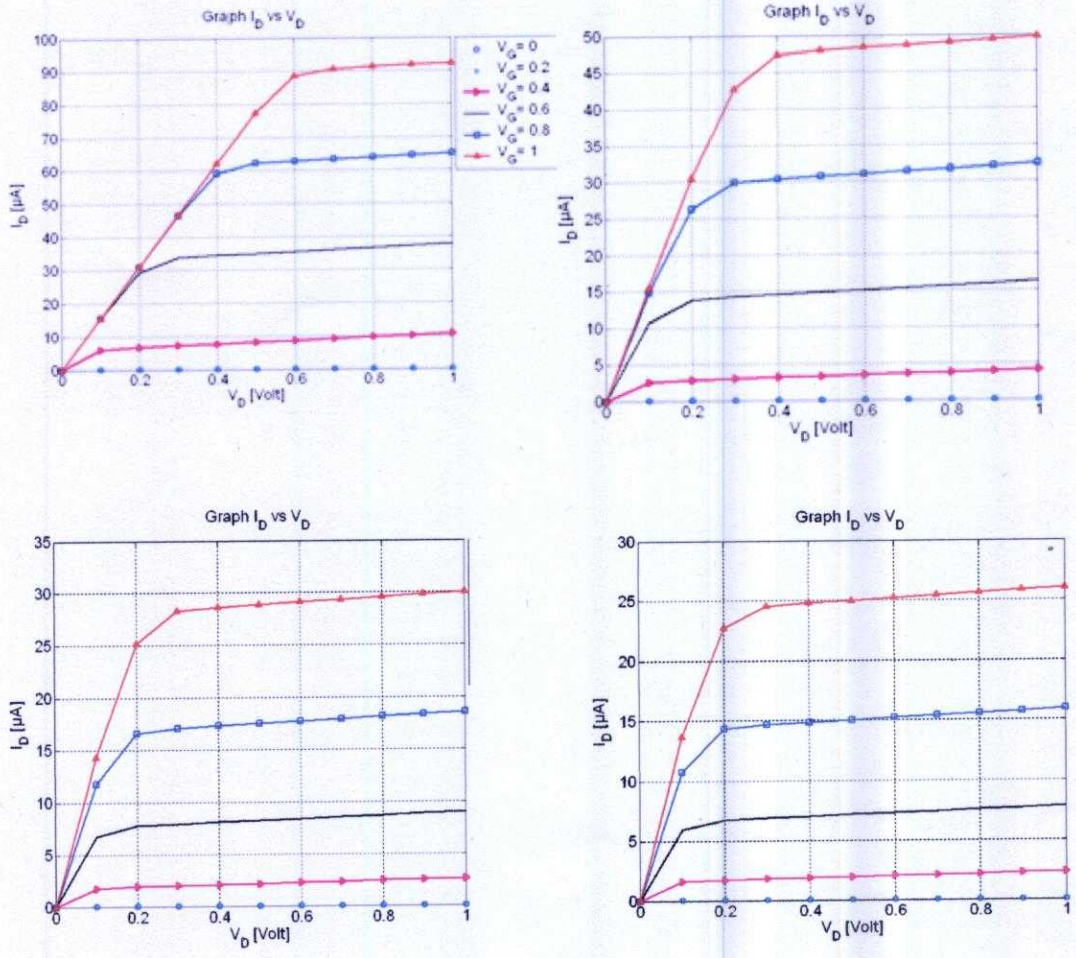


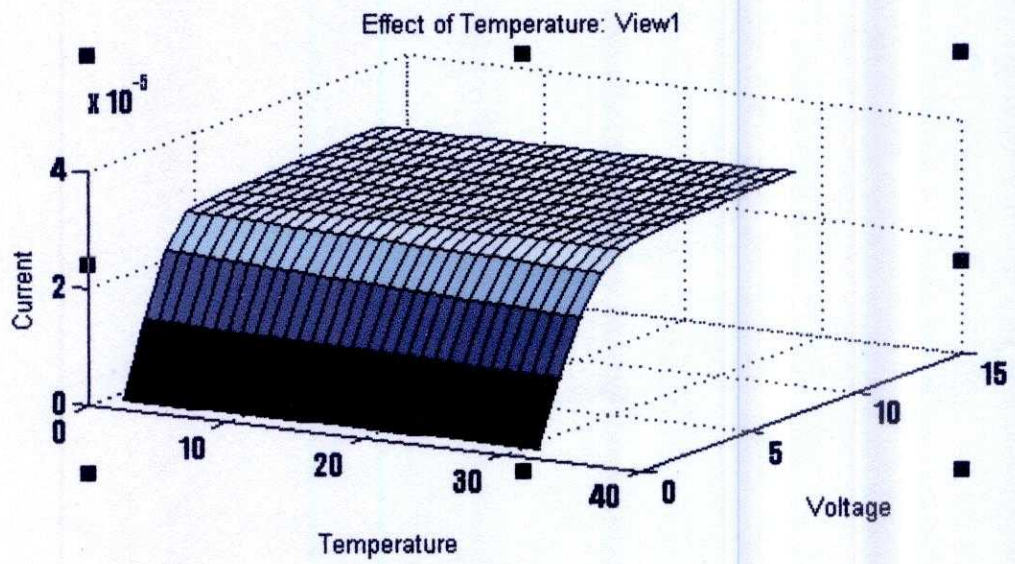
Fig 3.7: Gate Oxide thickness effect observation by Rahmat Bin Sanudin [10].

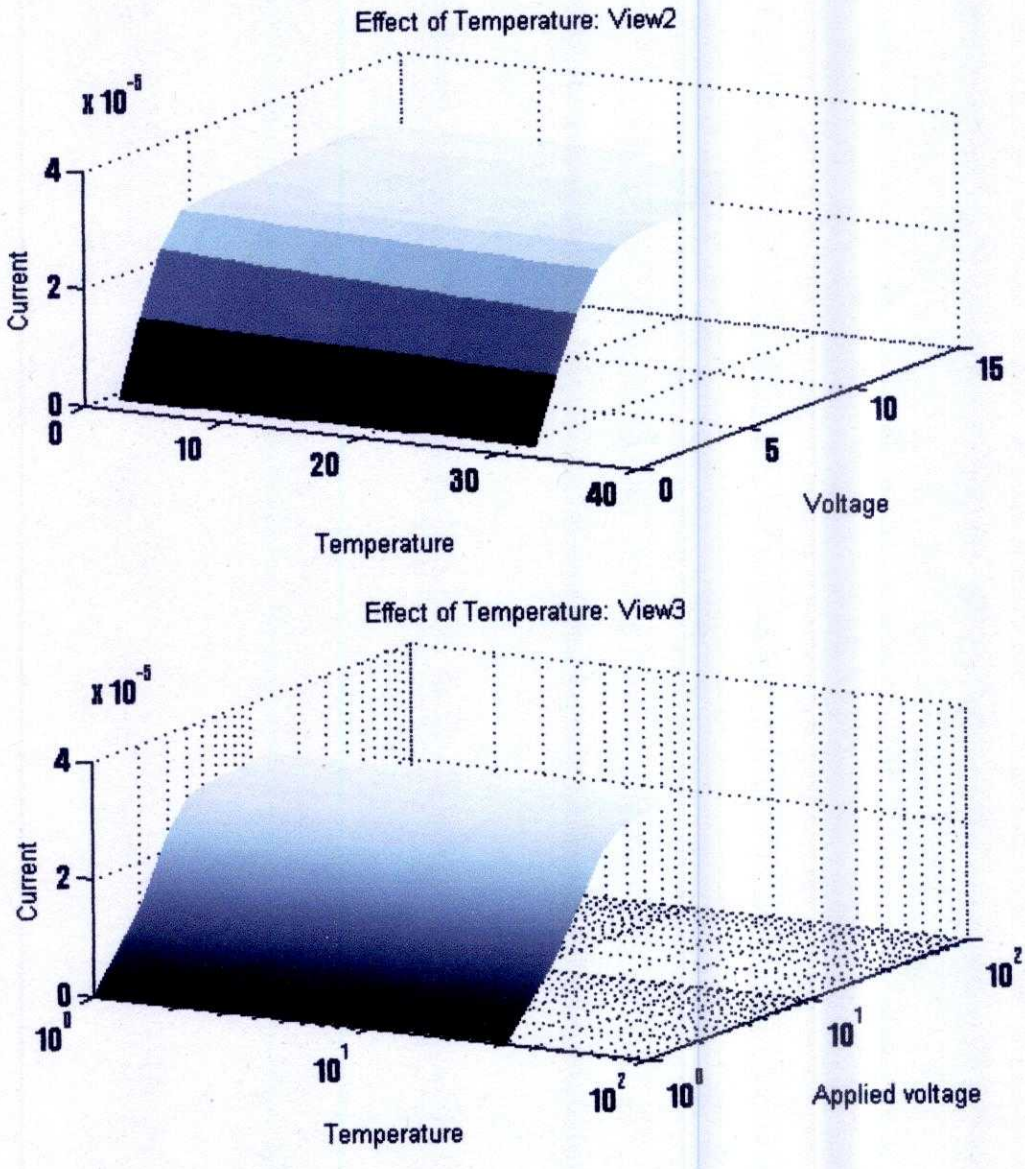
3.2.2 Effect of Temperature:

Now our concern is in temperature changing effect on carbon nanotube FET output. Figure: 3.8 deals with the temperature changing effect. We take our temperature range from 250K to 550K by keeping other parameter constant. In that case we considered gate oxide thickness 1.5nm which was the subject of changing in our previous experiment. From the figure we can observe very negligible change in output characteristics for temperature changing effect. Due to ballistic consideration temperature changing effect is reduced in the channel current. But still there is a small effect on drain current due to temperature increase which is also seen in Ali Naderi *et al.* observation [33]. It is seen (Fig: 3.7,3.9) at high temperature (550K) drain current is little bit higher than at the low temperature drain current.

But according to Ali Naderi *et al*, by increasing the gate source voltage, at low drain source voltages, for higher temperature in fig.3.8 (500 K) the drain current is less than lower temperature (250 K). So, gate source voltage has vital effect in order to change drain current along with temperature. From Ali Naderi *et al* in the saturation region by increasing the gate source voltage the drain current difference between high and low temperature reduces. It is evident from the figure: 3.9 that the drain current in the saturation region and $V_{GS} = 0.8$ for 250 K and 500 K are approximately equal and this result can also see in our result fig: 5.7. So there is small increment in on state current with the increase of temperature.

According to the Ali Naderi *et al* although on-state current increase with the increasing of temperature, the off-state leakage current grows much faster than the on-state current. But this result is not in our concern in this research.





3D View1(shading faceted)
3D View2(shading flat)
3d View3(shading interp)
"Ballistic consideration reduce Temperature changing effect"

Fig 3.7: Temperature changing effect on Carbon Nanotube Field effect Transistor.

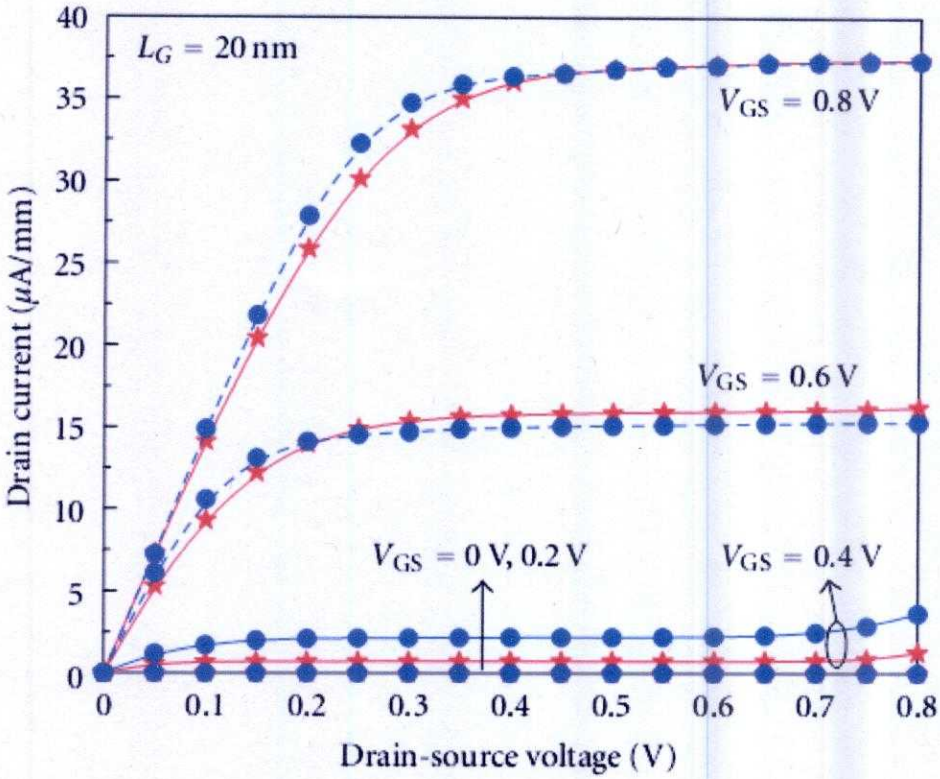


Figure 3.8: Comparison of output Characteristics of CNTFET in 250K and 500K in different gate voltage by Ali Naderi *et al* [33].

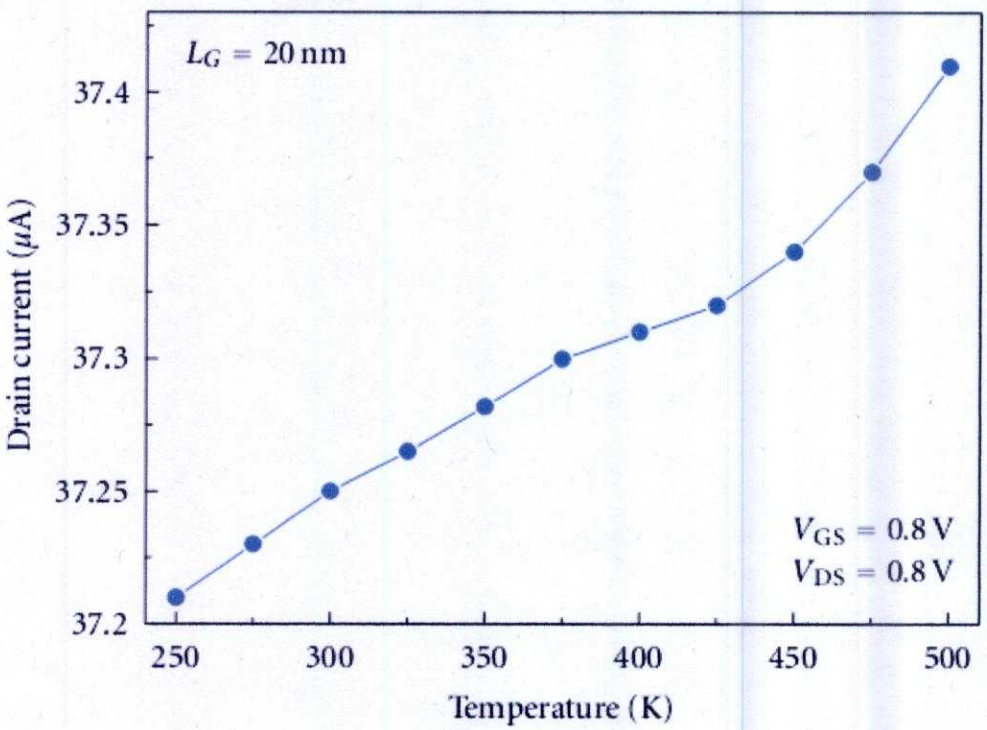
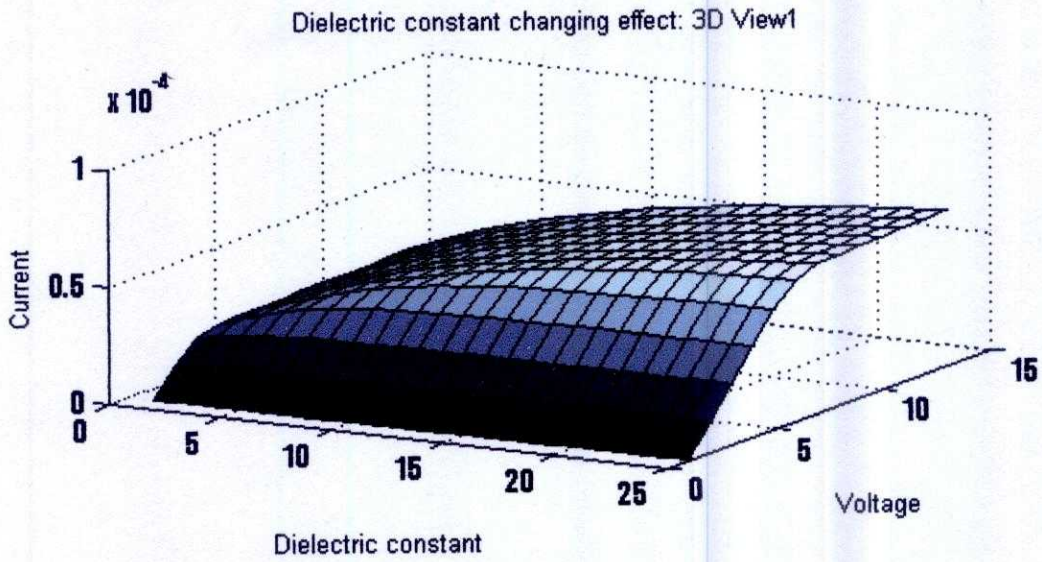


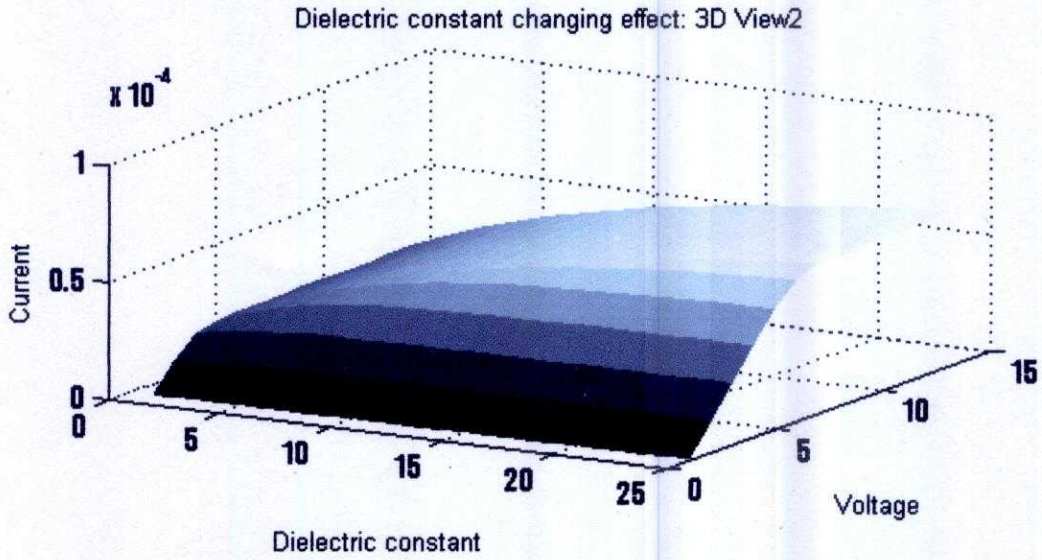
Fig 3.8: Small change in I_D by Temperature increasing which satisfy our simulation result.

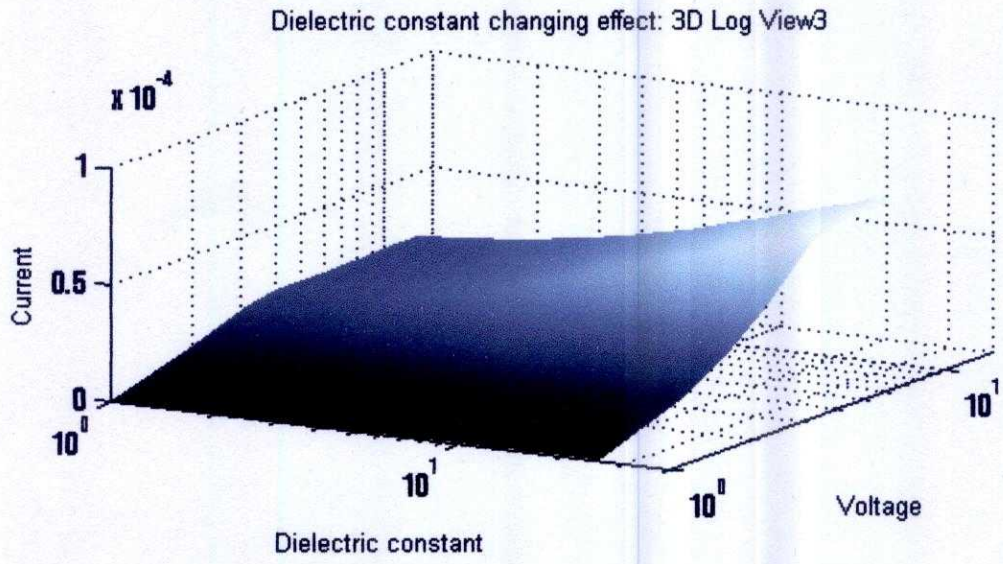
3.2.3 Dielectric Constant Changing effect:

At this stage of our report now our concern is to investigate the result effect CNTFET output by changing the dielectric constant. Naturally SiO_2 is used as a gate oxide material which has a dielectric constant of 3.9. But other material can be used as an oxide material for better performance. At this case dielectric constant will change definitely.

Because of scaling, bulk Si MOSFET suffers from many limitations like short channel effect, tunneling etc. as we said before in chapter 2. To overcome these limitations many solutions were proposed by different researchers. Use of high dielectric material as gate insulator was one of the proposed solutions [34]. Keeping this in eye we have tried to see the effect of using different dielectric materials as gate insulator in CNTFET. In this case we change our dielectric constant within a range of 3 to 15 and interval is 0.5 keeping other parameter constant as usual. At this inspect we kept our temperature at 300K which was a subject of change in our previous experiment. From figure 3.9 we can easily observe that changing of dielectric constant has vital effect on output current. It is clear from the plot is that the saturation current increases for increasing dielectric constant but degree of this positive effect reduces as we go for higher dielectric material . This means that as we are going for higher and higher dielectric material the increment in I_D with respect to k reduces. This result also match with the result of Rasmita Sahoo *et al* Fig: 3.10.







View1(shading faceted)
View2(shading flat)
View3(shading interp)
"Current increasing with increasing Dielectric Constant"

Fig 3.9: Dielectric constant changing effect on CNTFET output.

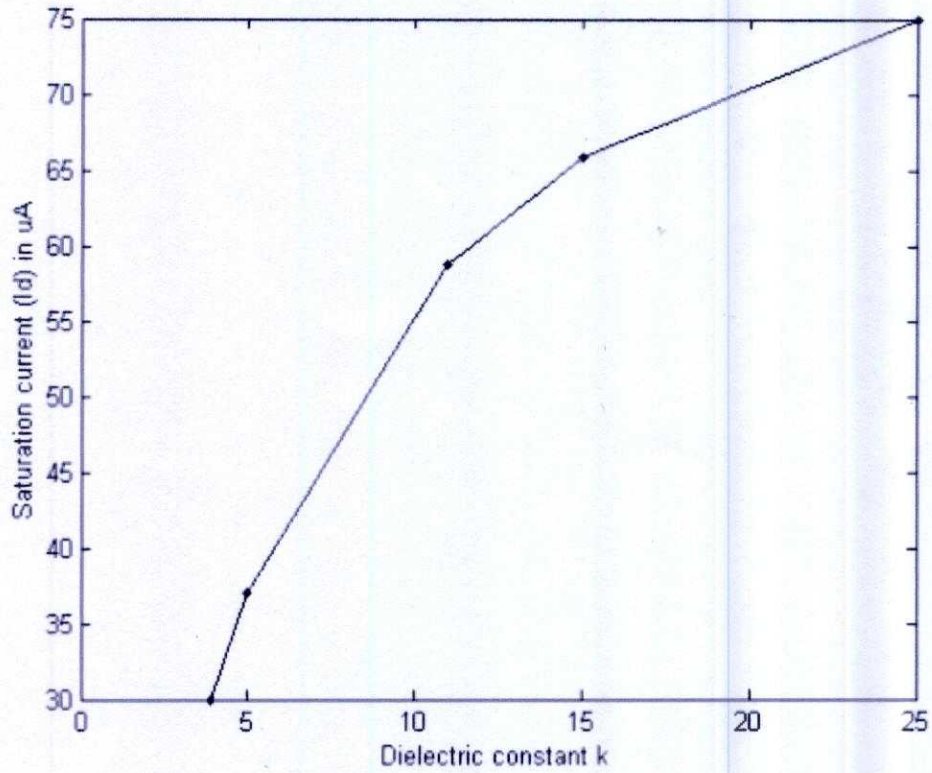


Fig 3.10: Dielectric constant changing effect investigated by Rasmita Sahoo *et al* which satisfied our simulation result [35].

3.2.4 Chirality Changing Effect:

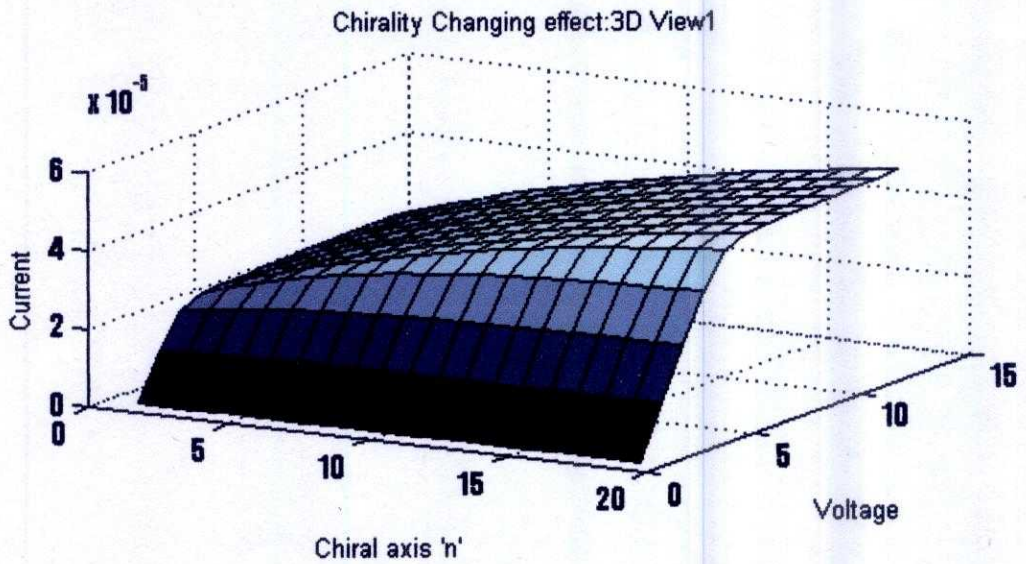
In this section we are going to discuss and important parameter changing effect on CNTFET which is chirality. Actually chirality relates with the diameter and diameter changing effect is very important for FET. That's why chirality changing effect is very important for any Carbon Nanotube based design. The equation that relates chirality and diameter is:

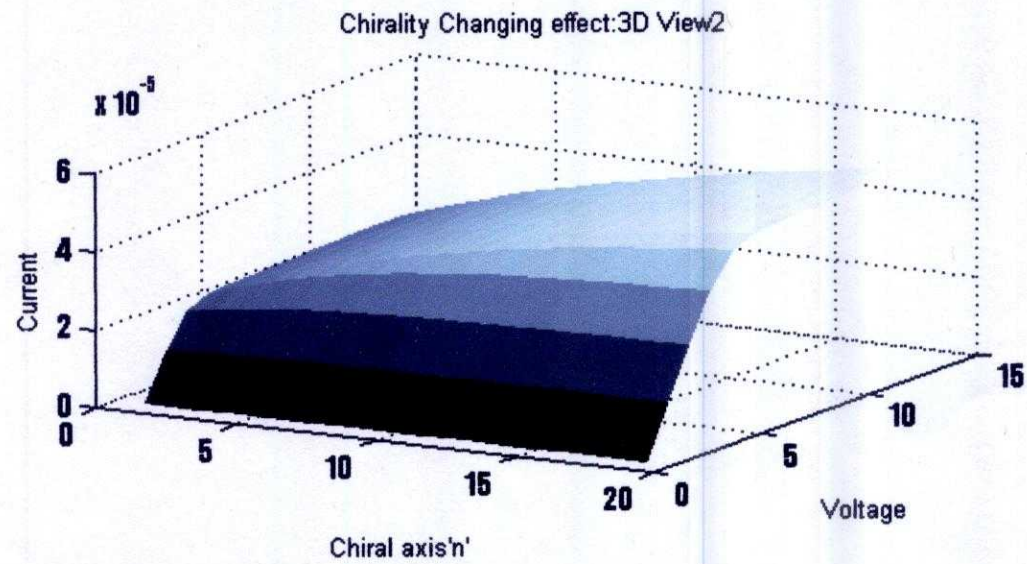
$$d=a\,(m^2+mn+n^2)^{.5}/pi$$

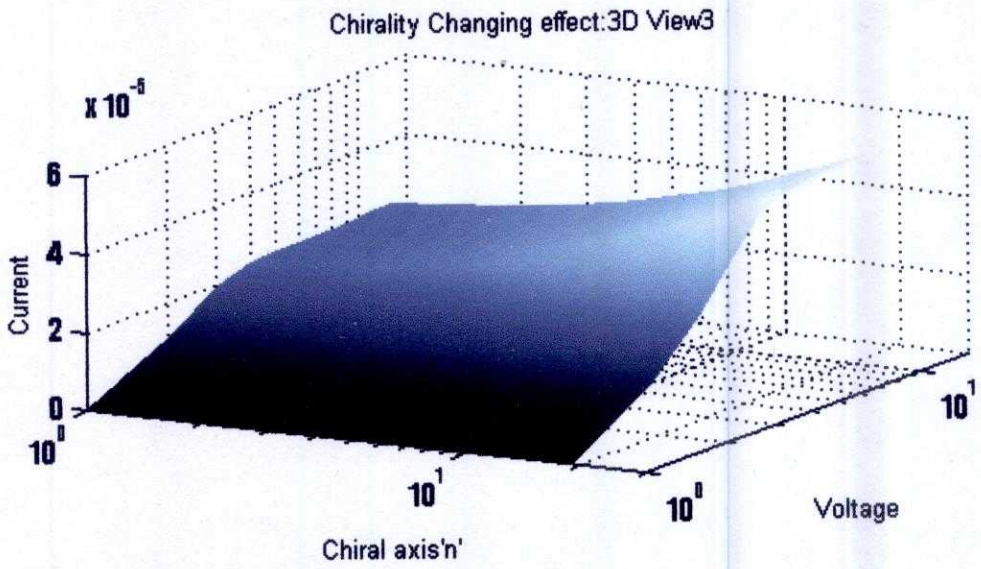
Where, m and n is the chiral axis (n, m). Here n should be always greater than m.

The energy bandgap of the CNT is inversely proportional to the nanotube diameter *(Egap α 1/Diameter)*. Since the drain current of CNFET is dependent on the total charge that filled up the first subband, therefore it is possible that the drain current too depends on the diameter of CNT [10]. So ultimately the drain current depends on the chirality. In this experiment we will observe two chiral axis changing effect that is m and n. When we are changing n we will keep m value constant and the range of n value should such a value that is always greater than m value. Similarly we will keep n value constant and make change to the m value to observe the effect on output. Other parameter will maintain their default value as like previous experiment.

When one of the chiral axis of CNT increases than the diameter is also increasing from above equation resulting large diameter nanotube (smaller energy bandgap) the threshold voltage will be reached sooner and be smaller in magnitude. So current will increase gradually. In the figure: 3.11 the range of n is taken from 10 to 28 and m remain 0 for all the cases. In figure 3.12 the range of m value is taken from 0 to 11 which are lower than the default value of n and the n value is kept constant though out the total calculation. Fig: 3.12 also demonstrate the same result as for fig: 3.11 which mean current is increasing with the increasing of m value but comparatively lower rate.

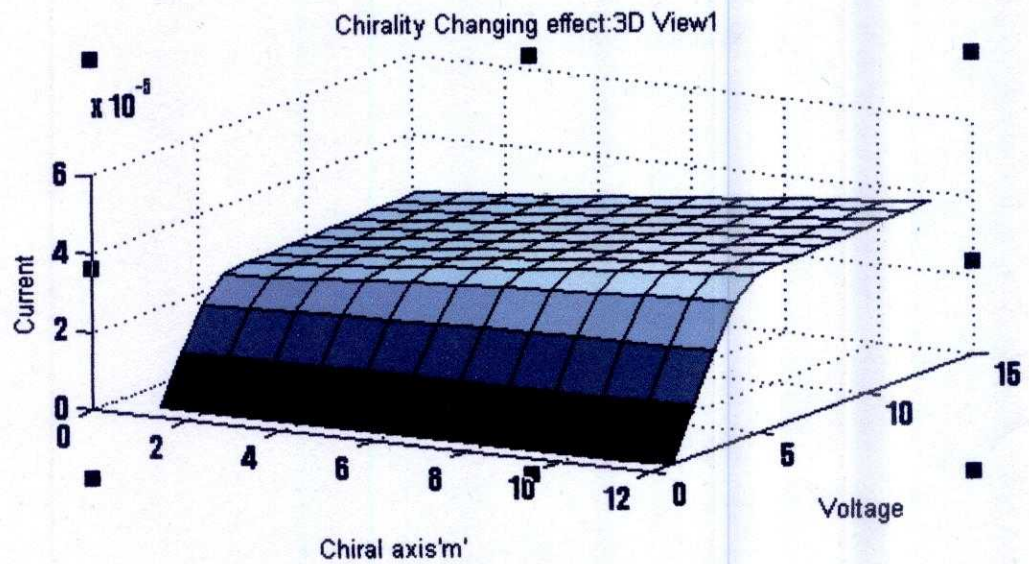


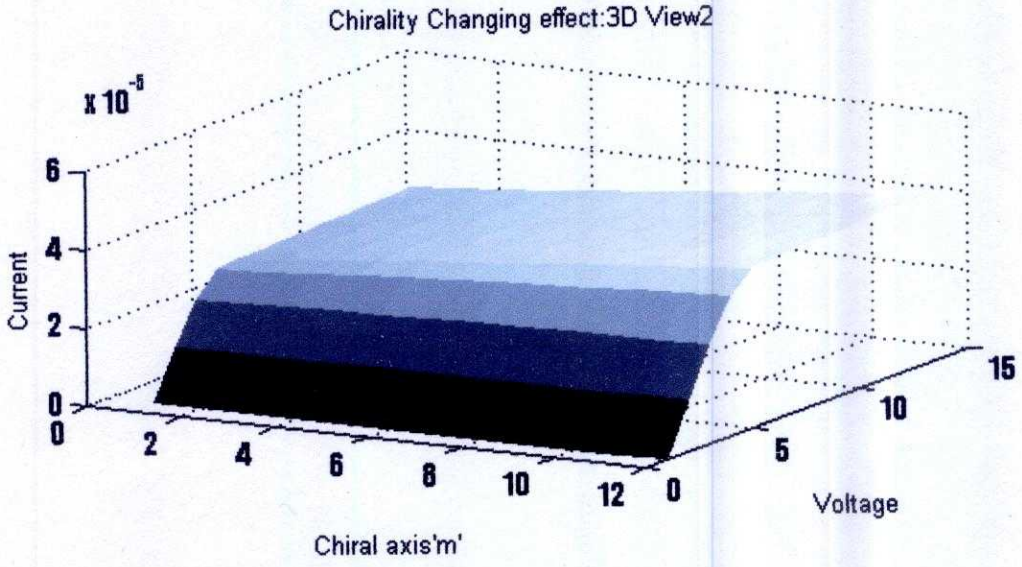


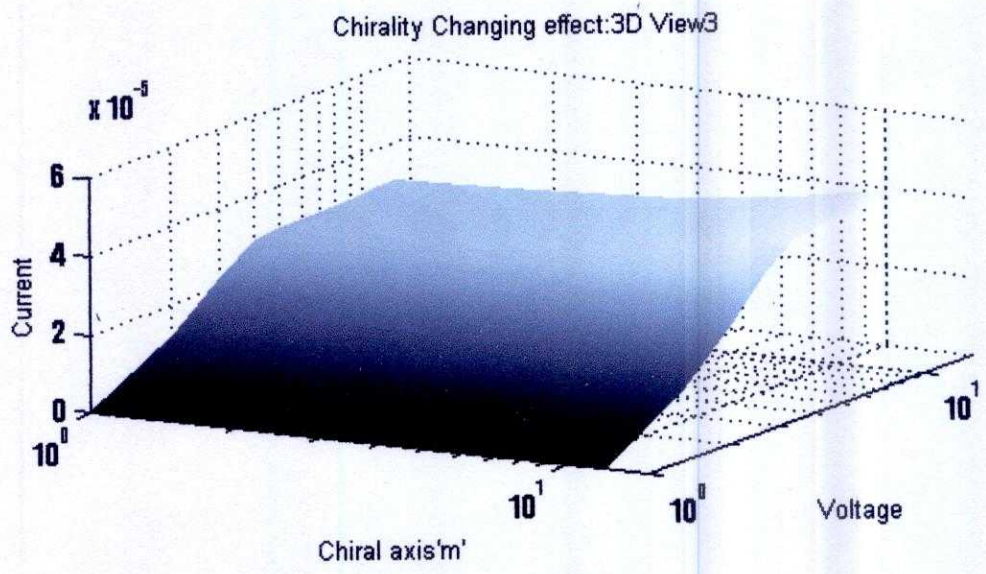


sD View1(shading faceted)
sD View2(shading flat)
sD View3(shading interp)
"Increasing Chiral axis increase the diameter resulting increase Current"

Fig: 3.11: Chirality changing (n axis) effect on output characteristics.







3D View1(shading faceted)
3D View2(shading flat)
3D View3(shading interp)
"Increasing Chiral axis increase the diameter resulting increase Current"

Fig 3.12: Chirality (axis 'm') changing effect on output CNTFET.

Based on above discussion we can say that the chiral axis is directly proportional to the diameter and analyzing above figure it can be summarize that CNT diameter is directly proportional to the I_{on} current. According to the diagram I_{on} increases enormously when the chiral axis means diameter increases. In fig 5.11 for (10,0) chirality current value is 1.9×10^{-5} A, but for (28,0) chirality current value is 5.1×10^{-5} A which is much bigger than (10,0) chirality. This significant result is also shown in fig: 5.12 where for (13,0) chirality on-current value is 2.2×10^{-5} A and for the (13,11) chirality the on-current value is 3.9×10^{-5} A which is at higher rate like n axis but still it is higher enough. According to the Rahmat Bin Sanudin [10] I_{OFF} is not affected by the diameter change resulting the on-off ratio higher by higher the chiral axis. Hence, we can say that larger size of CNT will give better performance of CNFET. However, scaling issue will be a major concern if very large diameter of CNT is used in CNFET since one of the advantages of CNFET over MOSFET is that it offers smaller size of transistor. Again larger size of CNT may increase the capacitance over the contact area. Our simulation accuracy can be justified by investigating other simulation result:

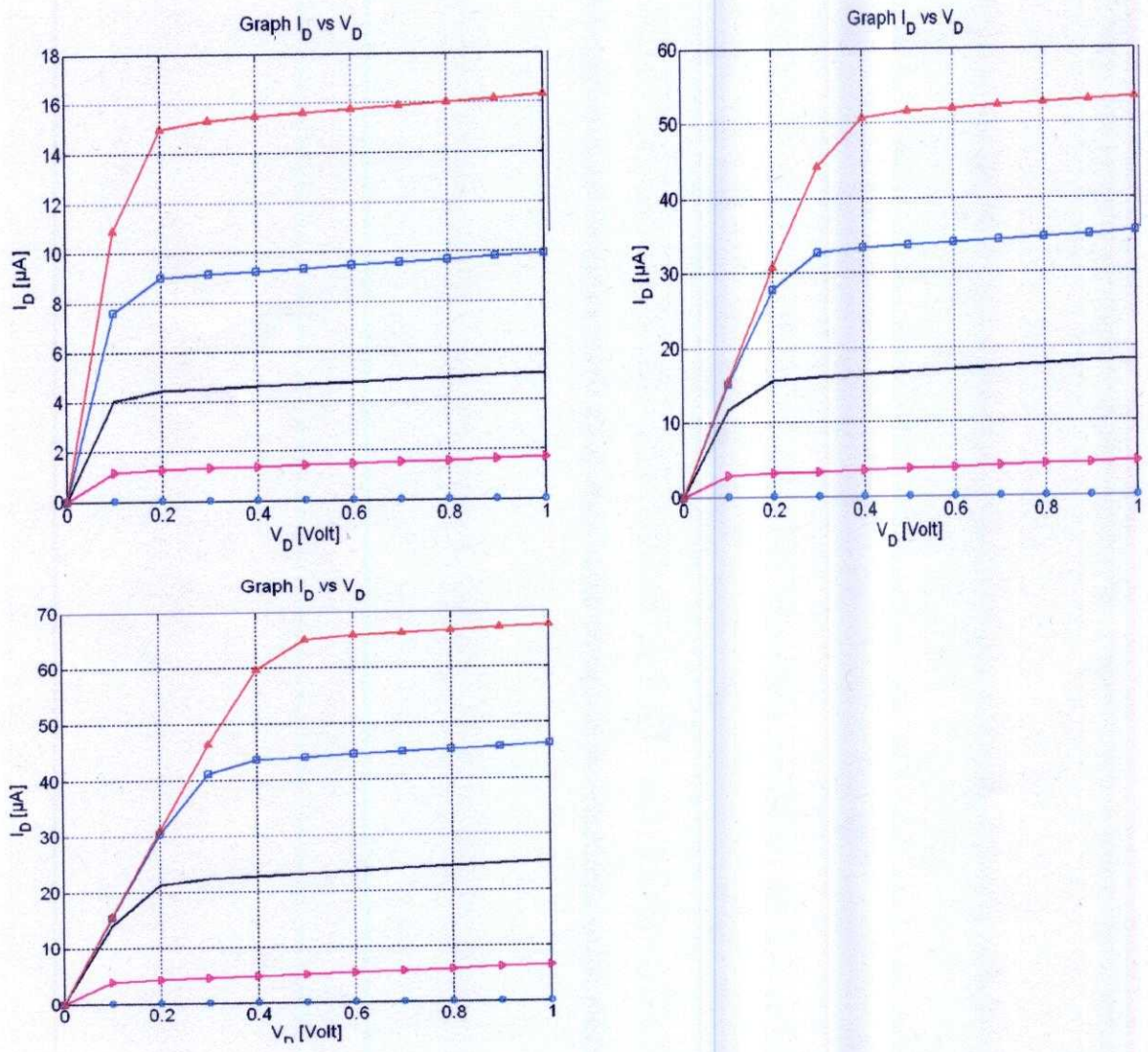


Fig 3.13: Different diameter and output effect on CNTFET by Rahmat Bin Sanudin [10].

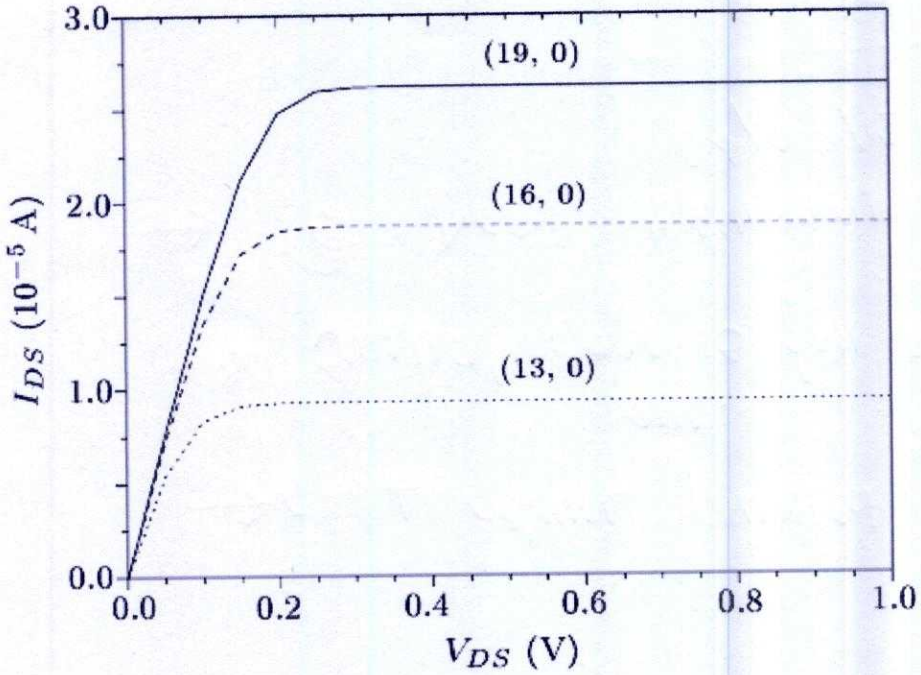


Fig: 3.14: I-V characteristics by changing Chirality by Zhao Xu *et al.* This result justifies the accuracy of our result [36].

4.1 Conclusion

Carbon nanotube (CNT) is a honeycomb tube made of graphene sheet that can grow of up to millimeters in length and the size is within nanometer scale. The size of CNT gives a possibility of making small-scale transistor and it also has unique properties that can boost the device performance such as it can growa very high current density. Depending on its chirality, CNT can have either semiconducting or metallic characteristic. Semiconducting CNT can be used as transistor channel since it has the characteristic of semiconductor whereas metallic CNT can be used as wire on circuit boards or electronic interconnections.

The main purpose of this project is to analysis the characteristic of carbon nanotube field-effect transistor (CNFET). Basically, the scheme of CNFET is almost the same as MOSFET except that the silicon channel is now being replaced by CNT. The structure of MOSFET has evolved from back-gated to top-gated and recently vertical structure has been proposed. The operation of CNFET can be seen either as Schottky barrier CNFET (SB-CNFET) or MOSFET-like CNFET. While the former structure used metal as its source/drain terminals, the latter structure used highly doped CNT as its source/drain terminals. In our project our main concern is to develop simulation from MOSFET-like CNFET. In our result part we analysis oxide effect, temperature effect, chirality effect, drain and gate control coefficient effect and also dielectric constant effect.

As a conclusion, CNFET has large potential that can be exploited to be an effective switching device. CNFET is still far to be a commercial device in electronic industry but the researchers are pushing very hard to improve its performance in order to replace MOSFET as the heart of digital applications.

4.2 Future work

Investigating the CNFET characteristics is very interesting since this device has many aspects that can be explored and improved. For future works, the comparison analysis between CNFET and MOSFET can be extended from on-off-current ratio to other parameters such as transconductance and conductance of the device. Expanding the comparison analysis will give a clearer picture of CNFET performance over MOSFET. Besides, since the outcome of simulation analysis in this project is totally based on ideal condition of CNFET, an experimental work including the fabrication process of CNFET will provide more realistic result.

1. D. Jiménez, X. Cartoixà, E. Miranda, J. Suñé, F. A. Chaves, and S. Roche, ***"A simple drain current model for Schottky-barrier carbon nanotube field effect transistors"***.
2. Heng Chin Chuan, ***"Modeling and Analysis of Ballistic Carbon Nanotube Field Effect Transistor (CNTFET) with Quantum Transport Concept"*** MAY 2007.
3. M P Anantram, and FL ´Léonard, ***"Physics of carbon nanotube electronic devices"*** Institute of Physics Publishing, Rep. Prog. Phys. 69 (2006) 507–561.
4. P. Avouris, J. Appenzeller, R. Martel, and S. J. Wind, ***"Carbon nanotube electronics"***, Proceedings of the IEEE, Vol. 91, pp. 1772-1784, 2003.
5. P. L. McEuen, M. S. Fuhrer, and H. K. Park, ***"Single-walled carbon nanotube electronics"***, IEEE Transactions on Nanotechnology, Vol. 1, pp. 78-85, 2002.
6. J. E. Lilienfeld, ***"Method and apparatus for controlling electric currents,"*** U.S. Patent 1 745 175, 1930.
7. D. Kahng and M. M. Atalla, ***"Silicon–silicon dioxide field induced surface devices,"*** presented at the IRE Solid-State Device Res. Conf., Pittsburgh, PA, June 1960.
8. David J. Frank *et al*, ***"Device Scaling Limits of Si MOSFETs and Their Application Dependencies,"*** proceedings of the IEEE, vol. 89, no. 3, march 2001.
9. Chen, Z. *et. al.* ***"I_{DDQ} Testing for Deep-Submicron ICs: Challenges and Solutions"***. 2002. IEEE Design and Test of Computers. 24-33.
10. Rahmat Bin Sanudin, ***"Characterization of Ballistic Carbon Nanotube Field-Effect Transistor,"*** Thesis report, University Technology Malaysia, November 2005.
11. Taur, Y., ***"CMOS design near the limit of scaling,"*** 2002. IBM J. Ref. & Dev., 46(2): 213-220.
12. Compano, R. ed. ***"Technology Roadmap for Nanoelectronics,"*** Microelectronics Advanced Research Initiative, 2000.
13. T Surukai, ***"Perspectives on power aware electronics"***, Keynote presentation, February 2003, ISSCC Conference, pp.26-29.
14. John L. Hennessy and David A. Patterson, ***"Computer Architecture, A Qualitative Approach"***, Ed. 3, pp. 14.
15. Shazia Hassan *et al*, ***"Limitation of Silicon Based Computation and Future Prospects"*** 2010 Second International Conference on Communication Software and Networks, pp. 559-561.
16. Rahman, A. *et al*., ***"Theory of Ballistic Nanotransistors"*** IEEE Transactions on Electron Devices, 50(9): 1853-1864,2003.
17. Heng Chin Chuan., ***"Modeling and Analysis of Ballistic Carbon Nanotube Field Effect Transistor (CNTFET) with Quantum Transport Concept"*** Thesis report, University Technology Malaysia, April 2007.
18. Ali Naderi, A. *et al*., ***"Temperature dependence of Electrical Characteristics of CNTFET: A Quantum Simulation Study"*** Journal of Nanomaterials Volume 2012, Article I D 532625, 7 pages.
19. S. Mudanai, Y Y Fang, Q Quyang, ***"Modeling of direct tunneling current through gate dielectric stacks"***, IEEE Trans. Electron Dev, vol. 47, Number. 10, pp. 1851–1857, 2000.
20. Rasmita Sahoo *et al*., ***"Carbon Nanotube Field Effect Transistor: Basic Characterization and Effect of High Dielectric Material"*** International Journal of Recent Trends in Engineering, Vol 2, No. 7, November 2009.
21. Zhao Xu *et al*, ***"Modeling of Chirality-Dependent Current–Voltage Characteristics of Carbon-Nanotube Field-Effect Transistors"*** Chinese Phy. Latt, Vol:23 No.5(2006).