

# **DESIGN OF A SINGLE PHASE AC-AC CONVERTER**

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE  
REQUIREMENTS FOR THE DEGREE OF BACHELOR OF SCIENCE IN  
ELECTRICAL AND ELECTRONIC ENGINEERING

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## **DECLARATION**

This is to certify that the thesis entitled “Design of a single phase ac-ac converter”, submitted by Md. Imtiaz Khan (ID. 10121103), Abdul Ahad (ID. 09221087) and Kamrul Islam (ID. 09221151), in partial fulfillment of the award of Bachelor of Science (B.Sc.) in Electrical and Electronic Engineering in the Department of Electrical and Electronic Engineering at BRAC University is an authentic work carried out by them under my supervision and guidance.

To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other University / Institute for the award of any Degree or Diploma.

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## **ABSTRACT**

An AC-AC voltage controller is a converter which controls the voltage, current and average power delivered to an AC load from an AC source. They are used in practical circuits like light dimmer circuits, speed controls of induction motors, traction motors control etc. In our thesis we will analyze the performance of a single-phase AC-AC circuit with emphasis on the output harmonic content and utilization of input voltage. This converter can convert from a fixed AC input voltage into variable AC output voltage with desired frequency.

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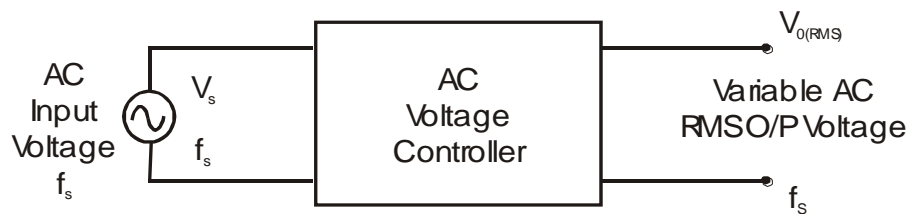
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# **CHAPTER 1**

## **INTRODUCTION**

# 1.0 INTRODUCTION

We will analyze the performance of a single-phase AC-AC circuit with emphasis on the output harmonic content and utilization of input voltage. The only disadvantage of the single-phase AC-AC converter is that the amplitudes of certain harmonic frequencies become abnormally high. This converter can convert from a fixed AC input voltage into variable AC output voltage.



AC voltage controllers are working to vary the RMS value of the alternating voltage applied to a load circuit by introducing Thyristors, IGBT, BJT and MOSFET between the load and a constant voltage AC source.

We have used MOSFET and design a single phase full wave AC voltage bi-directional controller.

Our thesis is about AC-AC converter. An ac voltage controller is a converter which controls the voltage, current and average power delivered to an ac load from an ac source. The input voltage source is ac and the output voltage is also ac, so the circuit is an ac- ac converter. Voltage controllers use electronic switches to connect and disconnect a load to an ac source at regular intervals. This type of circuit is classified as an ac-ac converter.

## 1.1 TYPE OF AC VOLTAGE CONTROLLERS<sup>1</sup>

The ac voltage controllers are classified into two types based on the type of input ac supply applied to the circuit. They are:

- Single Phase AC Controllers.
- Three Phase AC Controller

Each type of controller may be sub divided into;

- Uni-directional or half wave ac controller.
- Bi-directional or full wave ac controller.

In brief different types of ac voltage controllers are:

- Single phase half wave ac voltage controller (uni-directional controller).
- Single phase full wave ac voltage controller (bi-directional controller).
- Three phase half wave ac voltage controller (uni-directional controller).
- Three phase full wave ac voltage controller (bi-directional controller).

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<sup>1</sup> Lecture notes on Power Electronics by Prof. Madhusudhan Rao

## 1.2 AC-AC CONVERSION

Power electronics is the application of electronics for power conversion. A subcategory of power conversion is the AC to AC conversion. Converting an AC waveform to another AC waveform allows one to control the voltage, frequency, and phase of the waveform applied to a load from a supplied AC waveform. The two main categories that can be used to separate the types of converters are whether the frequency of the waveform is changed. The ones which don't allow the user to modify the frequencies are known as AC Voltage Controllers, or AC Regulators. AC converters are the ones which allow the user to change the frequency are simply referred to as frequency converters for AC to AC conversion. Under frequency converters there are three different types of converters that are typically used: cycloconverter, matrix converter, DC link converter (aka AC/DC/AC converter).<sup>2</sup>

The purpose of an AC Voltage Controller, or AC Regulator, is to vary the RMS voltage across the load at a constant frequency. Three control methods that are generally accepted are:

- ON/OFF control
- Phase-Angle Control
- Pulse Width Modulation AC Chopper Control (PWM AC Chopper Control).

All three of these methods can be implemented not only in single-phase circuits, but three-phase circuits as well. In our thesis we applied PWM AC Chopper Control method.

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<sup>2</sup> Power Electronics- Circuits, Devices and Applications by Muhammad Harunur Rashid

**Applications:** Understanding how each of the converters work is all good and well, but it is useless in a practical sense if one does not understand where each converter is applied in the real world. Below is a list of common applications that each converter is used in.<sup>3</sup>

- **AC Voltage Controller:** Lighting Control; Domestic and Industrial Heating; Speed Control of Fan, Pump or Hoist Drives, Soft Starting of Induction Motors, Static AC Switches (Temperature Control, Transformer Tap Changing, etc)
- **Cycloconverter:** High-Power Low-Speed Reversible AC Motor Drives; Constant Frequency Power Supply with Variable Input Frequency; Controllable VAR Generators for Power Factor Correction; AC System Interties Linking Two Independent Power Systems.
- **Matrix Converter:** Currently the application of Matrix converters are limited due to non-availability of bilateral monolithic switches capable of operating at high-frequency, complex control law implementation, commutation and other reasons.
- **DC Link:** Can be used for individual or multiple load applications of machine building and construction.

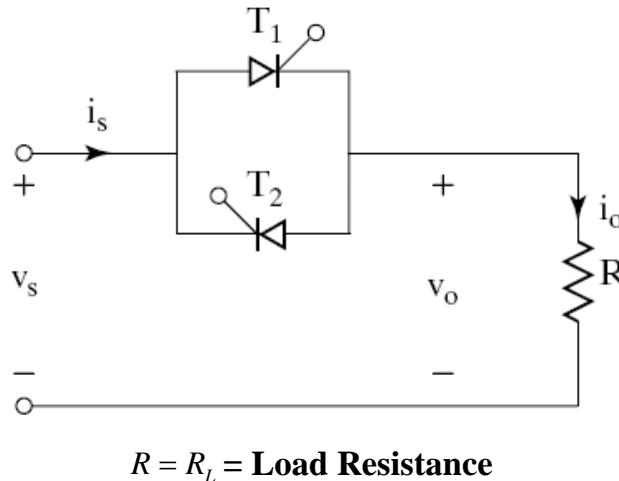
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<sup>3</sup> [http://en.wikipedia.org/wiki/Power\\_electronics](http://en.wikipedia.org/wiki/Power_electronics) reference

### 1.3 SINGLE PHASE FULL WAVE AC-AC VOLTAGE CONTROLLER:

**SCR** is a semi-controlled device turns on when a gate pulse is present and the anode is positive compared to the cathode. When a gate pulse is present, the device operates like a standard diode. When the anode is negative compared to the cathode, the device turns off and blocks positive or negative voltages present. The gate voltage does not allow the device to turn off.

The principle of on-off control technique is explained with reference to a single phase full wave ac voltage controller circuit **Fig. 1.3.a** which is composed of a pair of SCRs connected back-to-back (also known as inverse-parallel or anti parallel) between the ac supply and the load.<sup>4</sup>



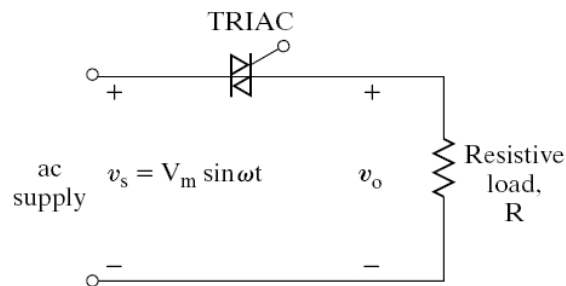
**Fig. 1.3a: Single phase full wave two SCRs in inverse parallel.**

Here the SCR,  $T_1$  is forward biased and during the positive half cycle of the input supply voltage. The SCR,  $T_1$  is triggered at a delay angle of ' $\alpha$ '. Considering the on SCR  $T_1$  as an ideal closed switch the input supply voltage appears across the load resistor,  $R$

<sup>4</sup> Power Electronics- Circuits, Devices and Applications by Muhammad Harunur Rashid

and the output voltage  $V_o = V_s$  during  $\omega t = \alpha$  to  $\pi$  radians. The load current flows through the SCR, T1 and through the load resistor R in the downward direction. At  $\omega t = \pi$ , when the input voltage falls to zero the SCR current falls to zero and hence the SCR, T1 turns off. No current flows in the circuit during  $\omega t = \pi$  to  $(\alpha + \pi)$ .

The SCR, T2 is forward biased during the negative cycle of input supply and when SCR T2 is triggered at a delay angle  $(\alpha + \pi)$ , the output voltage follows the negative half cycle of input from  $\omega t = (\alpha + \pi)$  to  $2\pi$ . When T2 is on, the load current flows in the reverse direction through SCR T2. The time interval (spacing) between the gates trigger pulses of T1 and T2 is kept at  $180^\circ$ . At  $\omega t = 2\pi$ , the input supply voltage falls to zero and hence the load current also falls to zero and SCR T2 turns off. Instead of using two SCR's in parallel, a Triac, **Fig. 1.3.b** can be used. <sup>5</sup>



**Fig.: 1.3.b Single phase full wave ac voltage controller (Bi-directional Controller) using TRIAC**

**Triac** is a device that is essentially an integrated pair of phase-controlled thyristors connected in inverse-parallel on the same chip. Like an SCR, when a voltage pulse is present on the gate terminal, the device turns on. The main difference between an SCR and a Triac is that both the positive and negative cycle can be turned on independently of each other, using a positive or negative gate pulse. Similar to an SCR, once the device is turned on, the device cannot be turned off. This device is considered bi-polar and reverse voltage blocking.

<sup>5</sup> Power Electronics- Circuits, Devices and Applications by Muhammad Harunur Rashid

# **CHAPTER 2**

## **APPLIED TECHNIQUES**

## 2.0 APPLIED TECHNIQUES

- **Switching**
- **PWM**
- **Optocoupler**
- **Filtering**

### 2.1 4 TYPES OF SWITCHES THAT COULD BE USED IN AN AC-AC CONVERTER

**Thyristor** – refers to a family of three terminal devices that include SCRs, GTOs, and MCT. For most of the devices, a gate pulse turns the device on. The device turns off when the reverse voltage at the anode is more negative than the cathode. When turned off, it is considered as a reverse voltage blocking device.<sup>6</sup>

The **BJT** cannot be used at high power, slower and more on resistive losses when compared to MOSFET type devices. In order to carry high current, BJTs must have relatively large base currents, thus these devices have high power losses when compared to MOSFET devices. BJTs along with MOSFETs are also considered unipolar and do not block reverse voltage very well, unless installed in pairs with protection diodes. Generally, BJTs are not utilized in power electronics switching circuits because of the  $i^2 \cdot r$  losses associated with on resistance and base current requirements. BJTs have lower current gains in high power packages, thus requiring them to be setup in Darlington configurations in order to handle the currents required by power electronic circuits. Because of these multiple transistor configurations, switching times are in the hundreds

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<sup>6</sup> [http://en.wikipedia.org/wiki/Power\\_electronics](http://en.wikipedia.org/wiki/Power_electronics) reference

of nanoseconds to microseconds. Devices have voltage ratings which max out around 1500 volts and fairly high current ratings. They can also be paralleled in order to increase power handling, but must be limited to around 5 devices for current sharing.

**MOSFET** technology's benefit over BJTs, is lower gate current (base current for BJT is large compared to almost zero for Mosfet gate current). Since the Mosfet is a depletion channel device, voltage, not current is necessary to create a conduction path from drain to source. The gate does not contribute to either drain or source current. Turn on gate current is essentially zero with the only power dissipated at the gate coming during switching. Losses in Mosfets are largely attributed to on-resistance. The calculations show a direct correlation to drain source on-resistance and the device blocking voltage rating,  $BV_{dss}$ . Switching times range from tens of nanoseconds to a few hundred microseconds, depending on the device. Mosfet drain source resistances increase as more current flows through the device. As frequencies increase the losses increase as well, making BJTs more attractive. Power Mosfets can be paralleled in order to increase switching current and therefore overall switching power. Nominal voltages for Mosfet switching devices range from a few volts to a little over 1000 volts, with currents up to about 100 amps or so. Newer devices may have higher operational characteristics. Mosfet devices are not bi-directional, nor are they reverse voltage blocking.

**IGBT** have the best characteristics of Mosfets and BJTs. Like Mosfet devices, the insulated gate bipolar transistor (IGBT) has a high gate impedance, thus low gate current requirements. Like BJTs, this device has low on state voltage drop, thus low power loss across the switch in operating mode. Similar to the GTO, the IGBT can be used to block both positive and negative voltages. Operating currents are fairly high, in excess of 1500 amps and switching voltage up to 3000 volts. The IGBT has reduced input capacitance compared to MOSFET devices which improves the Miller feedback effect during high  $dv/dt$  turn on and turn off.<sup>7</sup>

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<sup>7</sup> [http://en.wikipedia.org/wiki/Power\\_electronics](http://en.wikipedia.org/wiki/Power_electronics) reference

## 2.2 REASONS OF USING MOSFET IN OUR CIRCUIT

The most significant advantage is that MOSFETs don't need current on their control pin, but require more voltage. Some don't turn on fully at 5v, some do. A BJT is limited to something like 0.3v for the lowest voltage drop on the current path, but MOSFETs are only limited by their resistance ( $r_{DSon}$ ). MOSFETs are usually more efficient switches for power supplies, etc where we want a switch rather than an amplifier. FET's are only more efficient because they can be switched a lot faster and thus small SMPS can be used.

MOSFETs can easily be placed in parallel; bipolars unless external emitter resistors are added. The external resistance generates additional efficiency and voltage drop losses. Also to operate bipolars at high switching frequencies and high current, we have to prevent the devices from going into hard saturation as this will increase storage times (making it difficult to switch off quickly) but then cause the device to dissipate more heat due to higher  $V_{ce-sat}$ .<sup>8</sup>

The biggest thing a MOSFET switch does is route the high current flow from the battery, directly to the motor, bypassing the trigger contacts. The trigger contacts only draw a small current to activate the MOSFET switch, which for all intensive purposes, put no wear or stress on them.

### **Advantages:**

1. MOSFETs are small compare to bjt's so it fabricated easily and space saving scheme on the circuit.
2. MOSFET's input impedance is very high so they do not load the circuits. Loading effect doesn't arise.
3. Operating frequency is very high so may be used at higher frequencies.
4. MOSFETs are used in digital circuits for its reliability.

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<sup>8</sup> Introduction to Power Electronics by Daniel W. Hart

5. The effect of noise is less than BJT, so high signal to noise ratio.
6. MOSFET s are unipolar devices so reverse saturation current doesn't exist.
- 7 It consumes less D.C power rather than BJT.
8. It protects electrical system (but in a different way than the fuse does. MOSFET's do not eliminate the need for a fuse, unless your MOSFET has a fuse build in). The MOSFET passes much less current through the trigger contacts. The benefit of this is that it eliminates arcing which will blacken and slowly corrode/destroy the contacts.

**Disadvantages:**

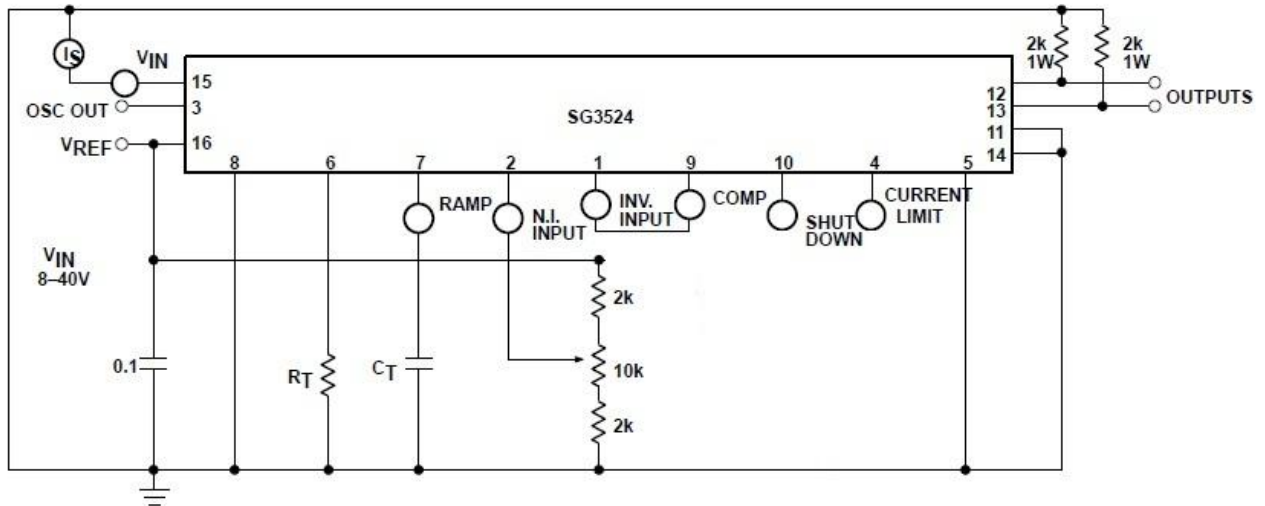
1. Handling is not easy. MOSFET is very sensitive to electrostatic charge so it may be destroy when one touch the pins of a MOSFET devices by hand.
2. Trans conductance is lower than BJT.

## **2.3 PULSE WIDTH MODULATOR**

We have used SG 3524 for constructing the pulse width modulator circuit. The SG2524 and SG3524 incorporate all the functions required in the construction of a regulating power supply, inverter, or switching regulator on a single chip. They also can be used as the control element for high-power-output applications. The SG2524 and SG3524 were designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformer less voltage doublers, and polarity converter applications employing fixed-frequency, pulse-width modulation (PWM) techniques. The complementary output allows either single-ended or push-pull application. Each device includes an on-chip regulator, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted pass transistors, a high-gain comparator, and current-limiting and shutdown circuitry.<sup>9</sup>

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<sup>9</sup> Introduction to Power Electronics *by* Daniel W. Hart



**Fig.: 2.3.1 Pulse Width Modulator, SG3524 pin configuration**

#### **Features:**

- Complete Pulse-Width Modulation (PWM) Power-Control Circuitry
- Uncommitted Outputs for Single-Ended or Push-Pull Applications
- Low Standby Current, 8 mA Type
- Interchangeable With Industry Standard SG3524

## **2.4 OPTO COUPLER**

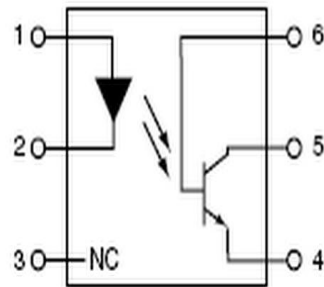
In electronics, an **optocoupler**, also called an **opto-isolator**, **photocoupler**, or **optical isolator**, is "an electronic device designed to transfer electrical signals by utilizing light waves to provide coupling with electrical isolation between its input and output". The main purpose of an opto-isolator is "to prevent high voltages or rapidly changing voltages on one side of the circuit from damaging components or distorting transmissions on the other side.

The general purpose of optocouplers is to isolate the ground between the switches and the circuit.<sup>10</sup>

<sup>10</sup> Lecture notes on Power Electronics by Prof. Madhusudhan Rao

**Applications:**

- Power supply regulators
- Microprocessor input
- Digital Logic Input



PIN 1. ANODE  
2. CATHODE  
3. NO CONNECTION  
4. EMITTER  
5. COLLECTOR  
6. BASE

**Fig.: 2.4.1 Opt-coupler pin configuration**

The desired frequency of current for which we have worked is 50 Hz and the switching frequency which we have applied here are 10Khz, 20Khz, 30Khz, 40Khz, 50Khz. That means the switching frequency is much bigger than our desired frequency. So when we operate our circuit, the switching frequency follows the formulae as that of DC circuit.

## **2.5 FILTER DESIGN**

We have designed two controlled circuit in our theses. BUCK and BOOST both are designed for reducing the harmonic contents using LC filter. The values here taken for both input and output inductor and capacitor by using the following formulae

Input filter design formula for BUCK topology is;

$$L1C1=1/(2\pi(f1))^2$$

Output filter design formula for BUCK topology

$$L2 = (1-D)R/2(f2)$$

Input filter design formula for BOOST topology

$$L1 = D(1-D)^2/2(f2)$$

Where, D = Duty Cycle, (f1) = Desired Frequency, (f2) = Switching Frequency.

# **CHAPTER 3**

## **BUCK CIRCUIT**

## 3.0 BUCK CIRCUIT

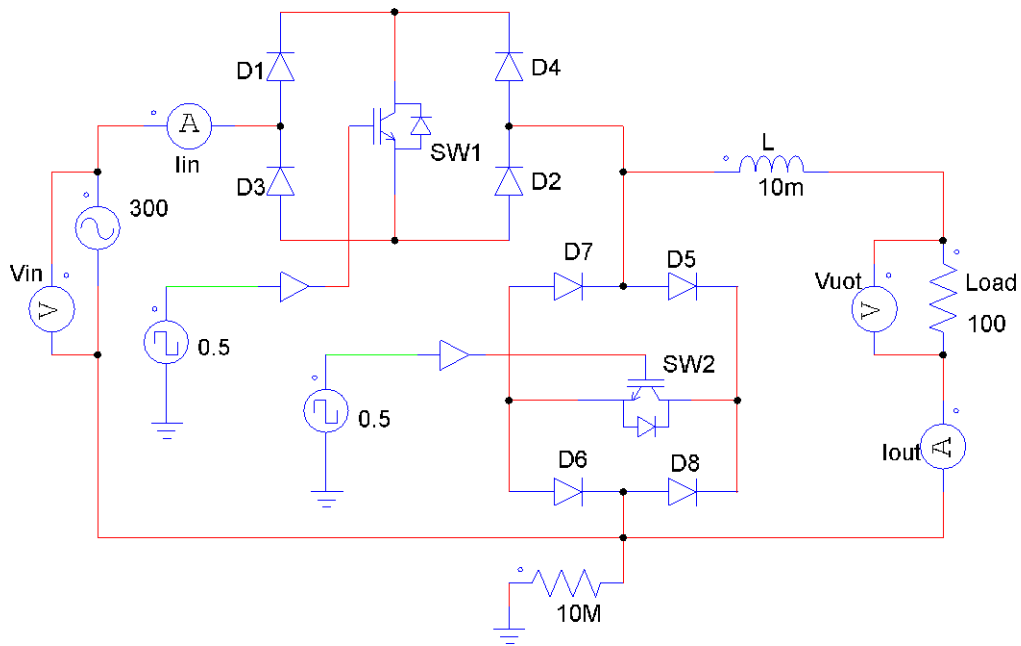
### 3.1 BUCK CONVERTER:

AC to AC voltage converters operate on the AC mains to regulate the output voltage. Part of the supply appears at the load while the semiconductor switches block the remaining portions. AC-AC phase-angle controlled or integral cycle controlled single voltage-controllers are widely used in low, medium and high power applications for controlling voltage across loads. Conventional techniques have many drawbacks like the retardation of the firing angle causing lagging power factor at the input side, substantial low order harmonics in the supply voltages/currents and discontinuity of power flow to the load etc. Solid-state switch based AC-AC PWM regulator similar to the DC-DC converters. They require a bi-directional freewheeling path across the load. Also, switches in the circuits require synchronized (current-sensed) switching to attain in-phase input current to improve power factor.

### 3.2 BASIC OPERATION OF BUCK TOPOLOGY

The BUCK converter is mainly controlled by two bi-directional switches. The condition of controlling the switches is when one switch is closed then the other switch must be open. In positive half cycle, when switch 1 (SW1) is closed, then current will flow directly through the load and the inductor (L) will be energized. In this case the output voltage drop is maximum but for some internal voltage drop for the impedances of inductors, capacitors etc output voltage can never exceed the input voltage. Hence the output voltage can be controlled by changing the duty cycle of the switches. In next state, SW1 is open and SW2 is closed, the load will be detached from the source and the inductor will supply the current at same direction, and this current will flow through SW2 and the load like a loop. In this case voltage drop across the load is very few.

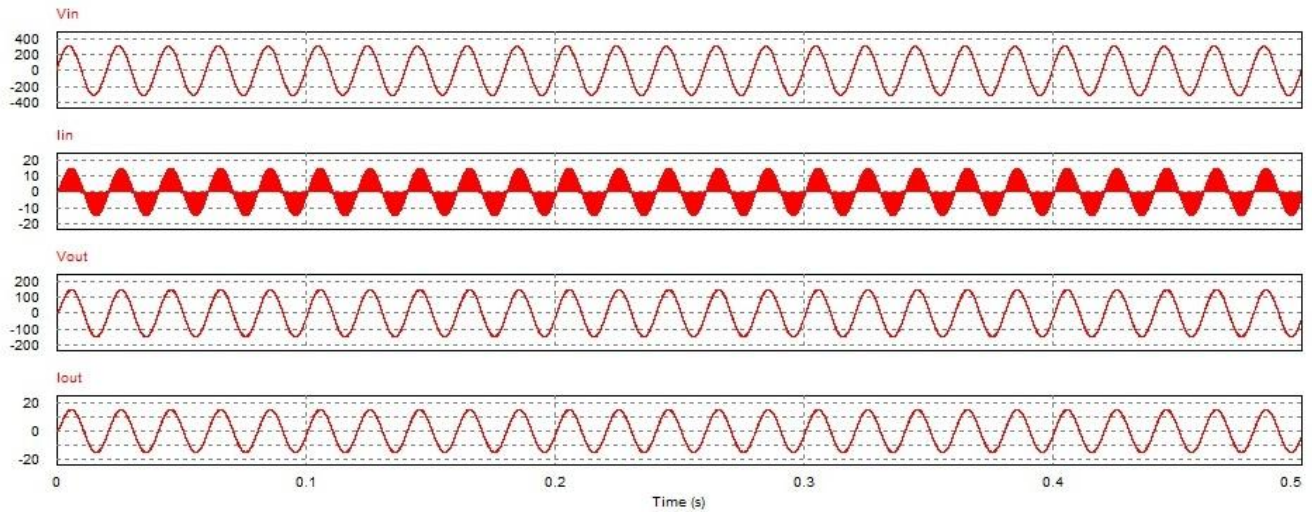
For negative half cycle, when SW1 is closed and SW2 is open, then the current flow through the load and returns to the source. Output voltage drop will be maximum. When SW1 is open and SW2 is closed then the inductor again supply current which will flow through SW2 and the load like a loop and again the source will be detached. A few voltage will drop across the load.



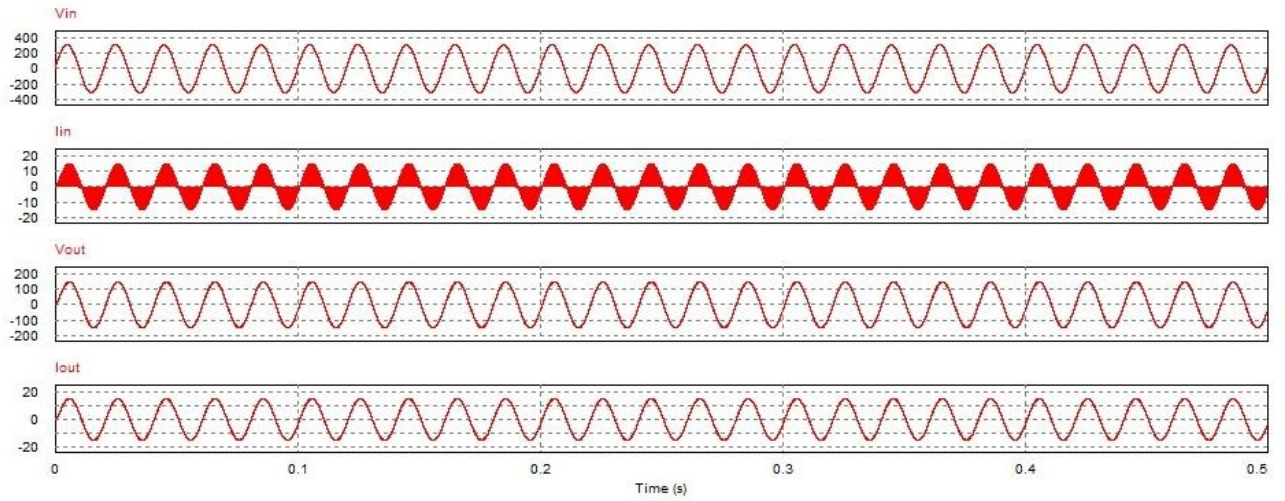
### 3.3 WAVE FORMS AND DATA SHEET OF BUCK TOPOLOGY CIRCUIT

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & I/P Volatge) | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|--------------------------------|----------------|
| 0.1              | 0.9              | 36                | 0.6708269           | 0.67080677           | 67.080677            | 299.91003             | 0.31630685                     | 99.96997002    |
| 0.2              | 0.8              | 72                | 0.9486925           | 0.94866403           | 94.866403            | 199.97002             | 0.44725833                     | 99.98496609    |
| 0.3              | 0.7              | 108               | 1.1619112           | 1.1618763            | 116.18763            | 152.73725             | 0.54775229                     | 99.98997105    |
| 0.4              | 0.6              | 144               | 1.3416706           | 1.3416303            | 134.16303            | 122.46531             | 0.63247926                     | 99.99246712    |
| 0.5              | 0.5              | 180               | 1.5000333           | 1.4999883            | 149.99883            | 99.994011             | 0.70712272                     | 99.99396471    |
| 0.6              | 0.4              | 216               | 1.643211            | 1.6431617            | 164.31617            | 81.645589             | 0.77460958                     | 99.99496688    |
| 0.7              | 0.3              | 252               | 1.774876            | 1.7748228            | 177.48228            | 65.462577             | 0.8366705                      | 99.99568272    |
| 0.8              | 0.2              | 288               | 1.8974206           | 1.8973636            | 189.73636            | 49.998143             | 0.89443278                     | 99.9962168     |
| 0.9              | 0.1              | 324               | 2.0125226           | 2.0124622            | 201.24622            | 33.332248             | 0.94868725                     | 99.99663468    |

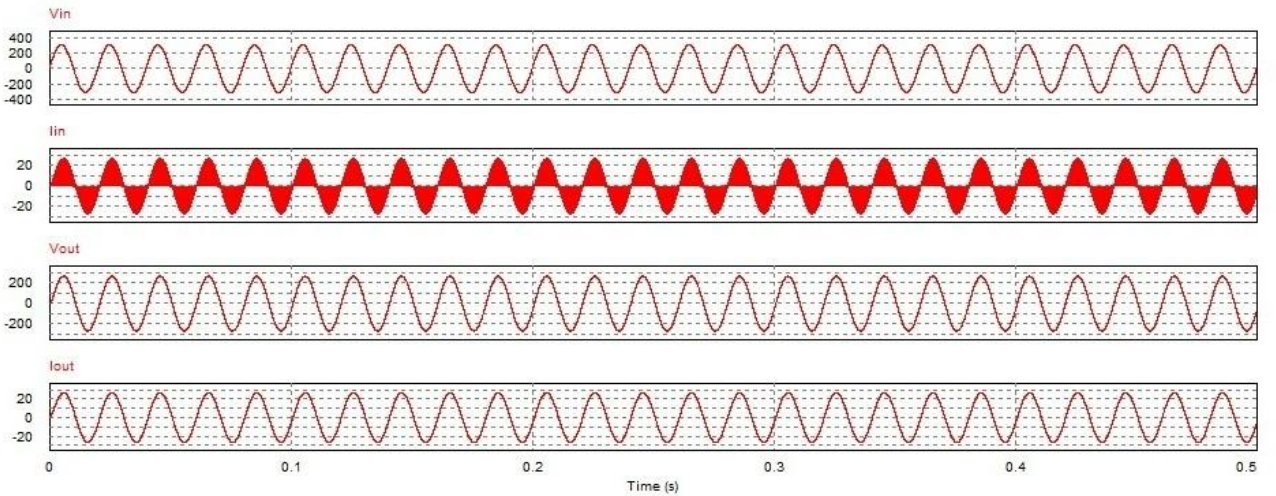
**Fig. 3.3.1 Data Sheet of a BUCK TOPOLOGY circuit performance at 20kHz**



**Fig. 3.3.2 Output and input of wave shape for duty cycle 0.1 with 20Khz frequency**

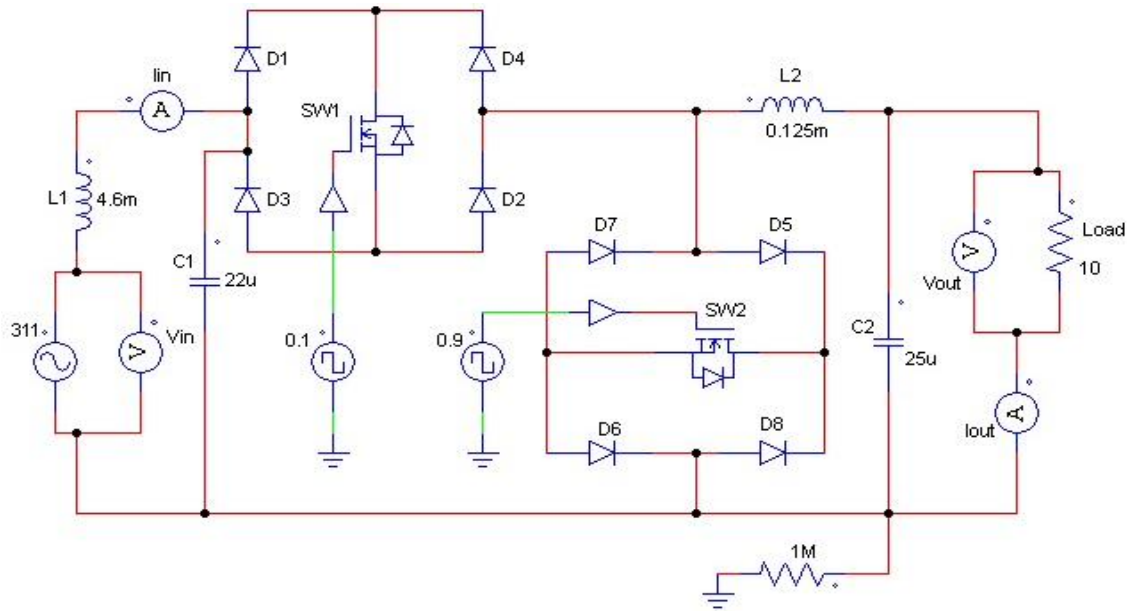


**Fig. 3.3.3 Output and input of wave shape for duty cycle 0.5 with 20KHz frequency**



**Fig. 3.3.4 Output and input of wave shape for duty cycle 0.9 with 20KHz frequency**

### 3.4 BUCK TOPOLOGY WITH FILTER DESIGN



**Fig.: 3.4.1 Buck Topology with Filter**

Formulae used to find the parameters here are:

$$L1C1=1/(2\pi(f1))^2$$

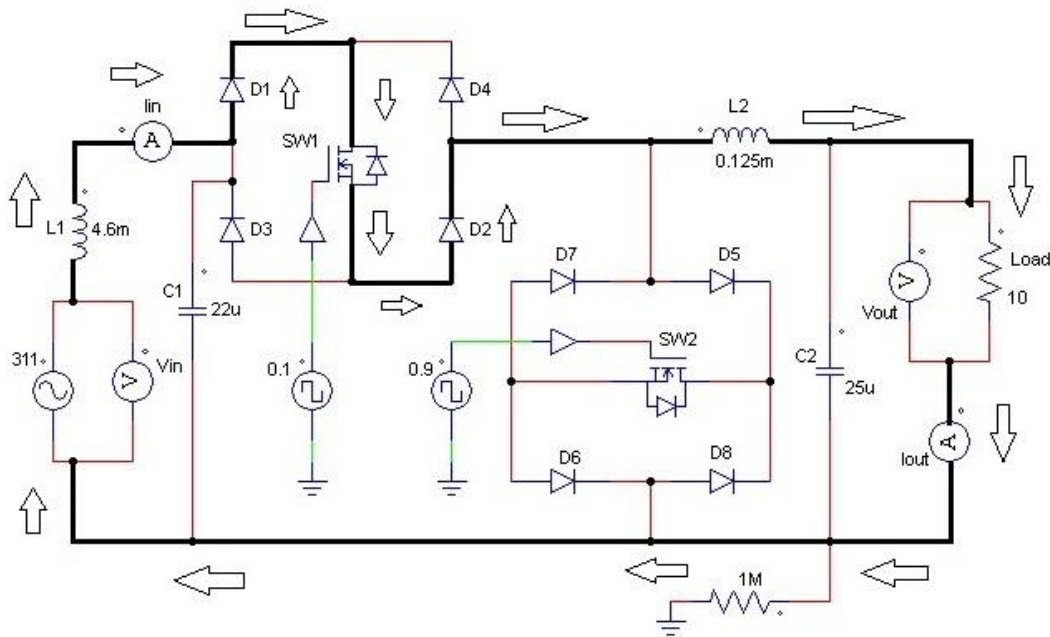
$$L2 = (1-D)R/2(f2)$$

Here ripple voltage is assumed 5%. (f1) is the desired frequency (5000). (f2) is switching frequency (Let 20kHz).

### 3.5 CURRENT FLOW DIAGRAMS

#### For +ve half cycle with SW1 on

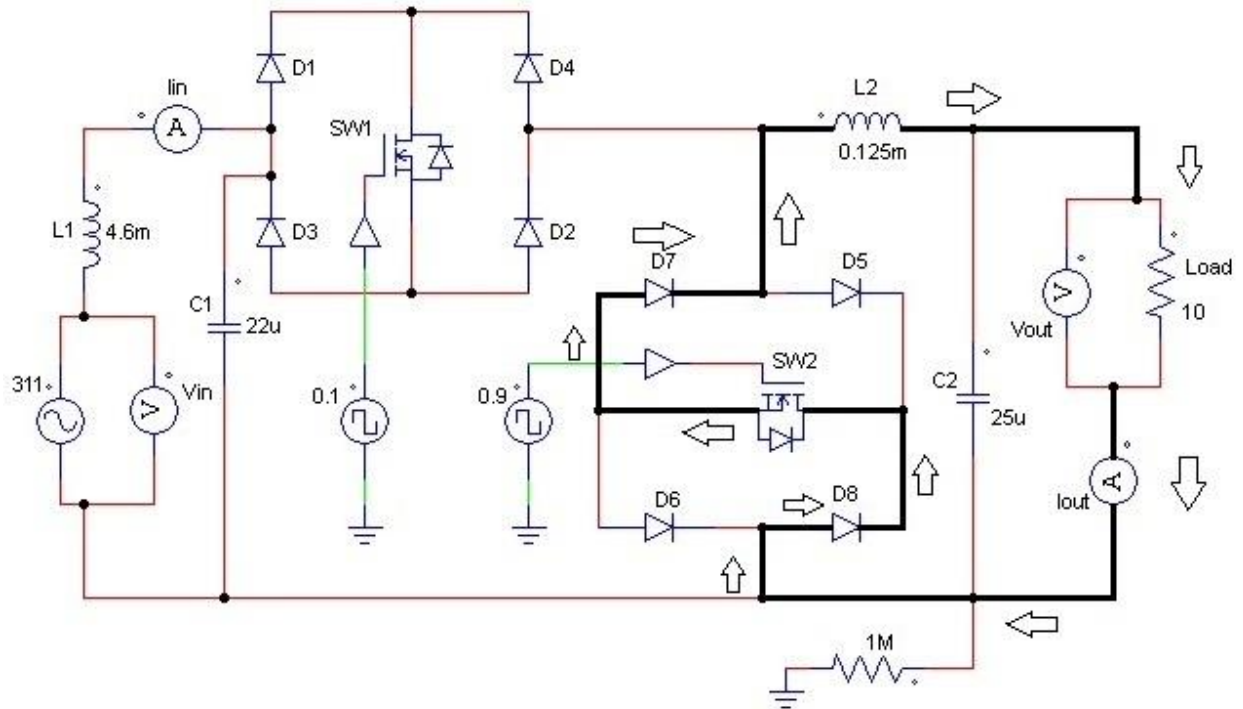
The input current will pass through the path L1, SW1, load and will return to the source as shown in the figure 3.4.2. L1 and C1 will reduce the input harmonic contents of input current and set its frequency. Both the inductors will be charged and L2 and C2 will reduce the harmonic contents output.



**Fig: 3.5.1 Current flow diagram of Buck Topology with Filter for (+ve) cycle when sw1 active**

**For +ve half cycle with SW2 on**

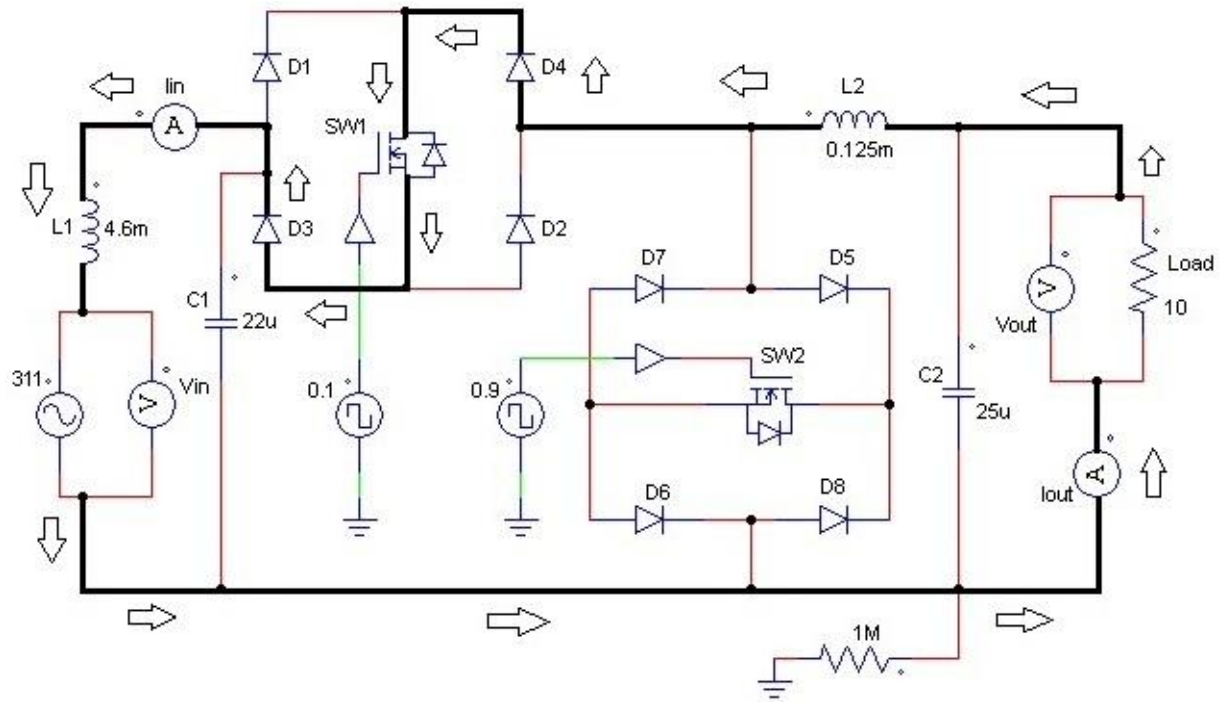
The source will detach from the load and L2 will supply current as it will find a closed loop path through the load. The direction of current flow is shown in **Fig. 3.5.2**.



**Fig: 3.5.2 Current flow diagram of Buck Topology with Filter for (+ve) cycle when sw2 active**

### For -ve cycle with SW1 on

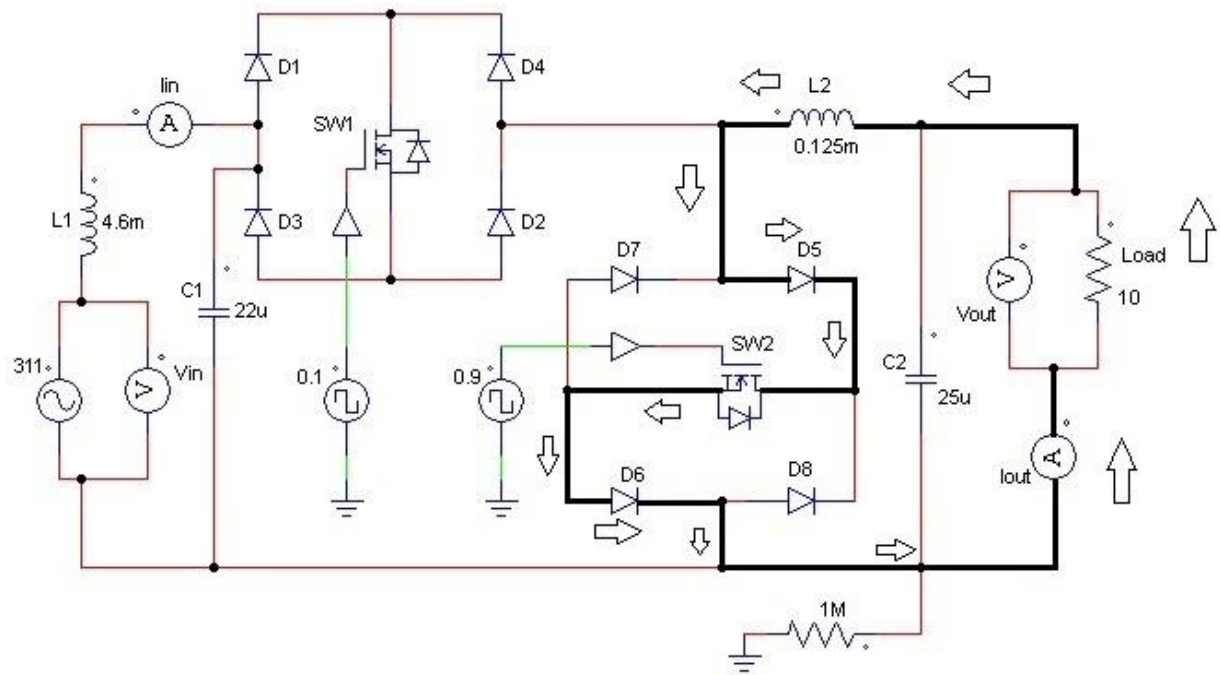
Input current will flow through the load directly and return to the source through SW1 as shown in **Fig 3.5.3**. The inductors will be energized.



**Fig: 3.5.3 Current flow diagram of Buck Topology with Filter for (-ve) cycle when sw1 active**

### For –ve cycle with SW2 on

L2 will supply current through SW2 and the load as a loop. The load will be detached from the source.

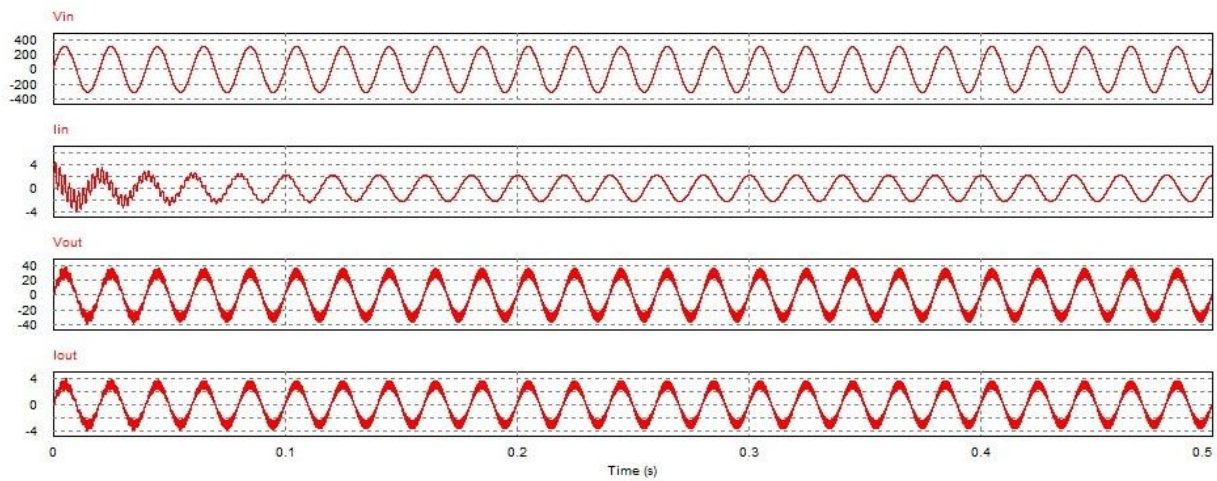


**Fig: 3.5.4 Current flow diagram of Buck Topology with Filter**

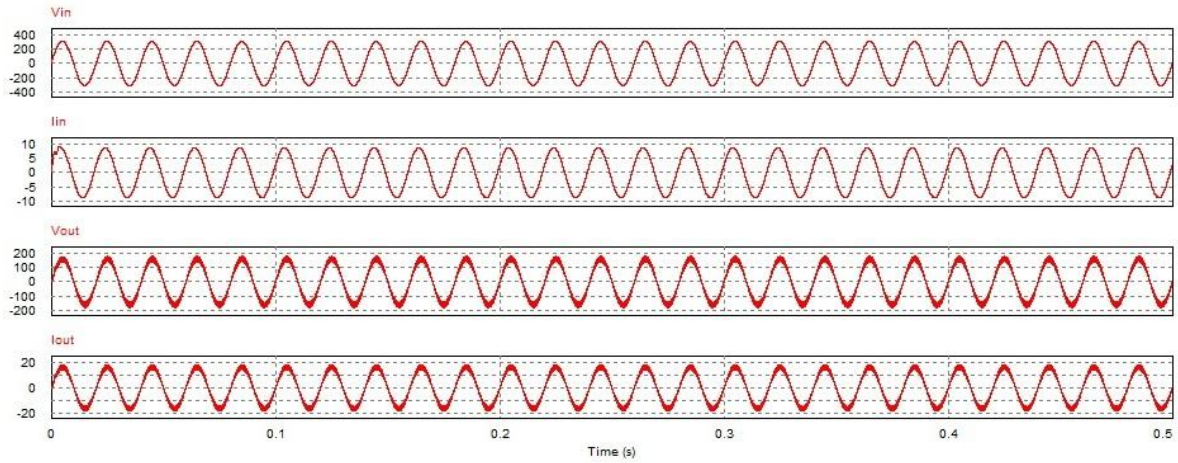
### 3.6 DATA ANALYSIS, WAVEFORMS AND CURVES

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & Volatge | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|---------------------------|----------------|
| 0.1              | 0.9              | 36                | 1.5329              | 2.166287             | 21.66287             | 0.089807              | 0.146679                  | 98.38862       |
| 0.2              | 0.8              | 72                | 1.799358            | 4.354713             | 43.54713             | 0.21934               | 0.498441                  | 99.67392       |
| 0.3              | 0.7              | 108               | 2.60927             | 6.568846             | 65.68846             | 0.347443              | 0.780618                  | 99.86525       |
| 0.4              | 0.6              | 144               | 4.023924            | 8.794677             | 87.94677             | 0.387292              | 0.906773                  | 99.92753       |
| 0.5              | 0.5              | 180               | 5.968495            | 11.00746             | 110.0746             | 0.369086              | 0.957413                  | 99.95477       |
| 0.6              | 0.4              | 216               | 8.361287            | 13.18053             | 131.8053             | 0.316221              | 0.97977                   | 99.96818       |
| 0.7              | 0.3              | 252               | 11.13448            | 15.29574             | 152.9574             | 0.242803              | 0.99077                   | 99.97509       |
| 0.8              | 0.2              | 288               | 14.24775            | 17.35333             | 173.5333             | 0.159884              | 0.996476                  | 99.98761       |
| 0.9              | 0.1              | 324               | 17.72212            | 19.38086             | 193.8086             | 0.075532              | 0.999246                  | 99.9889        |

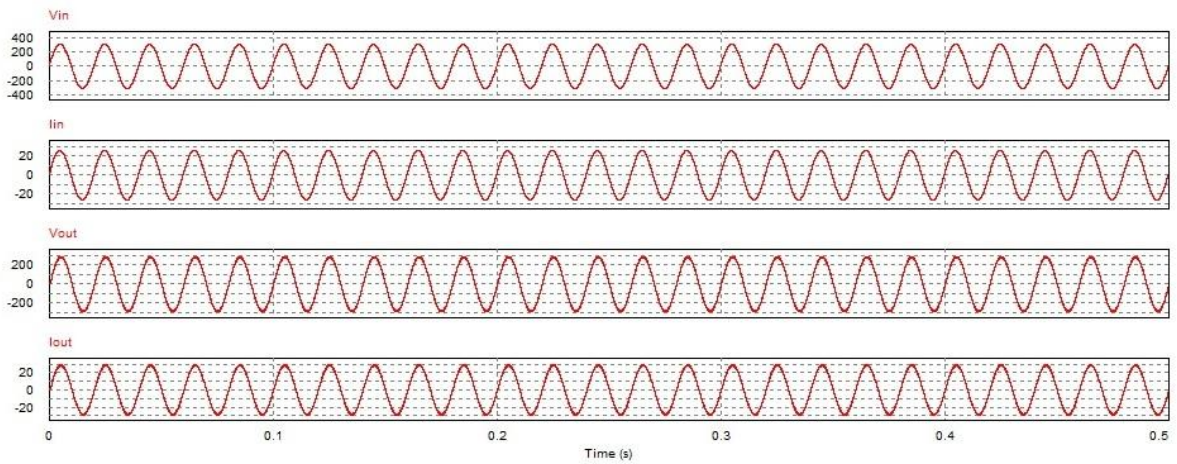
**Fig.: 3.6.1 Buck Topology with Filter Performance at 10kHz**



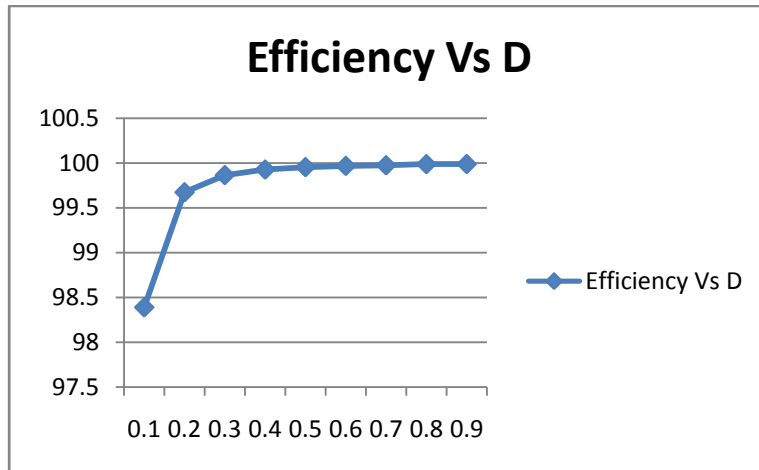
**Fig.: 3.6.1.a Output and input of wave shape for duty cycle 0.1 with 10Khz frequency**



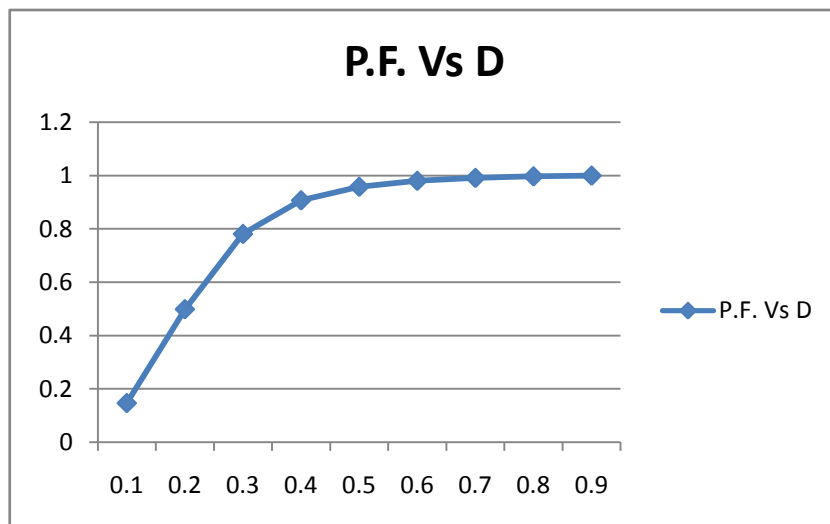
**Fig.: 3.6.1.b Output and input of wave shape for duty cycle 0.5 with 10KHz frequency**



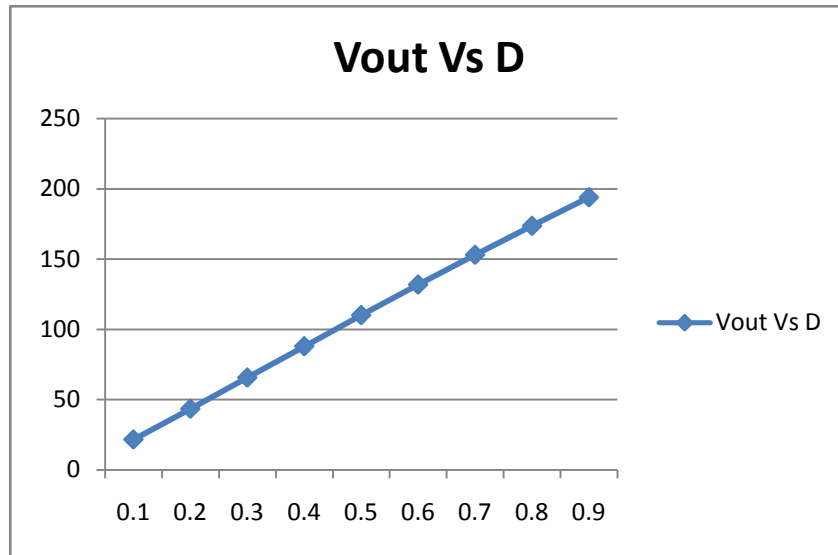
**Fig.: 3.6.1.c Output and input of wave shape for duty cycle 0.9 with 10KHz frequency**



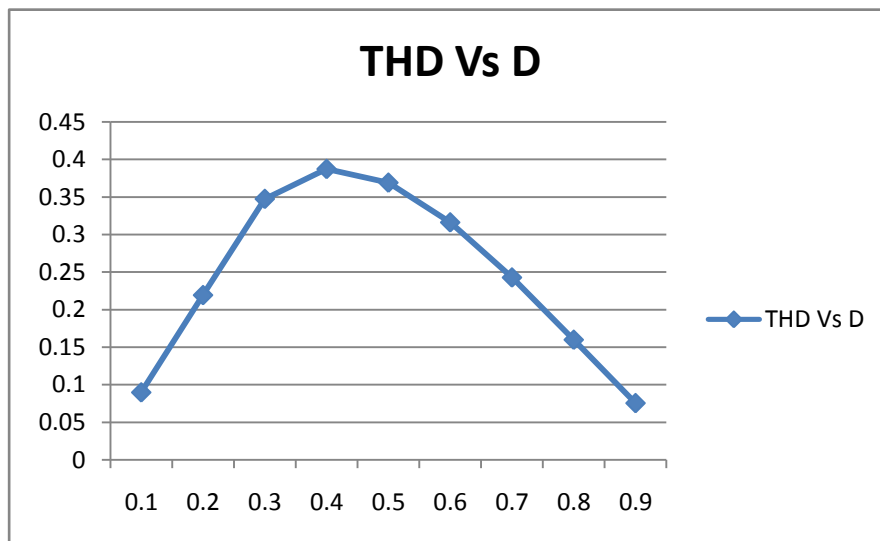
**Fig.: 3.6.1.d Efficiency Vs Duty Cycle at 10kHz**



**Fig.: 3.6.1.e Power Factor Vs Duty Cycle at 10kHz**



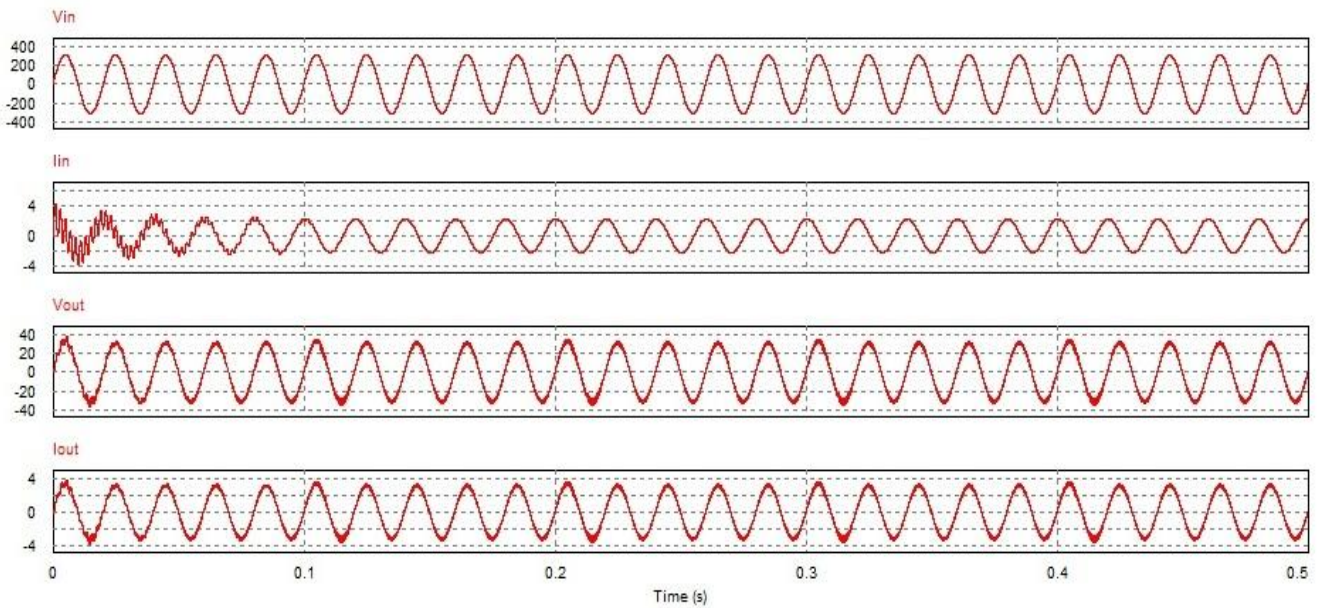
**Fig.: 3.6.1.f Output Voltage Vs Duty Cycle at 10kHz**



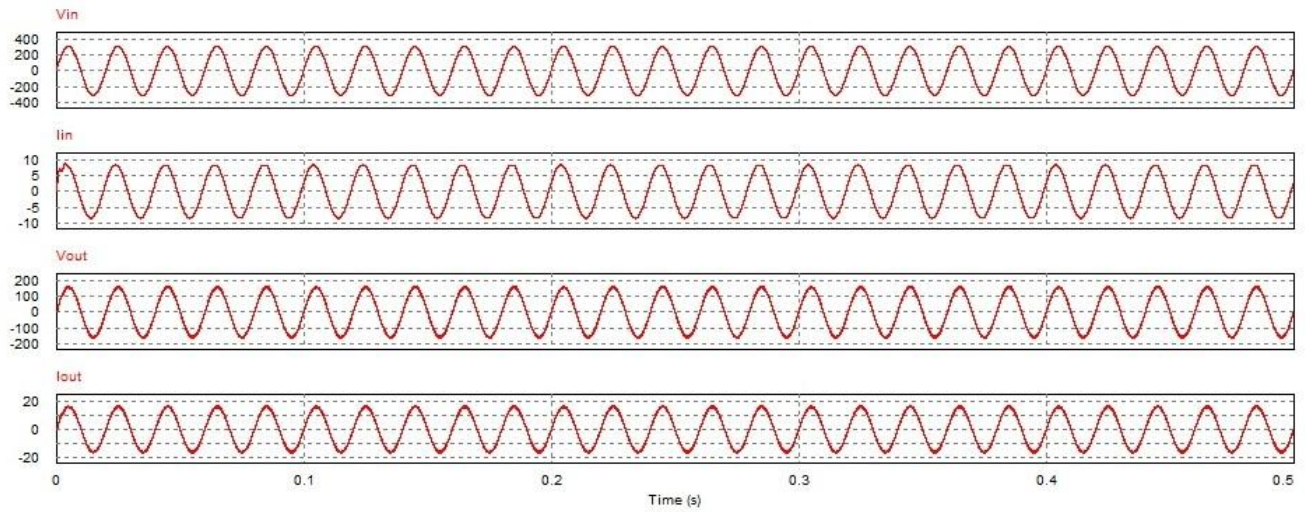
**Fig.: 3.6.1.g THD Vs Duty Cycle at 10kHz**

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F (I/P Current & I/P Volatge) | Efficiency % |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|---------------------------------|--------------|
| 0.10             | 0.90             | 36.00             | 1.60                | 2.24                 | 22.42                | 0.76                  | 0.15                            | 91.34        |
| 0.20             | 0.80             | 72.00             | 1.85                | 4.46                 | 44.62                | 0.57                  | 0.50                            | 97.72        |
| 0.30             | 0.70             | 108.00            | 2.65                | 6.70                 | 67.01                | 0.27                  | 0.77                            | 99.12        |
| 0.40             | 0.60             | 144.00            | 4.04                | 8.95                 | 89.50                | 0.21                  | 0.90                            | 99.55        |
| 0.50             | 0.50             | 180.00            | 5.98                | 11.21                | 112.10               | 1.25                  | 0.95                            | 99.81        |
| 0.60             | 0.40             | 216.00            | 8.38                | 13.43                | 134.28               | 0.08                  | 0.98                            | 99.89        |
| 0.70             | 0.30             | 252.00            | 11.26               | 15.65                | 156.51               | 0.04                  | 0.99                            | 99.91        |
| 0.80             | 0.20             | 288.00            | 14.56               | 17.85                | 178.57               | 0.03                  | 0.99                            | 99.92        |
| 0.90             | 0.10             | 324.00            | 18.30               | 20.04                | 200.45               | 0.02                  | 0.99                            | 99.93        |

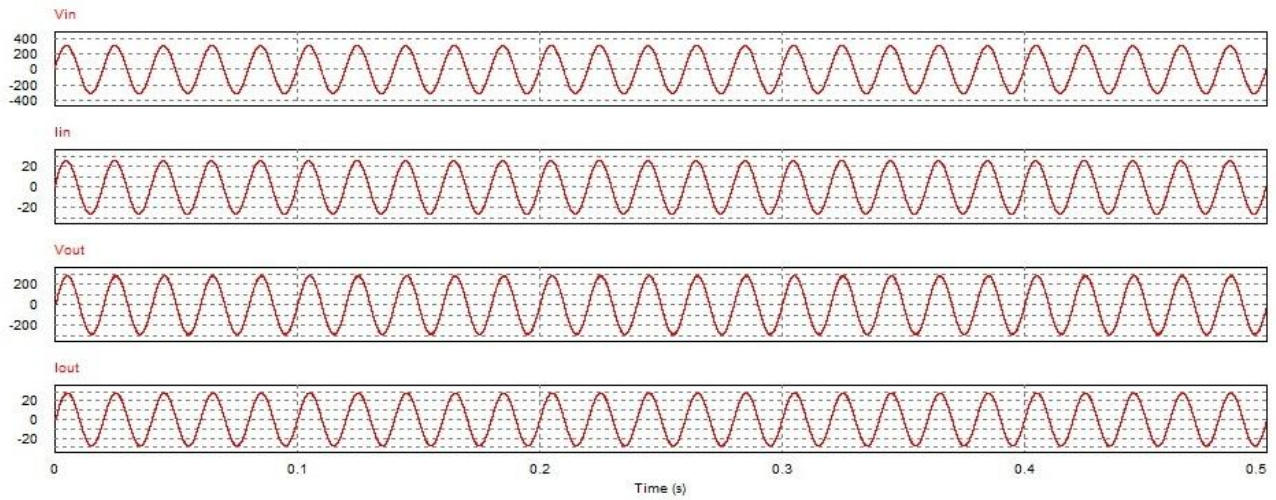
**Fig.: 3.6.2 Buck Topology with Filter Performance at 20kHz**



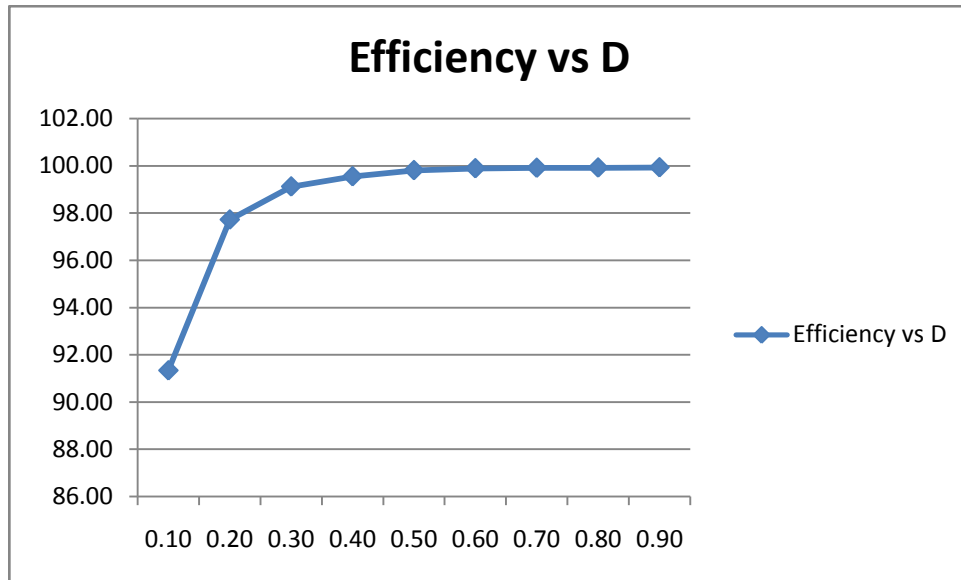
**Fig. 3.6.2.a Output and input of wave shape for duty cycle 0.1 with 20Khz frequency**



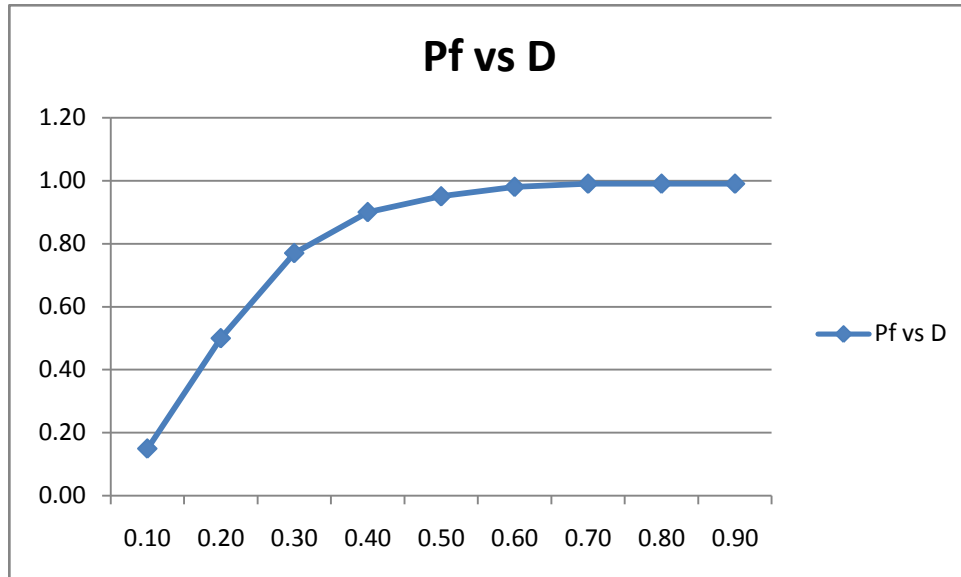
**Fig. 3.6.2.b Output and input of wave shape for duty cycle 0.5 with 20KHz frequency**



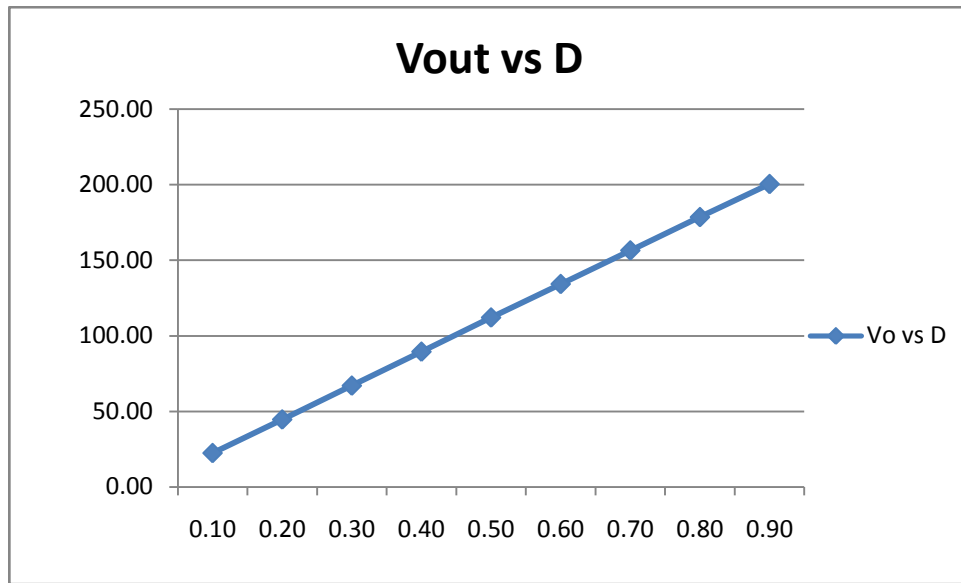
**Fig. 3.6.2.c Output and input of wave shape for duty cycle 0.9 with 20KHz frequency**



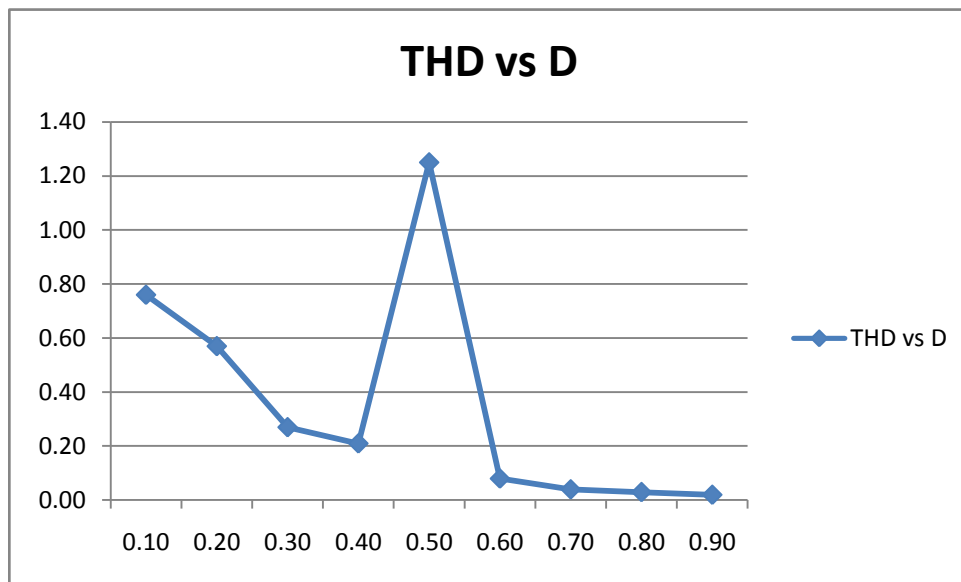
**Fig.: 3.6.2.d Efficiency Vs Duty Cycle at 20kHz**



**Fig.: 3.6.2.e Power Factor Vs Duty Cycle at 20kHz**



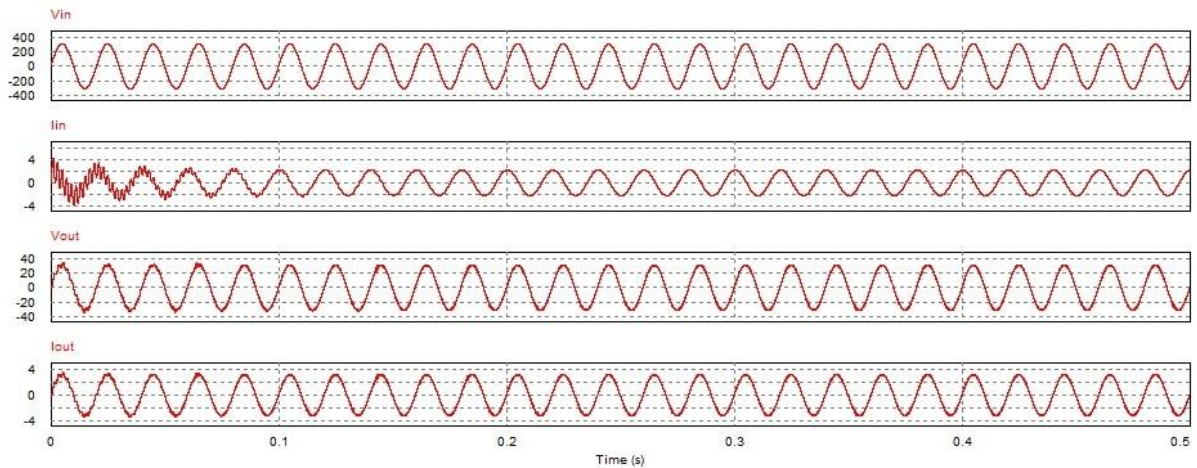
**Fig.: 3.6.2.f Output Voltage Vs Duty Cycle at 20kHz**



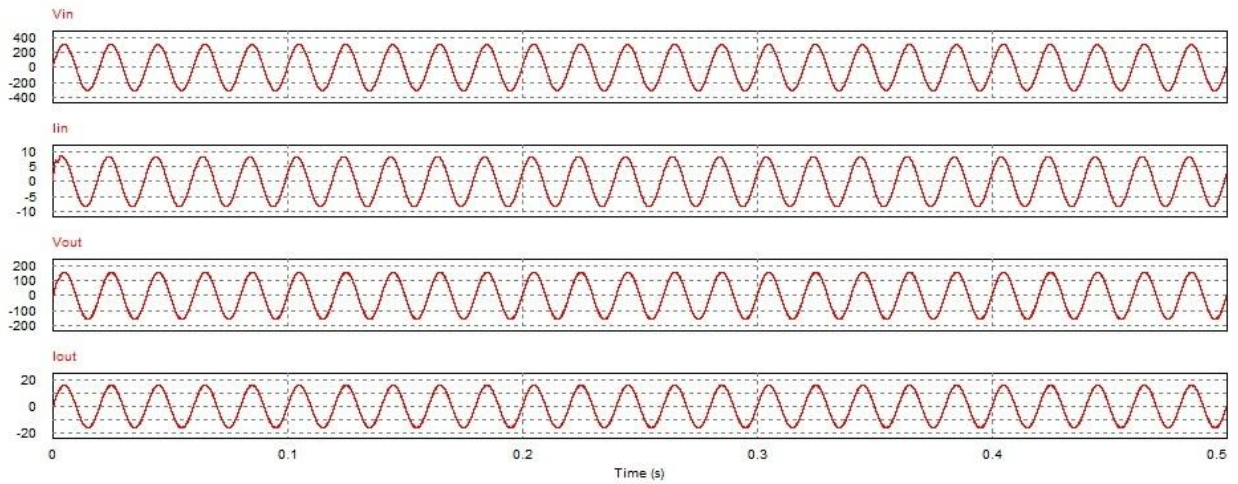
**Fig.: 3.6.2.g THD Vs Duty Cycle at 20kHz**

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & I/P Volatge) | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|--------------------------------|----------------|
| 0.1              | 0.9              | 36                | 1.52701             | 2.148179             | 21.48179             | 0.182431              | 0.146447                       | 97.27733       |
| 0.2              | 0.8              | 72                | 1.774809            | 4.297774             | 42.97774             | 0.500719              | 0.493543                       | 99.40407       |
| 0.3              | 0.7              | 108               | 2.535058            | 6.447343             | 64.47343             | 0.190551              | 0.774487                       | 99.80525       |
| 0.4              | 0.6              | 144               | 3.868229            | 8.603535             | 86.03535             | 0.037026              | 0.902936                       | 99.90304       |
| 0.5              | 0.5              | 180               | 5.718941            | 10.76239             | 107.6239             | 0.03352               | 0.955337                       | 99.93986       |
| 0.6              | 0.4              | 216               | 8.042439            | 12.91866             | 129.1866             | 0.022315              | 0.978657                       | 99.95631       |
| 0.7              | 0.3              | 252               | 10.81251            | 15.06799             | 150.6799             | 0.016581              | 0.990225                       | 99.96417       |
| 0.8              | 0.2              | 288               | 14.01262            | 17.20612             | 172.0612             | 0.011305              | 0.996277                       | 99.96783       |
| 0.9              | 0.1              | 324               | 17.63254            | 19.32962             | 193.2962             | 0.006641              | 0.999216                       | 99.96924       |

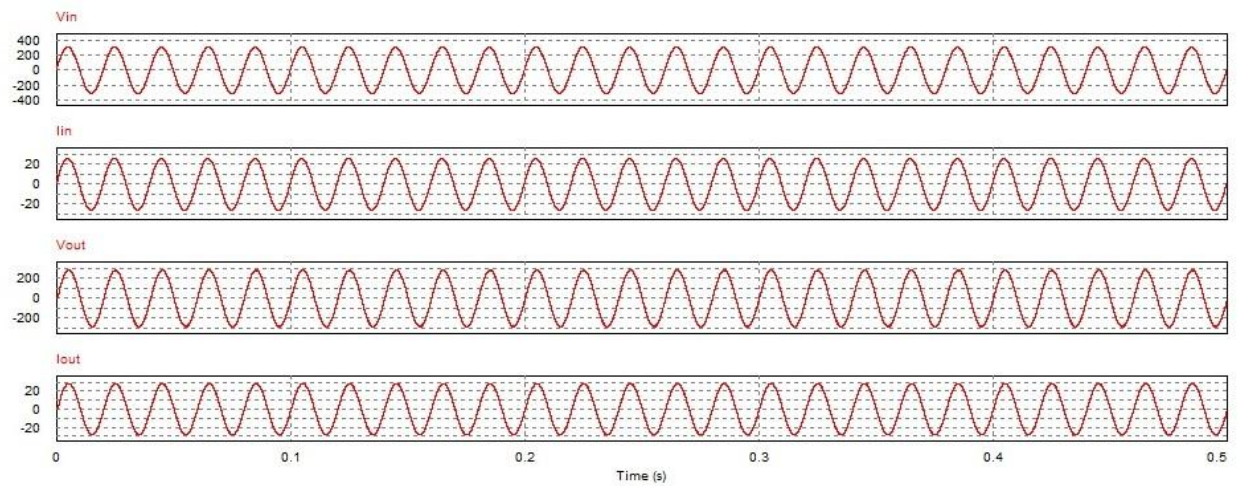
**Fig.: 3.6.3 Buck Topology with Filter Performance at 30kHz**



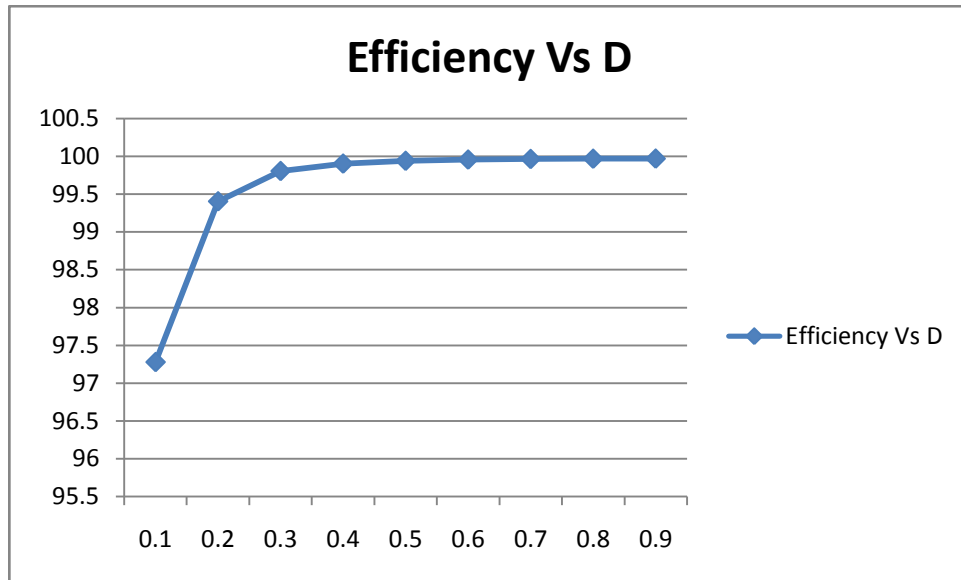
**Fig. 3.6.3.a Output and input of wave shape for duty cycle 0.1 with 30KHz frequency**



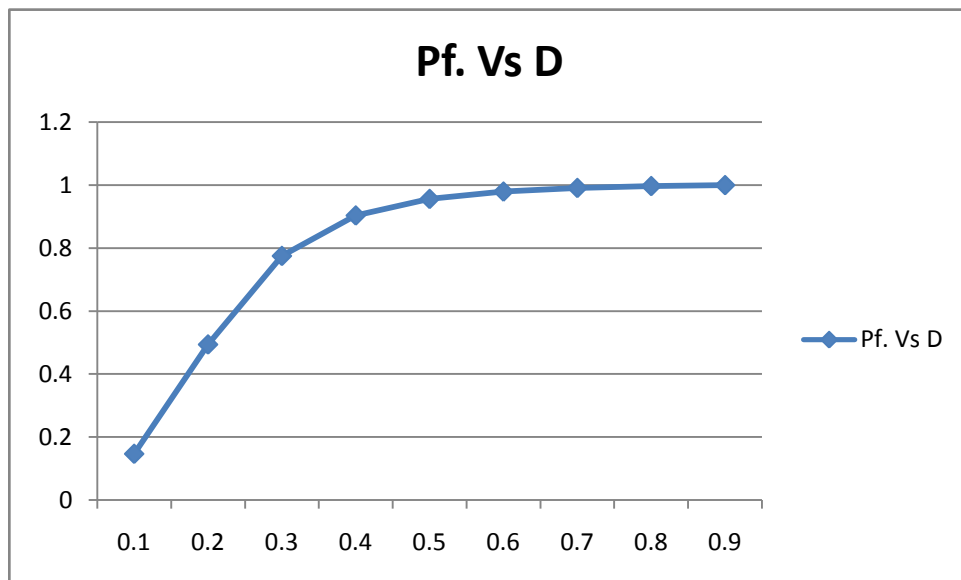
**Fig. 3.6.3.b Output and input of wave shape for duty cycle 0.5 with 30KHz frequency**



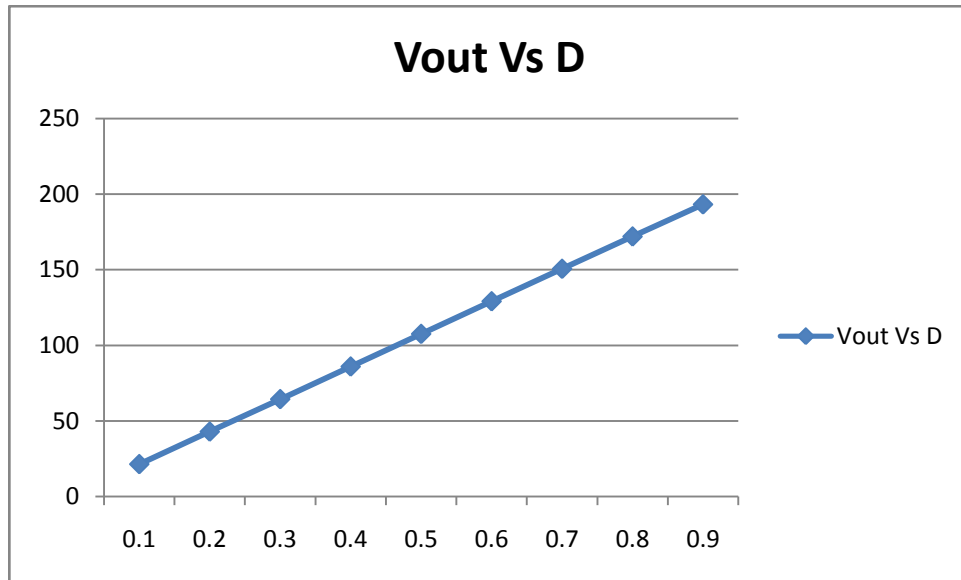
**Fig. 3.6.3.c Output and input of wave shape for duty cycle 0.9 with 30KHz frequency**



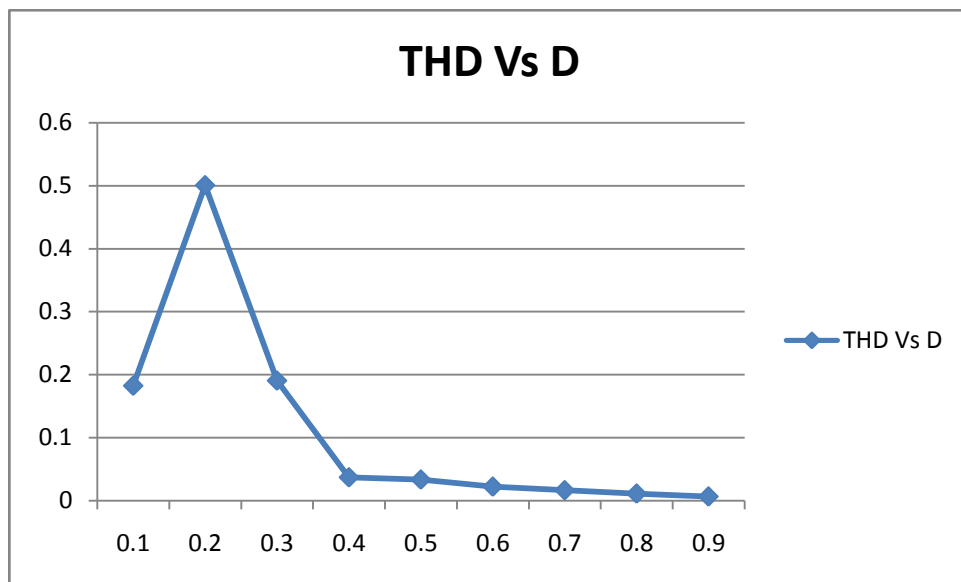
**Fig.: 3.6.3.d Efficiency Vs Duty Cycle at 30 kHz**



**Fig.: 3.6.3.e Power Factor Vs Duty Cycle at 30 kHz**



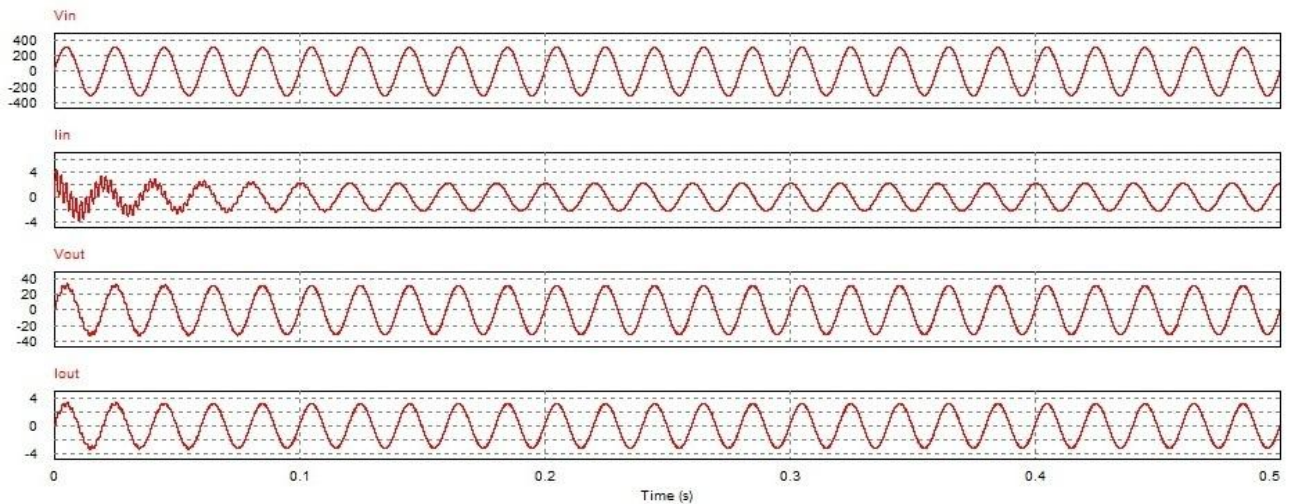
**Fig.: 3.6.3.f Output Voltage Vs Duty Cycle at 30 kHz**



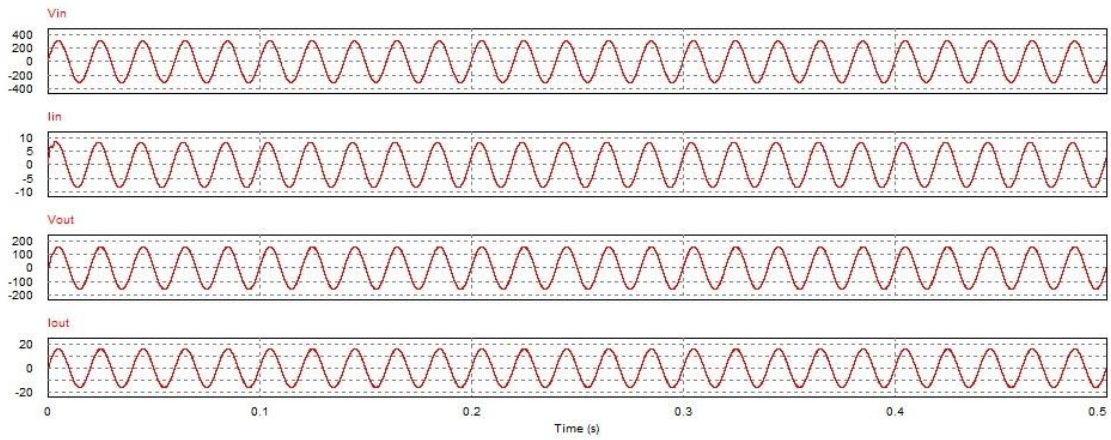
**Fig.: 3.6.3.g THD Vs Duty Cycle at 30 kHz**

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & I/P Volatge) | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|--------------------------------|----------------|
| 0.1              | 0.9              | 36                | 1.528147            | 2.144368             | 21.44368             | 0.102176              | 0.145954                       | 97.18786       |
| 0.2              | 0.8              | 72                | 1.774654            | 4.290921             | 42.90921             | 0.190397              | 0.492045                       | 99.39757       |
| 0.3              | 0.7              | 108               | 2.532878            | 6.441484             | 64.41484             | 0.106104              | 0.774034                       | 99.76805       |
| 0.4              | 0.6              | 144               | 3.862515            | 8.595709             | 85.95709             | 0.046918              | 0.902822                       | 99.88146       |
| 0.5              | 0.5              | 180               | 5.709035            | 10.75187             | 107.5187             | 0.022544              | 0.955255                       | 99.92629       |
| 0.6              | 0.4              | 216               | 8.029251            | 12.90712             | 129.0712             | 0.012877              | 0.978611                       | 99.94643       |
| 0.7              | 0.3              | 252               | 10.79893            | 15.05773             | 150.5773             | 0.009901              | 0.990202                       | 99.95594       |
| 0.8              | 0.2              | 288               | 14.00275            | 17.19934             | 171.9934             | 0.007193              | 0.996269                       | 99.96033       |
| 0.9              | 0.1              | 324               | 17.62935            | 19.32717             | 193.2717             | 0.005387              | 0.999215                       | 99.96199       |

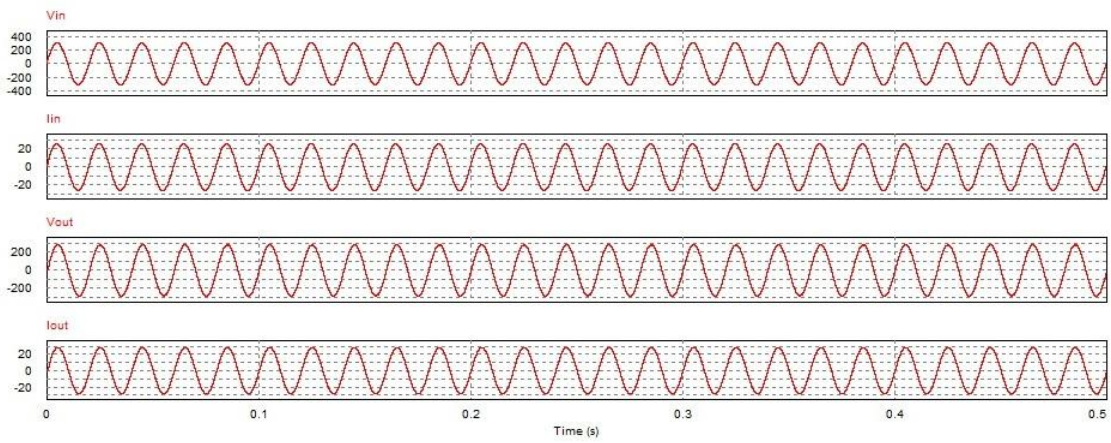
**Fig.: 3.6.4 Buck Topology with Filter Performance at 40kHz**



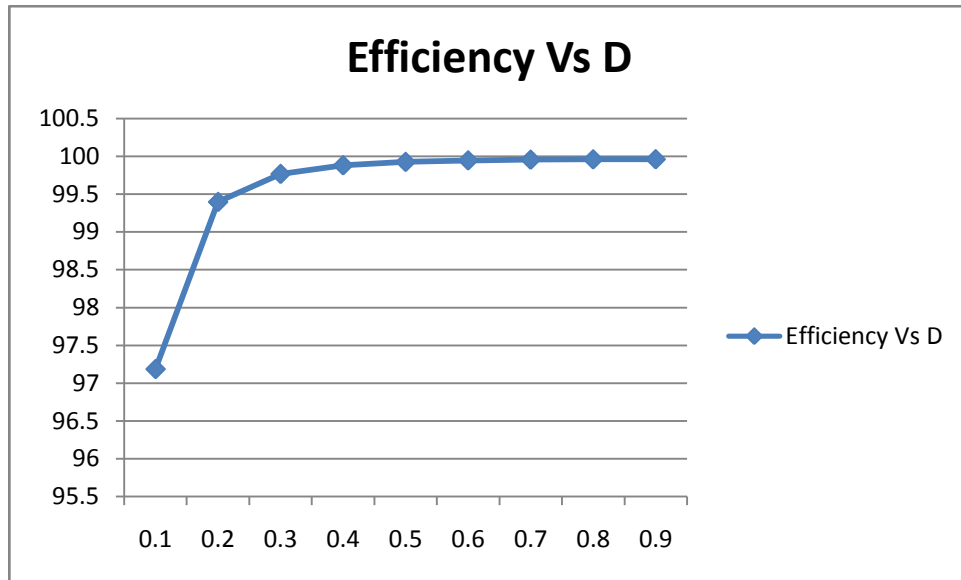
**Fig. 3.6.4.a Output and input of wave shape for duty cycle 0.1 with 40KHz frequency**



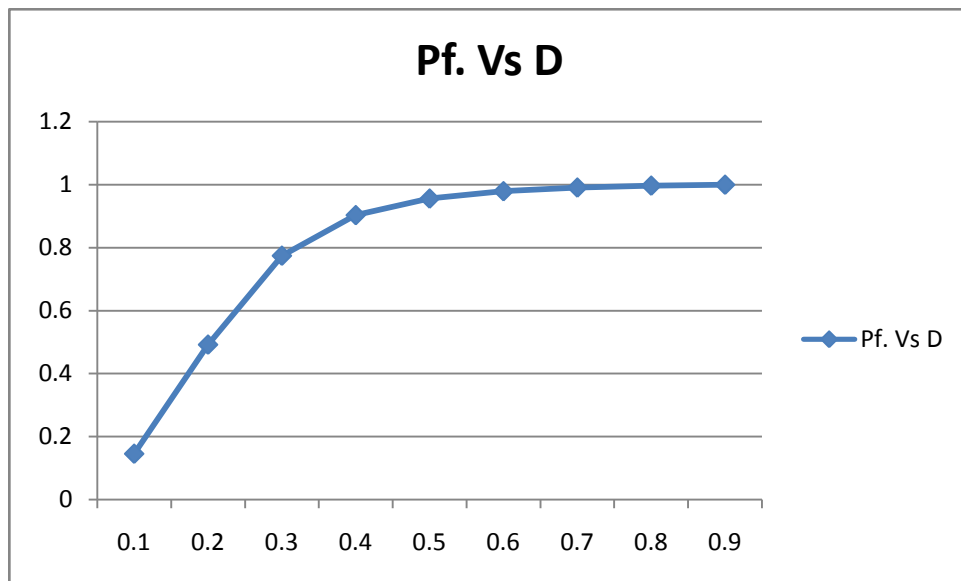
**Fig. 3.6.4.b Output and input of wave shape for duty cycle 0.5 with 40KHz frequency**



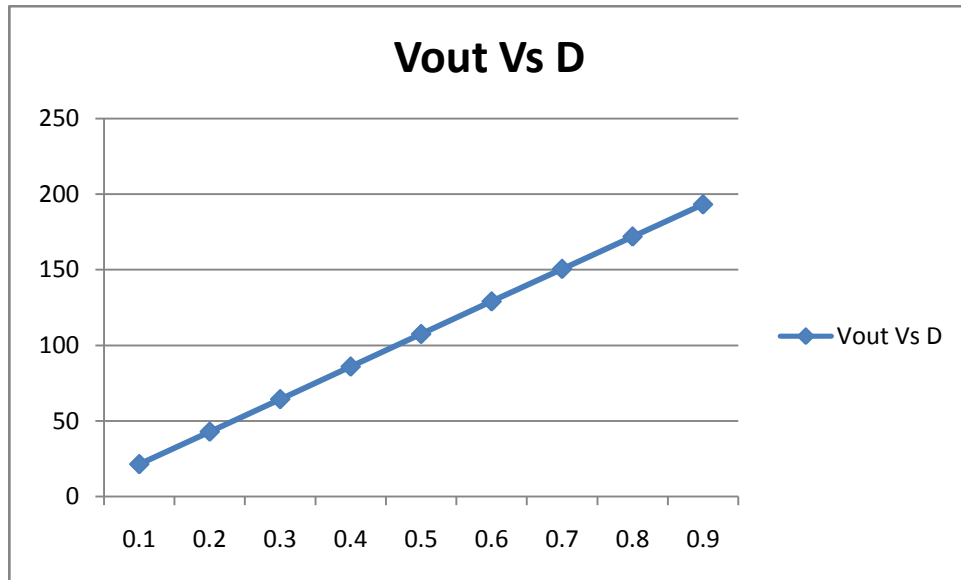
**Fig. 3.6.4.c Output and input of wave shape for duty cycle 0.9 with 40KHz frequency**



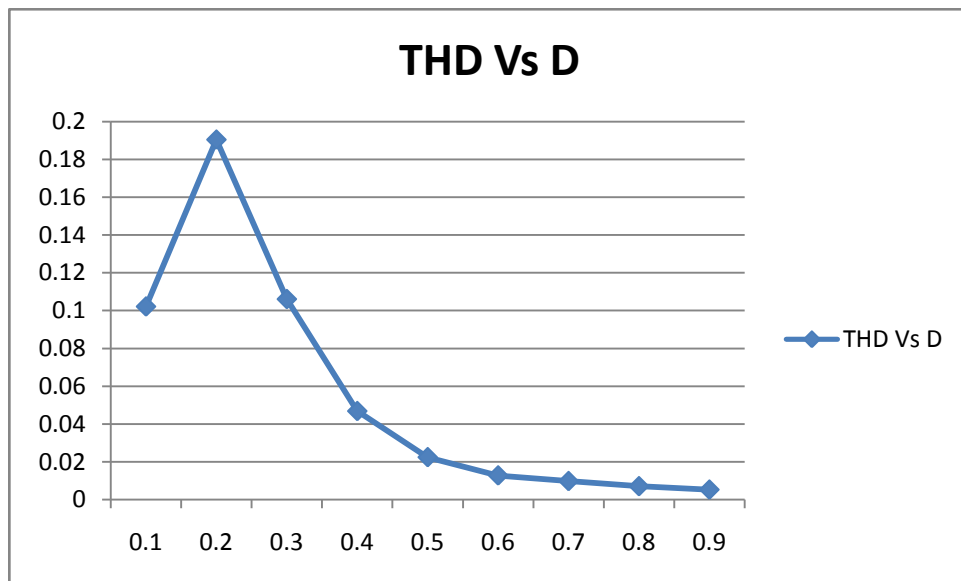
**Fig.: 3.6.4.d Efficiency Vs Duty Cycle at 40 kHz**



**Fig.: 3.6.4.e Power Factor Vs Duty Cycle at 40 kHz**



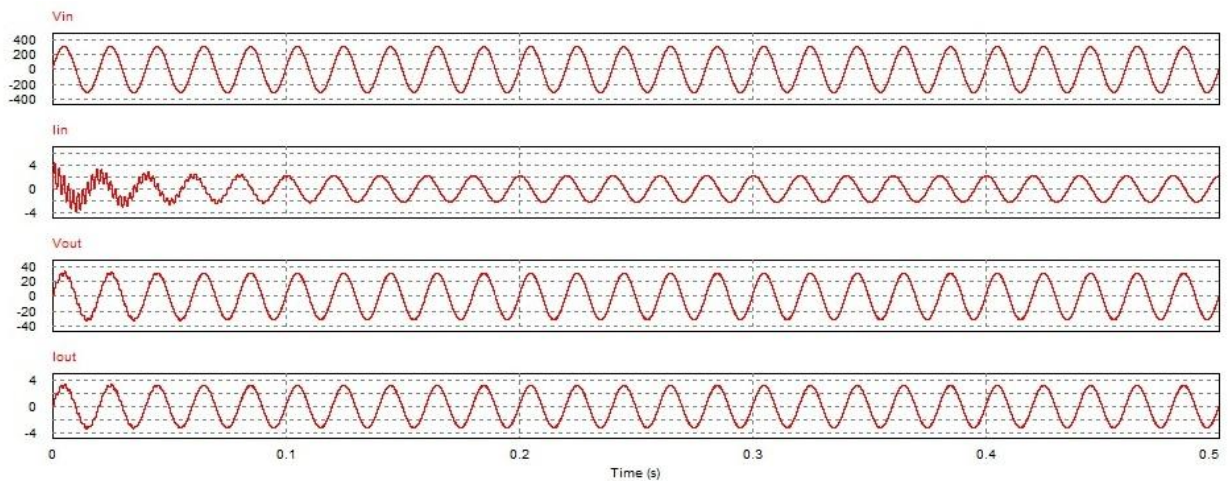
**Fig.: 3.6.4.f Output Voltage Vs Duty Cycle at 40 kHz**



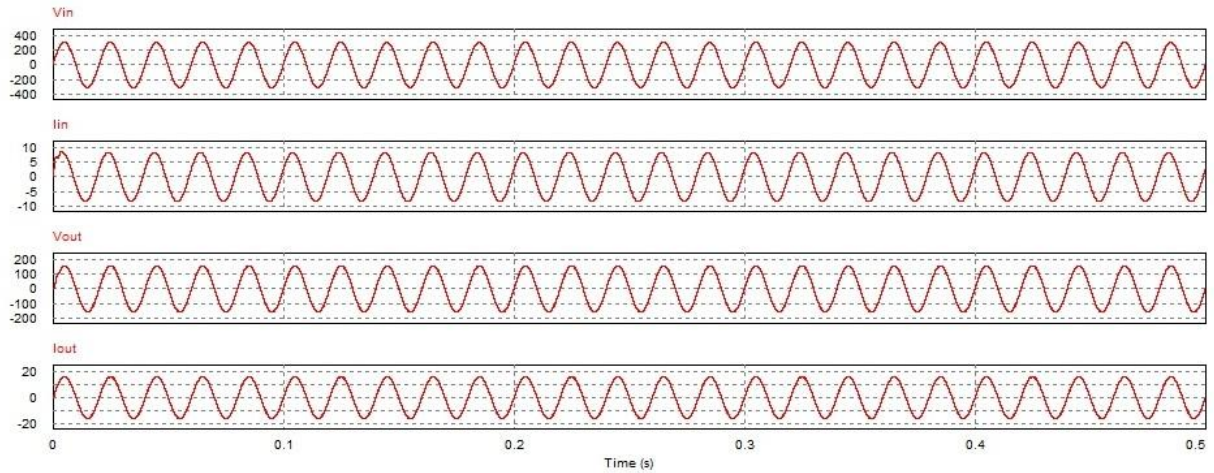
**Fig.: 3.6.4.g THD Vs Duty Cycle at 40 kHz**

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & I/P Volatge) | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|--------------------------------|----------------|
| 0.1              | 0.9              | 36                | 1.528318            | 2.144044             | 21.44044             | 0.057571              | 0.146934                       | 96.49942       |
| 0.2              | 0.8              | 72                | 1.775002            | 4.289987             | 42.89987             | 0.104091              | 0.49248                        | 99.24726       |
| 0.3              | 0.7              | 108               | 2.53247             | 6.439381             | 64.39381             | 0.073156              | 0.7741                         | 99.71044       |
| 0.4              | 0.6              | 144               | 3.860525            | 8.59215              | 85.9215              | 0.045185              | 0.902804                       | 99.85223       |
| 0.5              | 0.5              | 180               | 5.705127            | 10.74707             | 107.4707             | 0.017469              | 0.95523                        | 99.90819       |
| 0.6              | 0.4              | 216               | 8.023864            | 12.90183             | 129.0183             | 0.009309              | 0.978595                       | 99.93323       |
| 0.7              | 0.3              | 252               | 10.79343            | 15.05302             | 150.5302             | 0.007097              | 0.990194                       | 99.94503       |
| 0.8              | 0.2              | 288               | 13.99902            | 17.19619             | 171.9619             | 0.005891              | 0.996267                       | 99.95043       |
| 0.9              | 0.1              | 324               | 17.62886            | 19.32598             | 193.2598             | 0.004911              | 0.999215                       | 99.95243       |

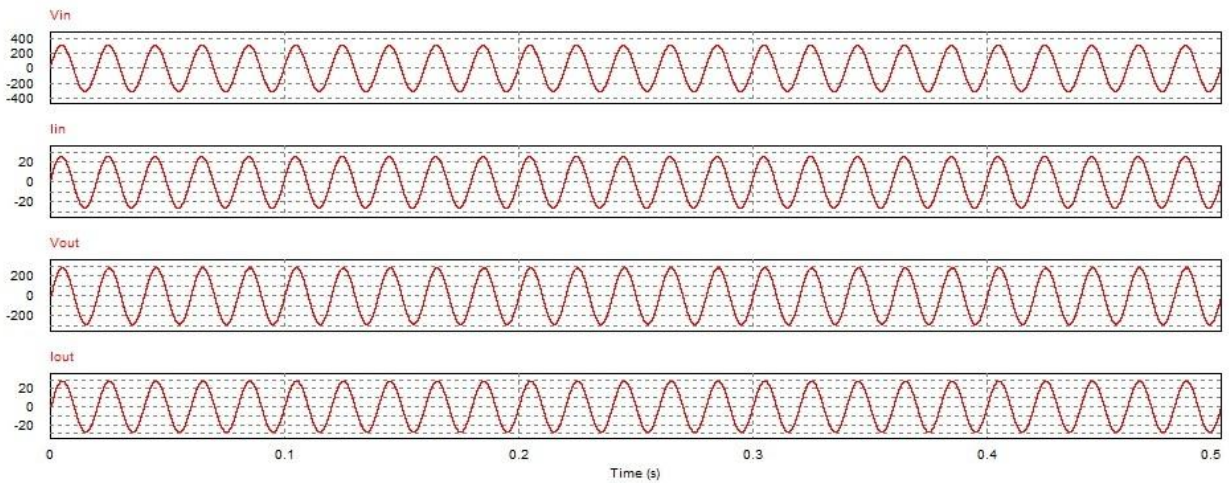
**Fig.: 3.6.5 Buck Topology with Filter Performance at 50kHz**



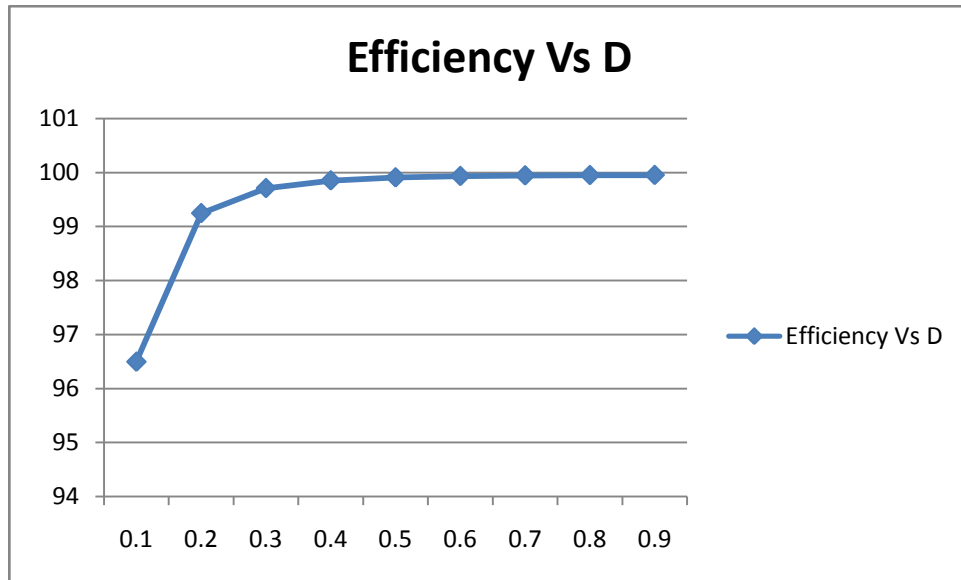
**Fig. 3.6.5.a Output and input of wave shape for duty cycle 0.1 with 50KHz frequency**



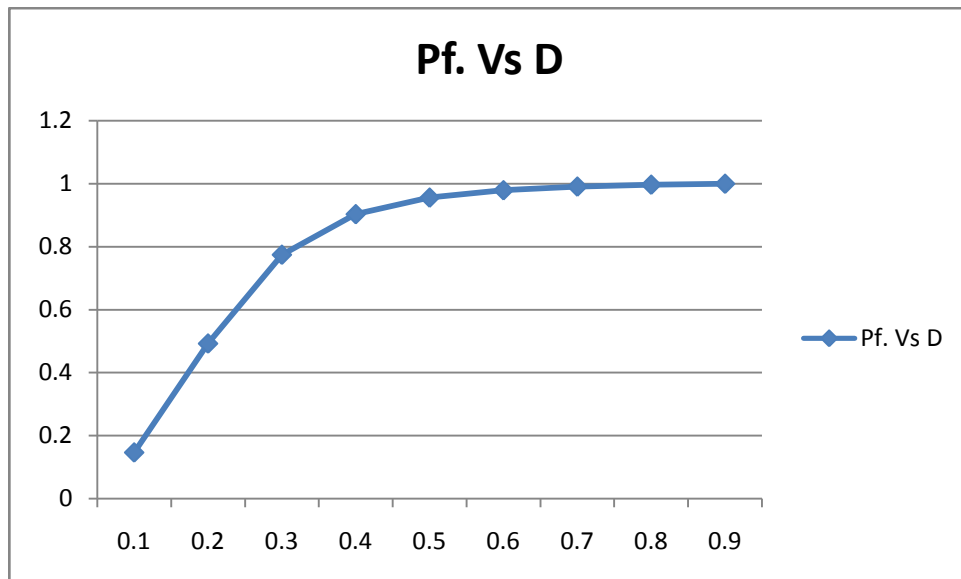
**Fig. 3.6.5.b Output and input of wave shape for duty cycle 0.5 with 50KHz frequency**



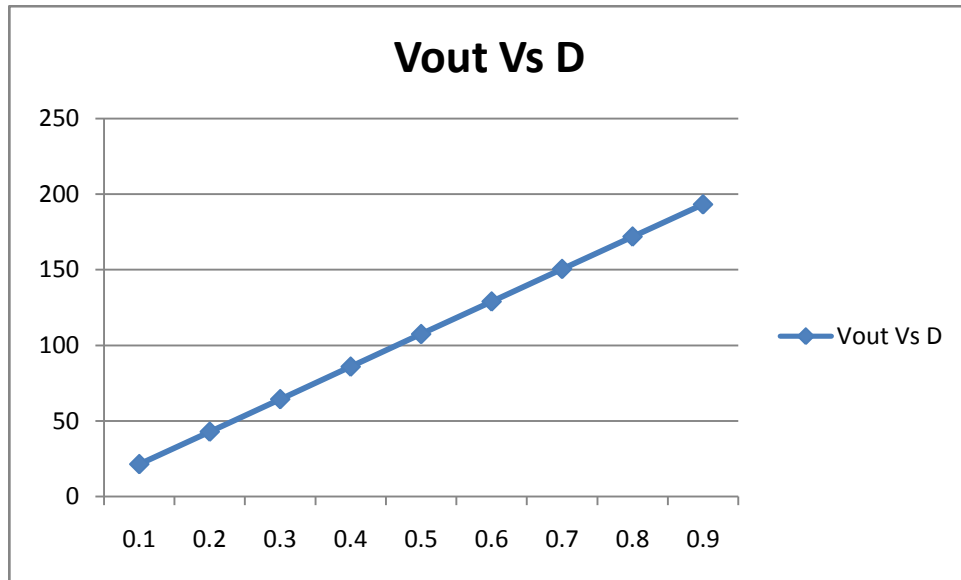
**Fig. 3.6.5.c Output and input of wave shape for duty cycle 0.9 with 50KHz frequency**



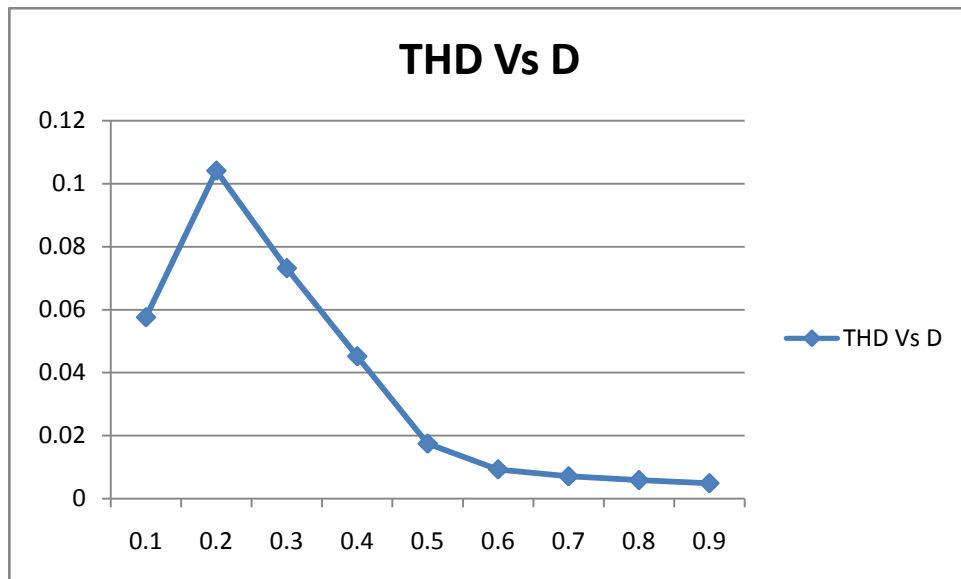
**Fig.: 3.6.5.d Efficiency Vs Duty Cycle at 50 kHz**



**Fig.: 3.6.5.e Power Factor Vs Duty Cycle at 50 kHz**



**Fig.: 3.6.5.f Output Voltage Vs Duty Cycle at 50 kHz**



**Fig.: 3.6.5.g THD Vs Duty Cycle at 50 kHz**

# **CHAPTER 4**

## **BOOST CONVERTER**

# 4.0 BOOST CONVERTER

## 4.1 BOOST CONVERTER

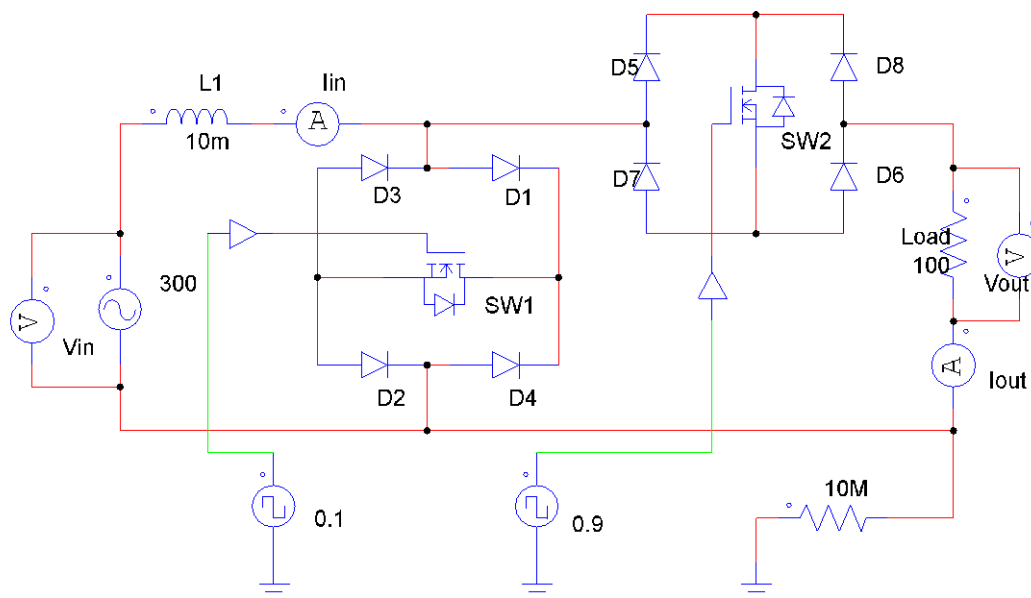
A **boost converter (step-up converter)** is a power converter with an output voltage greater than its input voltage. It is a class of switching-mode power supply (SMPS) containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple. A boost converter is sometimes called a step-up converter since it “steps up” the source voltage.<sup>11</sup>

## 4.2 BASIC OPERATION OF BOOST TOPOLOGY

The BOOST converter is also controlled by two bi-directional MOSFET switches. The condition of controlling the switches is as same as buck topology. In positive half cycle, when switch 1 (SW1) is closed, the input current will flow through the inductor L1 and SW1. L1 get energized and the current return to the source. When SW2 is on, the input current will flow through the load. At the same moment L1 also supply current at the same direction and the combination of these two current will result a big amount of voltage drop at load. In negative half cycle, when SW1 is on, input current passes through SW1 and L1 and L1 get energized. When SW2 is on the combination of input current and inductor current passes through the load and again makes a huge voltage drop at load. L1,C1 and L2,C2 are used for reducing input and output harmonic components. Here for the design condition the load voltage drop will always be higher than source voltage. The output voltage can be controlled by varying duty cycle of PWM.

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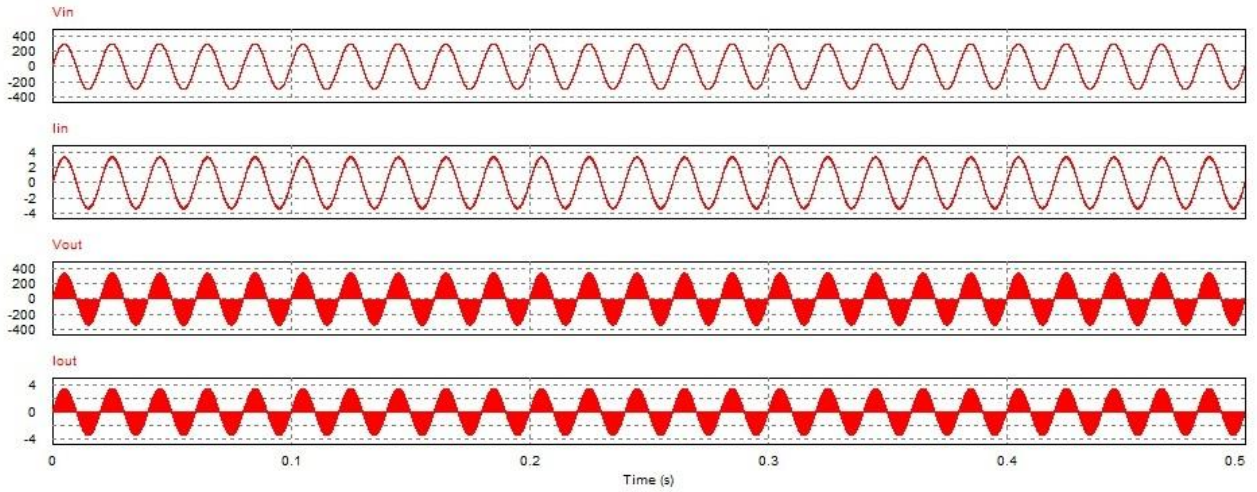
<sup>11</sup> Power Electronics- Circuits, Devices and Applications by Muhammad Harunur Rashid



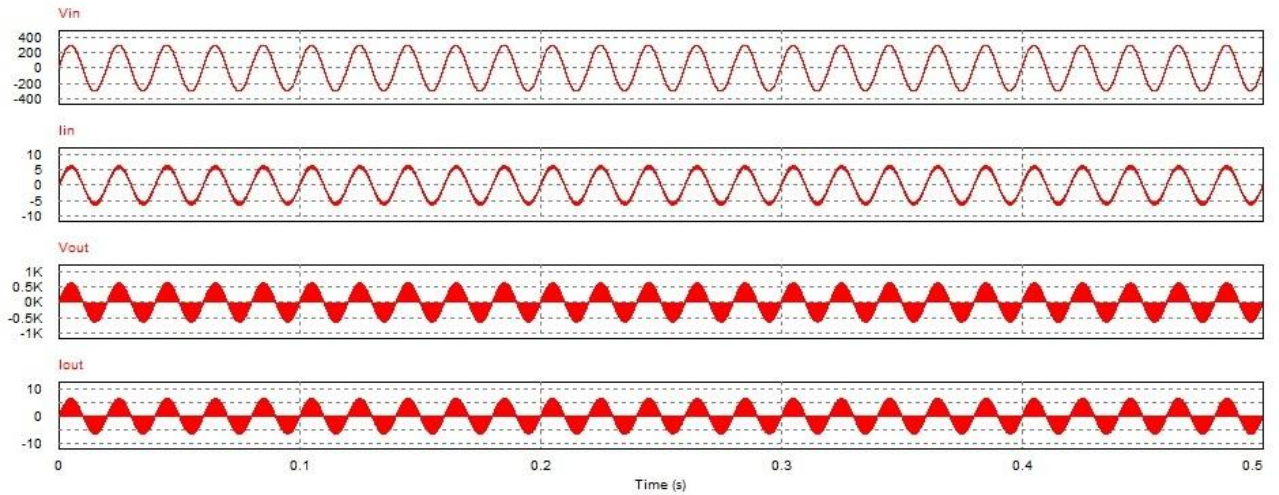
### 4.3 WAVE FORMS AND DATA SHEET OF BOOST TOPOLOGY CIRCUIT

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & I/P Volatge | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|-------------------------------|----------------|
| 0.1              | 0.9              | 36                | 2.3563915           | 2.2350318            | 223.50318            | 1.3074282             | 0.99930791                    | 100.0033112    |
| 0.2              | 0.8              | 72                | 2.6521492           | 2.3708391            | 237.08391            | 2.3175444             | 0.99896445                    | 100.0114942    |
| 0.3              | 0.7              | 108               | 3.0323364           | 2.5346716            | 253.46716            | 3.038578              | 0.99853701                    | 100.022011     |
| 0.4              | 0.6              | 144               | 3.5383534           | 2.7375027            | 273.75027            | 3.4704375             | 0.99803499                    | 100.0358993    |
| 0.5              | 0.5              | 180               | 4.2448279           | 2.9976713            | 299.76713            | 3.6137453             | 0.99738454                    | 100.0550568    |
| 0.6              | 0.4              | 216               | 5.3006945           | 3.3485178            | 334.85178            | 3.4690687             | 0.99633324                    | 100.0832884    |
| 0.7              | 0.3              | 252               | 7.050784            | 3.8583844            | 385.83844            | 3.0365831             | 0.9941021                     | 100.1235746    |
| 0.8              | 0.2              | 288               | 10.507817           | 4.6968211            | 469.68211            | 2.3163077             | 0.98760324                    | 100.2090113    |
| 0.9              | 0.1              | 324               | 20.330663           | 6.4276641            | 642.76641            | 1.3125344             | 0.95376587                    | 100.4400121    |

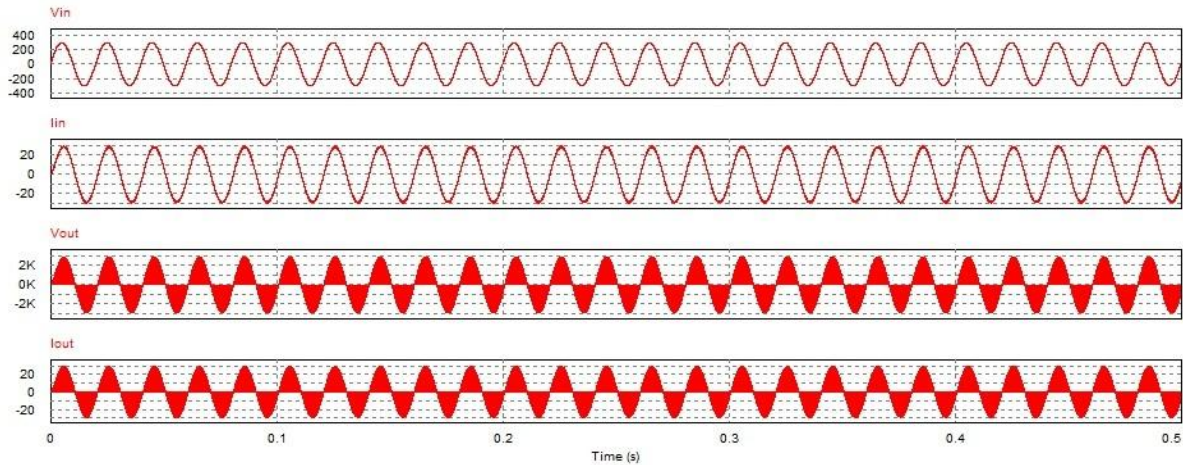
**Fig. 4.3.1 Data Sheet of a Basic BOOST circuit performance at 20kHz**



**Fig. 4.3.2 Output and input of wave shape for duty cycle 0.1 with 20Khz frequency**



**Fig. 4.3.3 Output and input of wave shape for duty cycle 0.5 with 20Khz frequency**



**Fig. 4.3.4 Output and input of wave shape for duty cycle 0.9 with 20Khz frequency**

## 4.4 BOOST TOPOLOGY WITH FILTER DESIGN

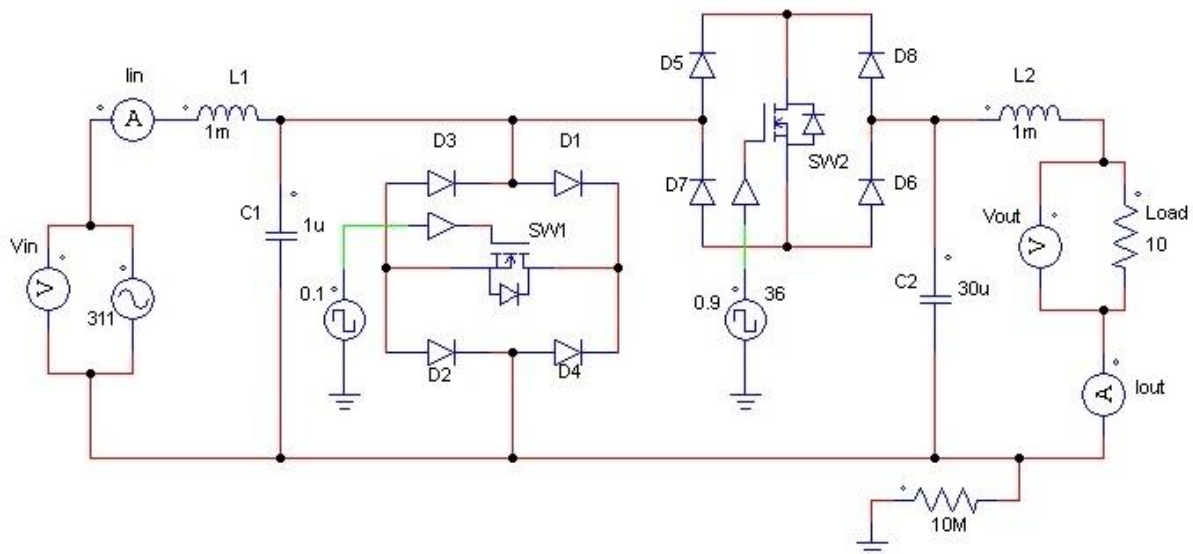
Used formulae to find the parameters:

$$L1 = D(1-D)^2 / (2(f2))$$

$$L1C1 = 1 / (2\pi(f1))^2$$

$$\Delta V_o / V_o = D / R(C2)(f2)$$

Here ripple voltage is assumed 5%. (f1) is the desired frequency (5000). (f2) is switching frequency (Let 20kHz).

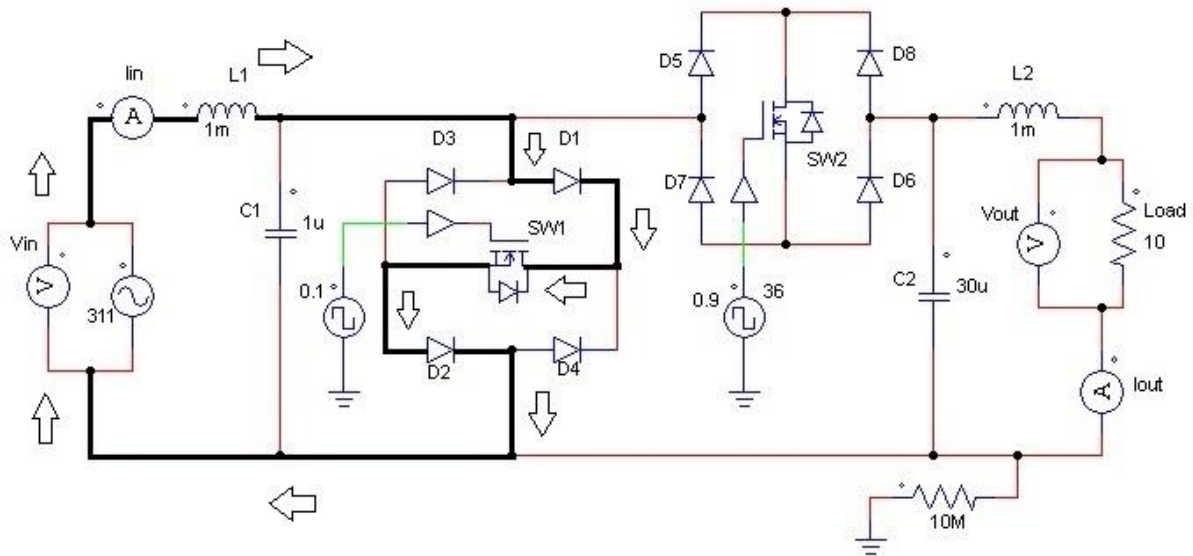


**Fig.: 4.4.1 Boost Topology with Filter**

## 4.5 CURRENT FLOW DIAGRAMS

### For +ve half cycle with SW1 on

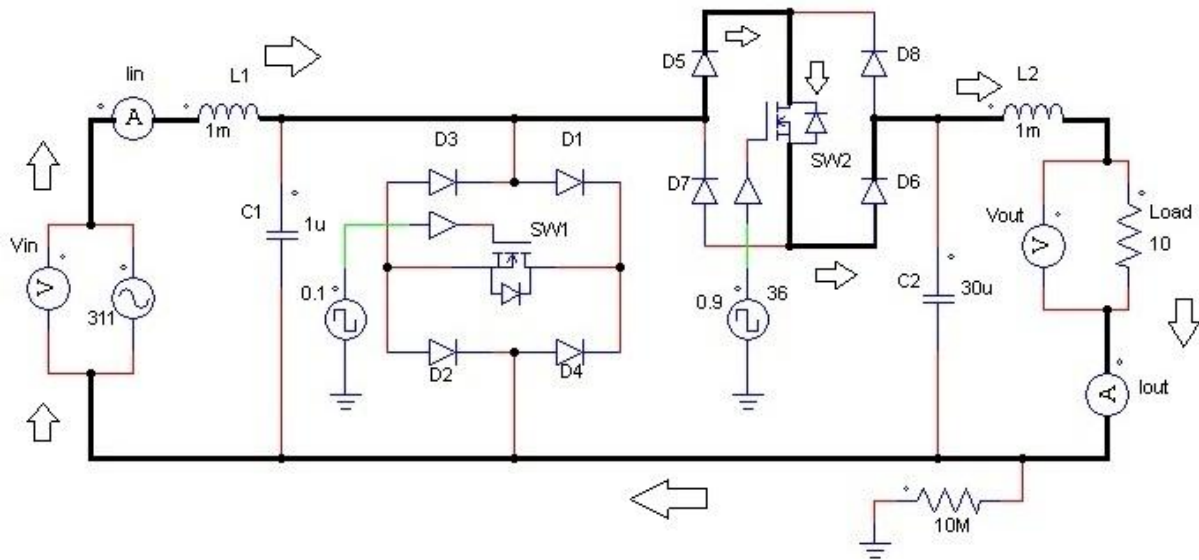
The input current will flow through L1 and SW1 and then return to the source. L1 get energized and both L1 and C1 are reducing the input harmonic components.



**Fig.: 4.5.1 Current flow diagram of Boost Topology with Filter for (+ve) cycle when sw1 active.**

### For +ve half cycle with SW2 on

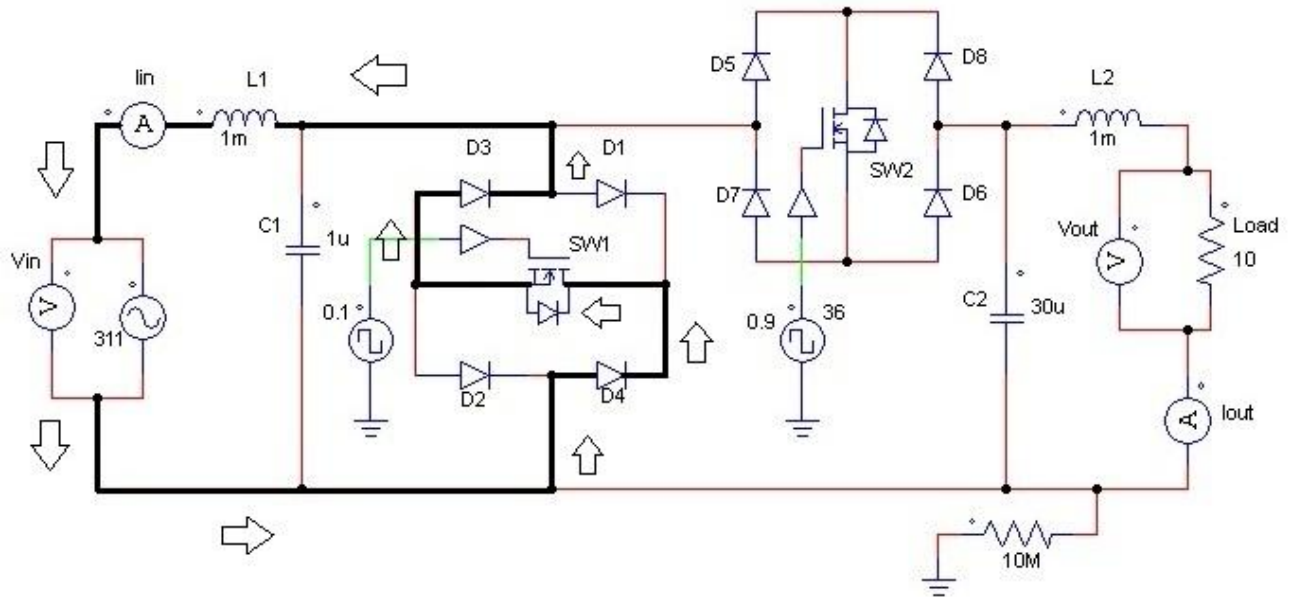
The input current will flow through L1, SW2 and load and then it will return to the source. Here the combination of input and the inductor current makes a large amount of voltage drop at load.



**Fig.: 4.5.2 Current flow diagram of Boost Topology with Filter for (+ve) cycle when sw2 active**

### For -ve half cycle with SW1 on

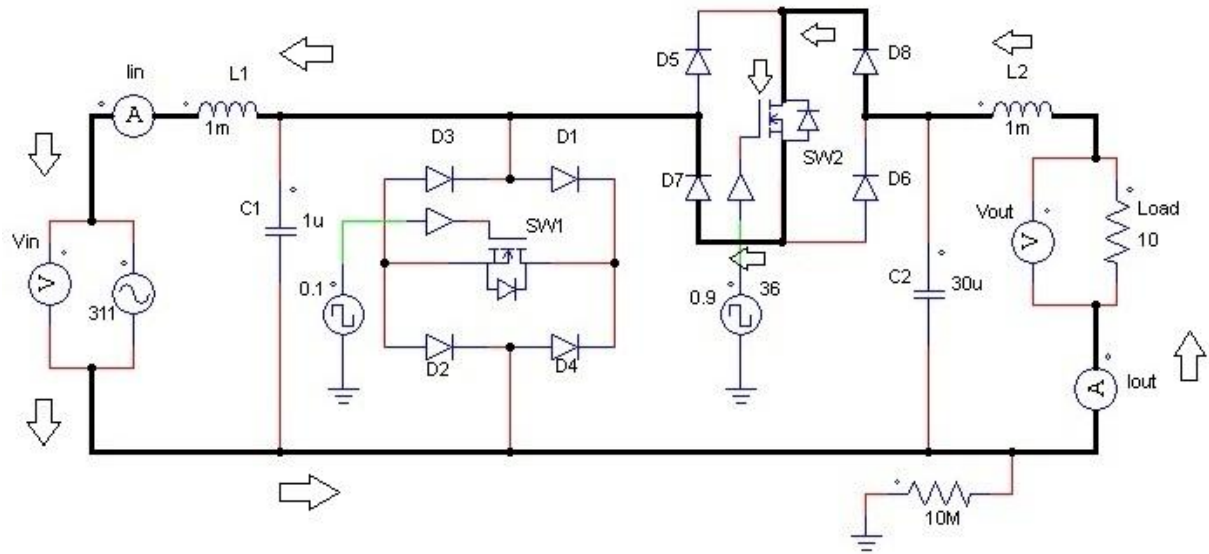
The negative input current passes through SW1 and L1 and return to the source. L1 get energized.



**Fig.: 4.5.3 Current flow diagram of Boost Topology with Filter for (-ve) cycle when sw1 active**

**For +ve half cycle with SW2 on**

Combination of negative input current and the inductor current make huge voltage drop at load and return to the source through SW2.

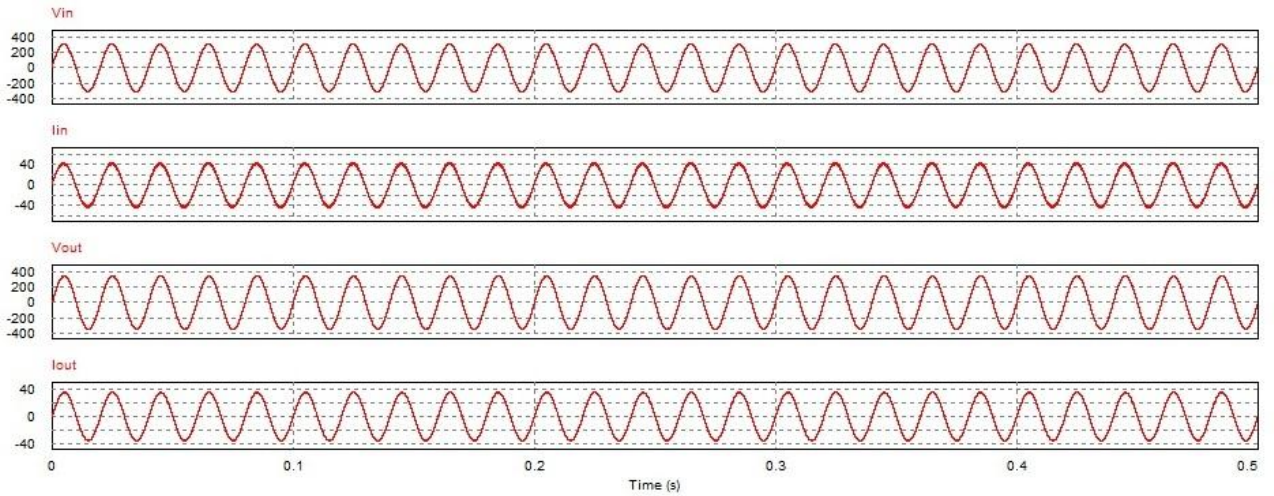


**Fig.: 4.5.4 Current flow diagram of Boost Topology with Filter for (-ve) cycle when sw2 active.**

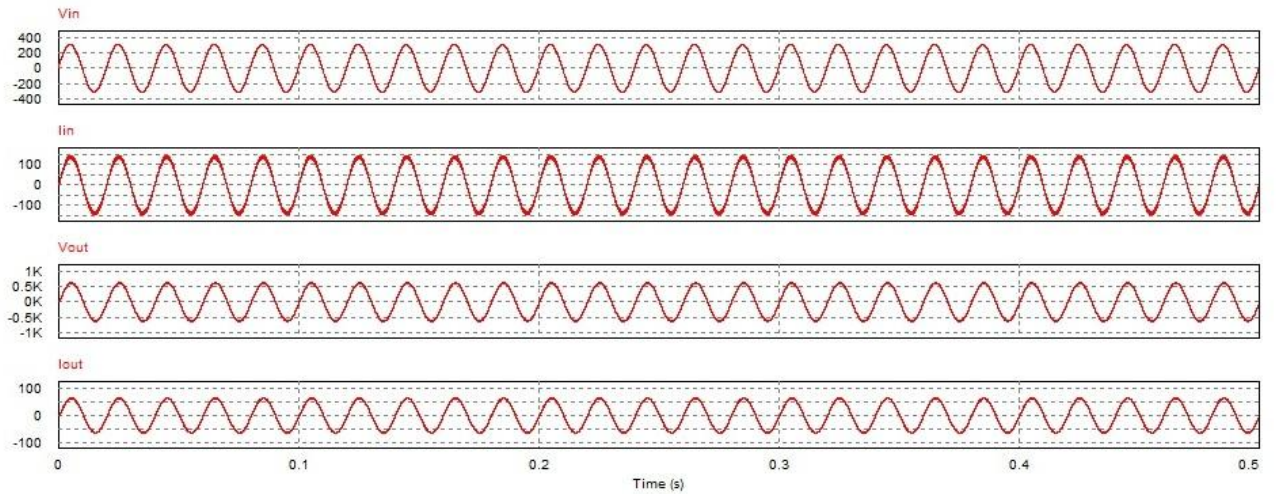
## 4.6 DATA ANALYSIS, WAVEFORMS AND CURVES

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & I/P Volatge) | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|--------------------------------|----------------|
| 0.1              | 0.9              | 36                | 30.054              | 24.49429             | 244.9429             | 2.138769              | 0.999631                       | 90.81179       |
| 0.2              | 0.8              | 72                | 38.12305            | 27.58873             | 275.8873             | 3.361482              | 0.999424                       | 90.84073       |
| 0.3              | 0.7              | 108               | 49.88989            | 31.55834             | 315.5834             | 3.84722               | 0.999188                       | 90.84957       |
| 0.4              | 0.6              | 144               | 68.00137            | 36.83105             | 368.3105             | 3.756765              | 0.998562                       | 90.8427        |
| 0.5              | 0.5              | 180               | 97.89529            | 44.1327              | 441.327              | 3.250316              | 0.996148                       | 90.82171       |
| 0.6              | 0.4              | 216               | 151.9064            | 54.70748             | 547.0748             | 2.487561              | 0.9869                         | 90.7818        |
| 0.7              | 0.3              | 252               | 260.194             | 70.16011             | 701.6011             | 1.627008              | 0.948577                       | 90.69126       |
| 0.8              | 0.2              | 288               | 477.2088            | 85.61458             | 856.1458             | 0.82499               | 0.773202                       | 90.33352       |
| 0.9              | 0.1              | 324               | 689.0183            | 61.6799              | 616.799              | 0.250362              | 0.289622                       | 86.69221       |

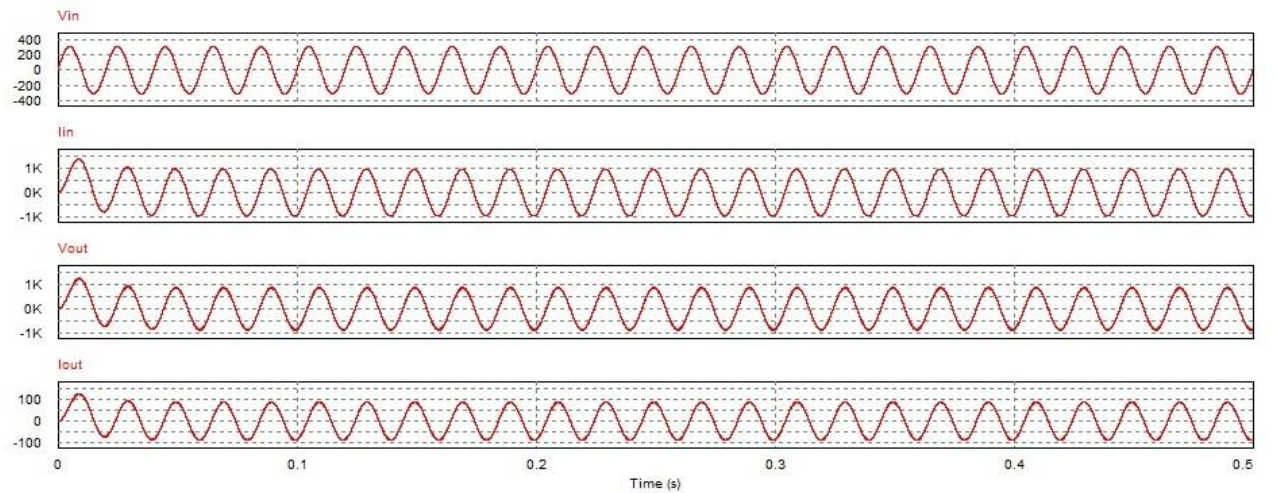
**Fig.: 4.6.1 Boost Topology with Filter Performance at 10kHz**



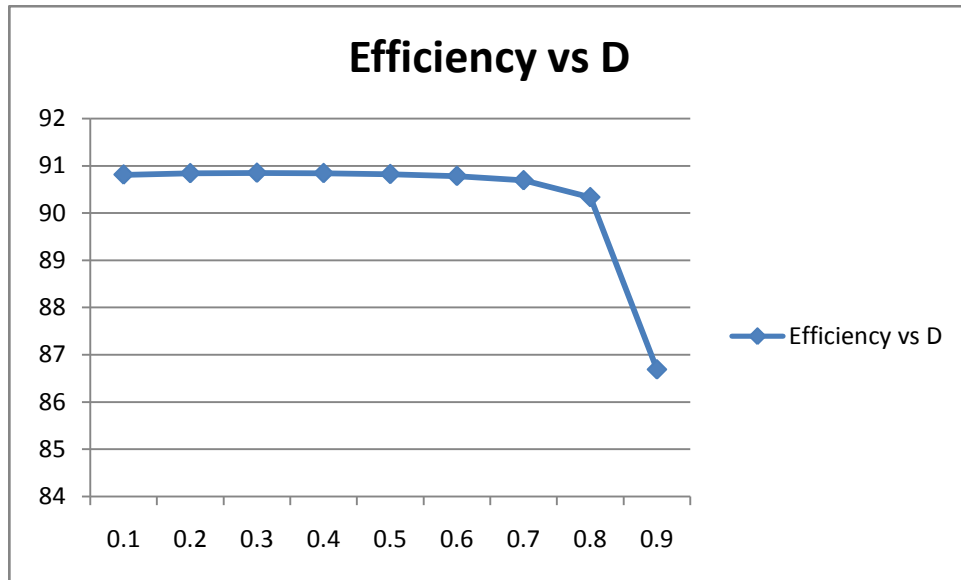
**Fig.: 4.6.1.a Output and input of wave shape for duty cycle 0.1 with 10Khz frequency**



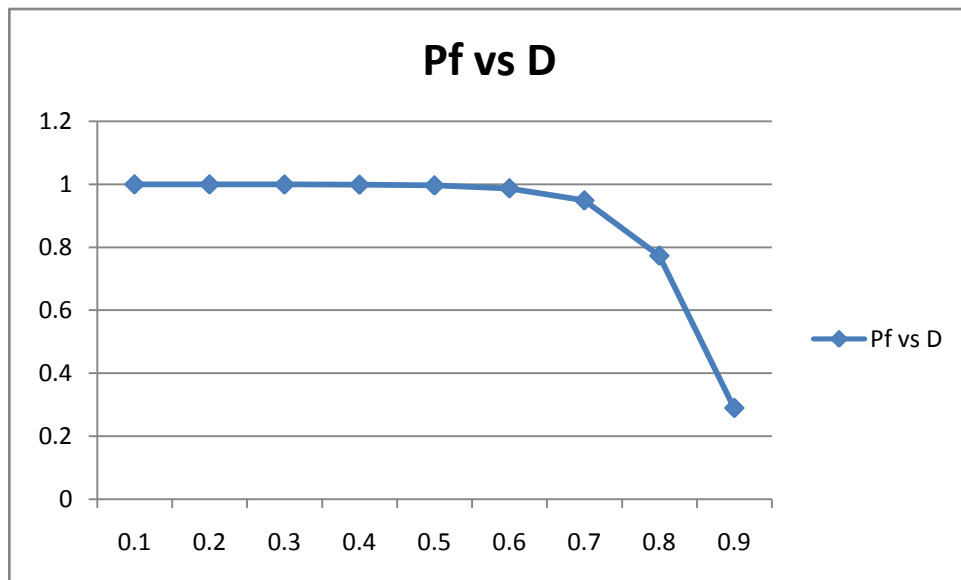
**Fig.: 4.6.1.b Output and input of wave shape for duty cycle 0.5 with 10Khz frequency**



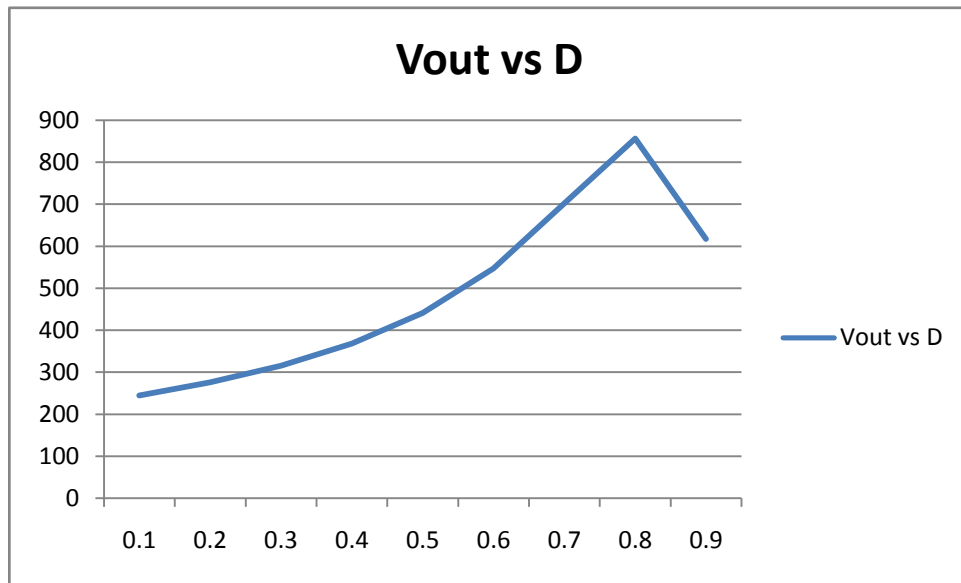
**Fig.: 4.6.1.c Output and input of wave shape for duty cycle 0.9 with 10Khz frequency**



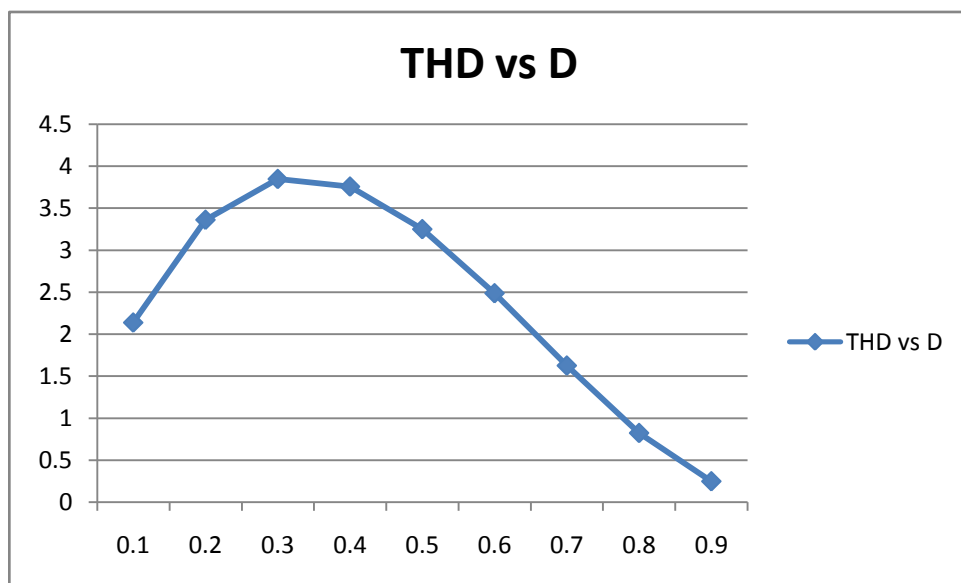
**Fig.: 4.6.1.d Efficiency Vs Duty Cycle at 10kHz**



**Fig.: 4.6.1.e Power Factor Vs Duty Cycle at 10kHz**



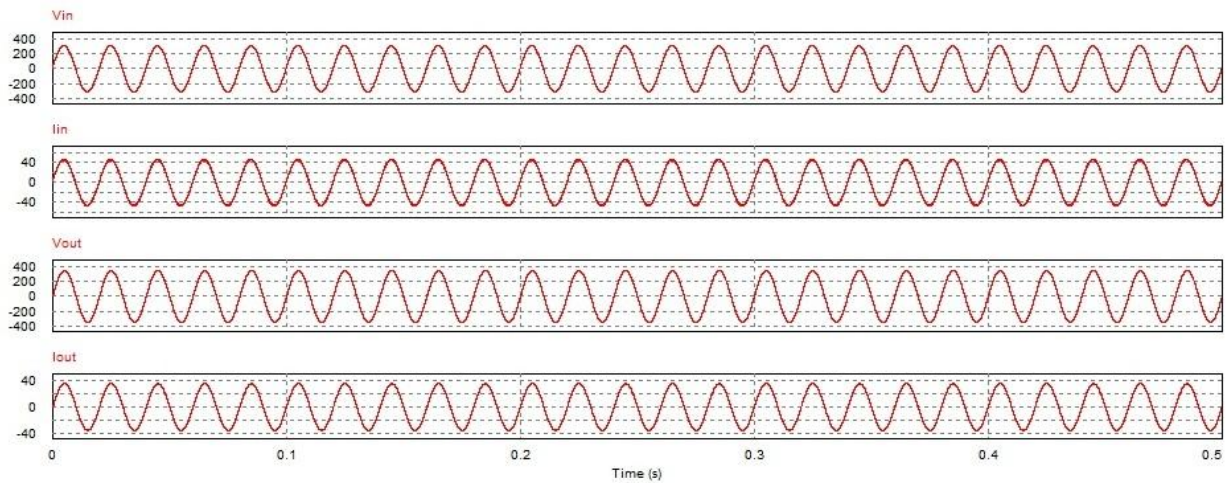
**Fig.: 4.6.1.f Output Voltage Vs Duty Cycle at 10kHz**



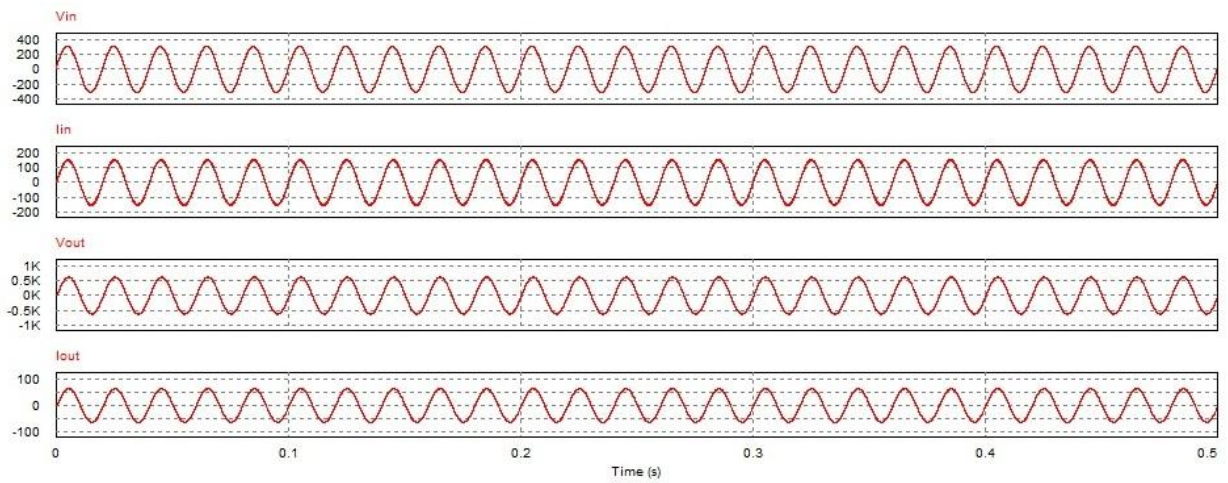
**Fig.: 4.6.1.g THD Vs Duty Cycle at 10kHz**

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & I/P Volatge | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|-------------------------------|----------------|
| 0.1              | 0.9              | 36                | 32.8159             | 24.49196             | 244.9196             | 0.979451              | 0.999922                      | 83.12877       |
| 0.2              | 0.8              | 72                | 41.63574            | 27.59374             | 275.9374             | 1.536529              | 0.99987                       | 83.16985       |
| 0.3              | 0.7              | 108               | 54.49912            | 31.57081             | 315.7081             | 1.75773               | 0.999565                      | 83.20043       |
| 0.4              | 0.6              | 144               | 74.27813            | 36.84172             | 368.4172             | 1.716543              | 0.998486                      | 83.22068       |
| 0.5              | 0.5              | 180               | 106.8331            | 44.10739             | 441.0739             | 1.48611               | 0.994958                      | 83.22748       |
| 0.6              | 0.4              | 216               | 165.2733            | 54.52277             | 545.2277             | 1.138975              | 0.982972                      | 83.20831       |
| 0.7              | 0.3              | 252               | 280.3986            | 69.28807             | 692.8807             | 0.747133              | 0.936766                      | 83.11217       |
| 0.8              | 0.2              | 288               | 498.785             | 82.05461             | 820.5461             | 0.384112              | 0.742617                      | 82.65749       |
| 0.9              | 0.1              | 324               | 690.4781            | 56.71797             | 567.1797             | 0.238248              | 0.274262                      | 77.2469        |

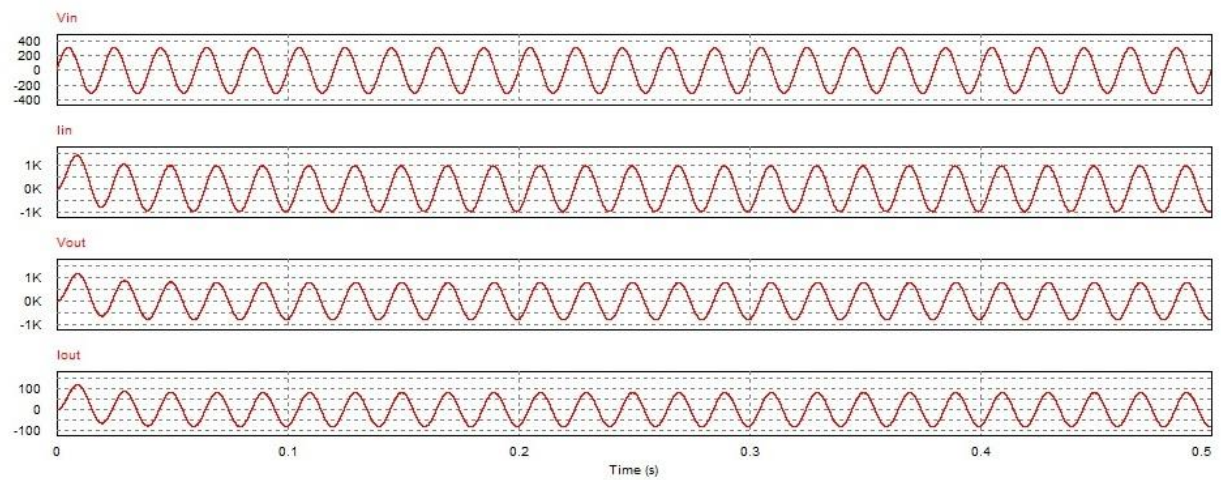
**Fig.: 4.6.2 Boost Topology with Filter Performance at 20kHz**



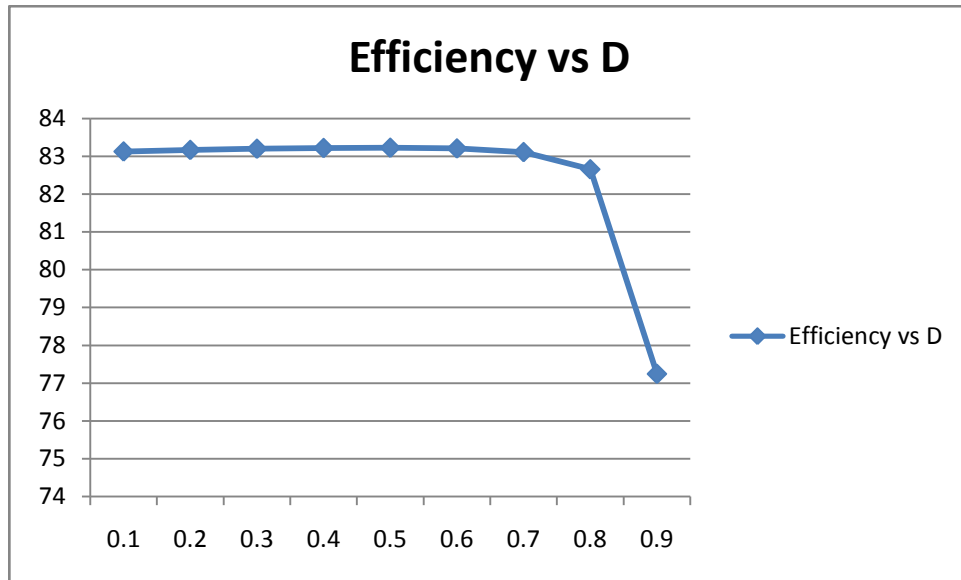
**Fig. 4.6.2.a Output and input of wave shape for duty cycle 0.1 with 20Khz frequency**



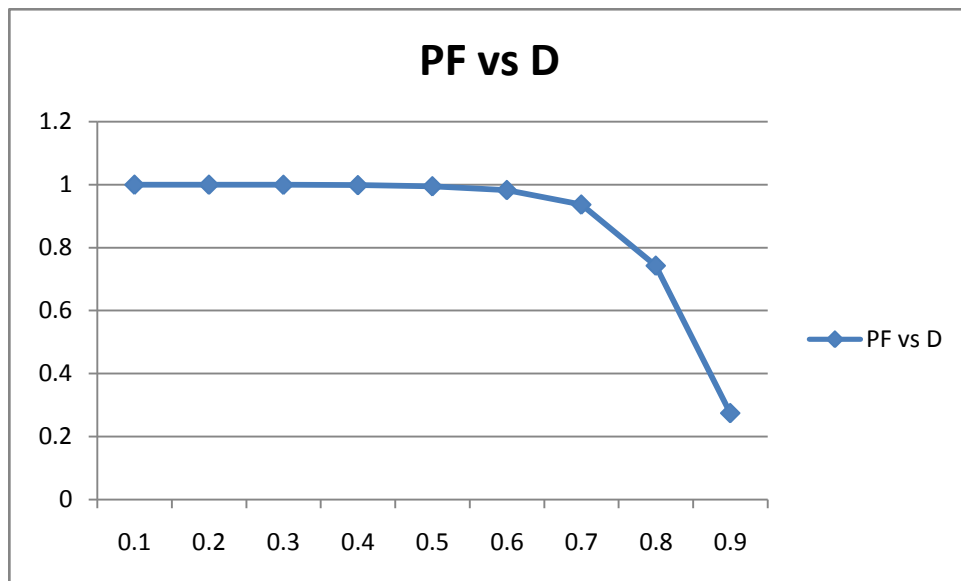
**Fig. 4.6.2.b Output and input of wave shape for duty cycle 0.5 with 20KHz frequency**



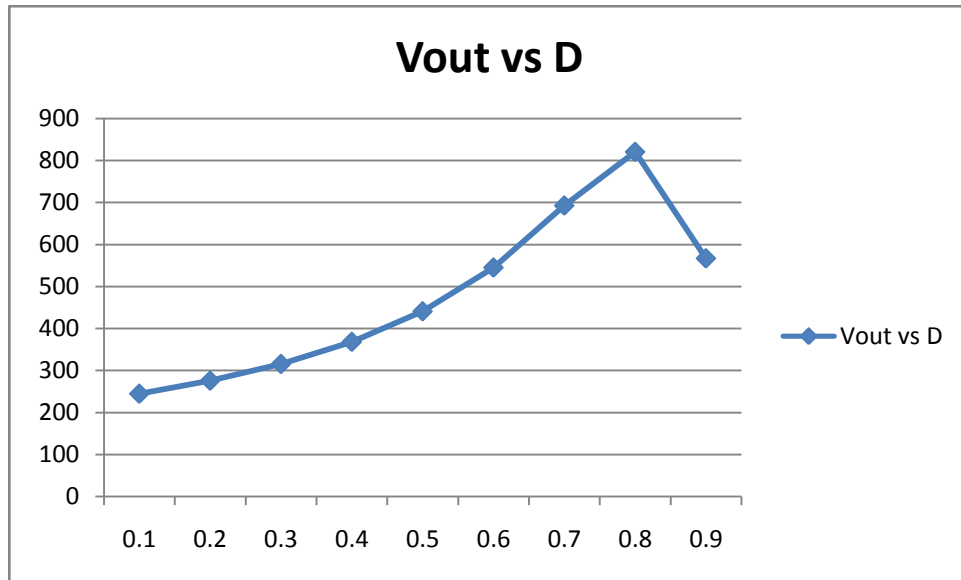
**Fig. 4.6.2.c Output and input of wave shape for duty cycle 0.9 with 20KHz frequency**



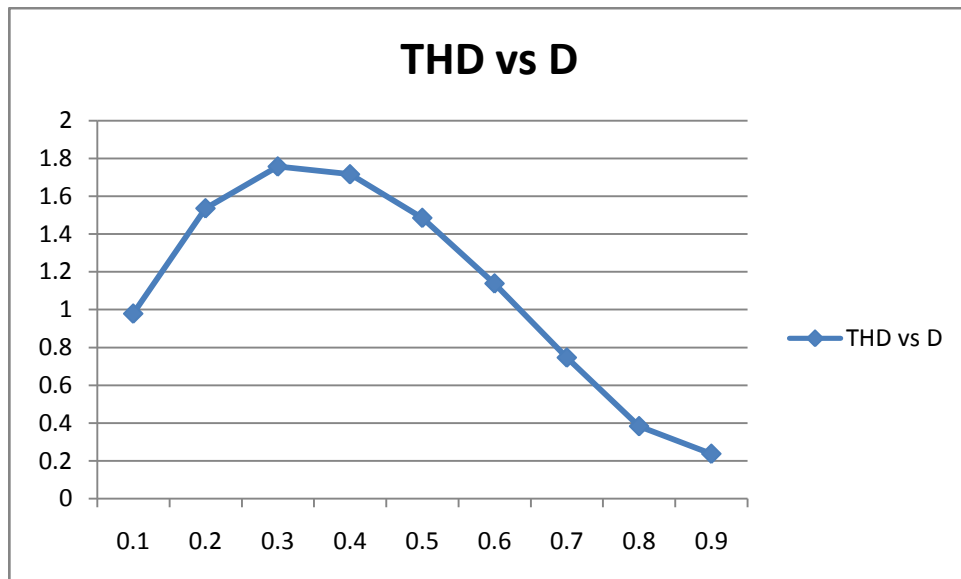
**Fig.: 4.6.2.d Efficiency Vs Duty Cycle at 20kHz**



**Fig.: 4.6.2.e Power Factor Vs Duty Cycle at 20kHz**



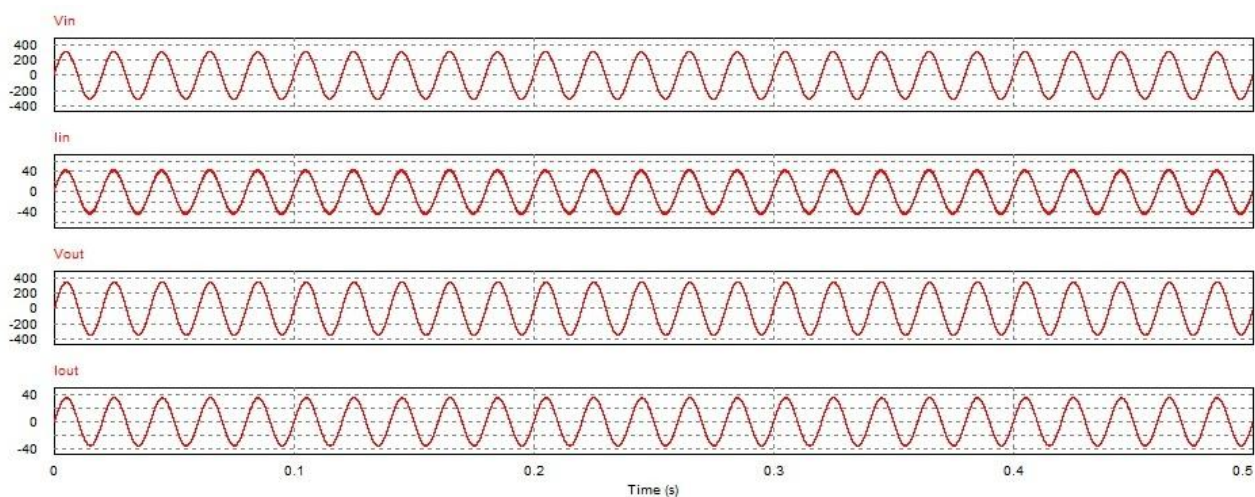
**Fig.: 4.6.2.f Output Voltage Vs Duty Cycle at 20kHz**



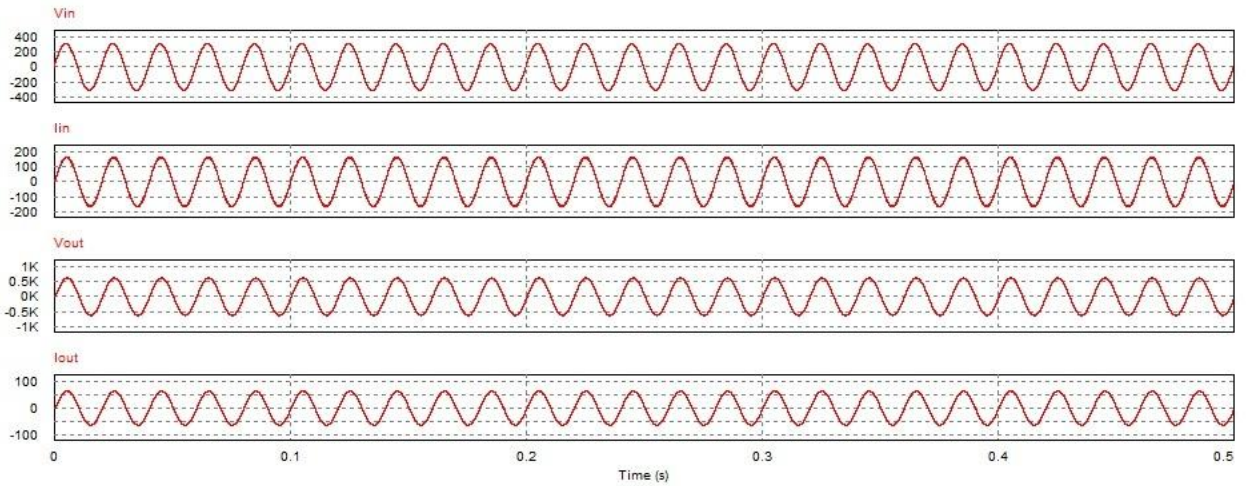
**Fig.: 4.6.2.g THD Vs Duty Cycle at 20kHz**

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & I/P Volatge) | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|--------------------------------|----------------|
| 0.1              | 0.9              | 36                | 35.57               | 24.49                | 244.89               | 0.59                  | 0.99                           | 76.66          |
| 0.2              | 0.8              | 72                | 45.12               | 27.89                | 275.8                | 0.94                  | 0.99                           | 76.72          |
| 0.3              | 0.7              | 108               | 59.04               | 31.56                | 315.63               | 1.07                  | 0.99                           | 76.77          |
| 0.4              | 0.6              | 144               | 80.43               | 36.81                | 368.19               | 1.05                  | 0.99                           | 76.81          |
| 0.5              | 0.5              | 180               | 115.55              | 44.04                | 440.39               | 0.91                  | 0.99                           | 76.84          |
| 0.6              | 0.4              | 216               | 178.24              | 54.29                | 542.95               | 0.69                  | 0.97                           | 76.86          |
| 0.7              | 0.3              | 252               | 299.72              | 68.4                 | 684.06               | 0.45                  | 0.92                           | 76.8           |
| 0.8              | 0.2              | 288               | 518.41              | 78.79                | 787.91               | 0.24                  | 0.71                           | 76.42          |
| 0.9              | 0.1              | 324               | 694.89              | 52.75                | 527.75               | 0.33                  | 0.25                           | 73.14          |

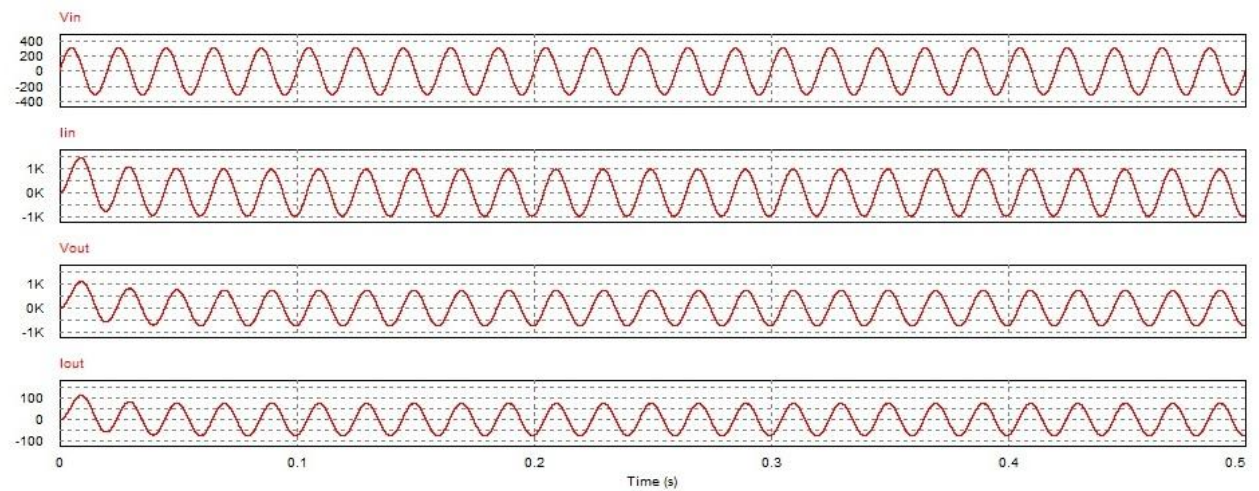
**Fig.: 4.6.3 Boost Topology with Filter Performance at 30kHz**



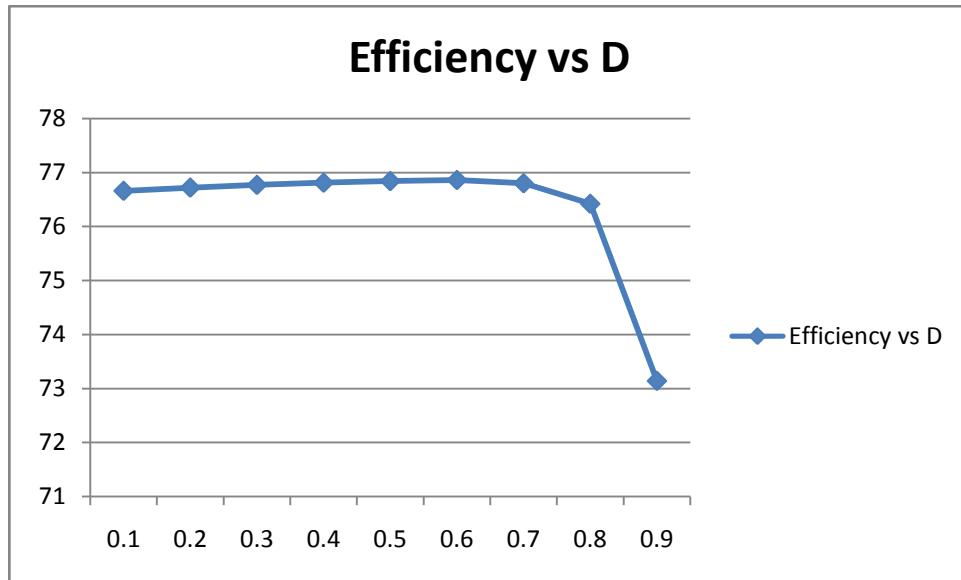
**Fig. 4.6.3.a Output and input of wave shape for duty cycle 0.1 with 30KHz frequency**



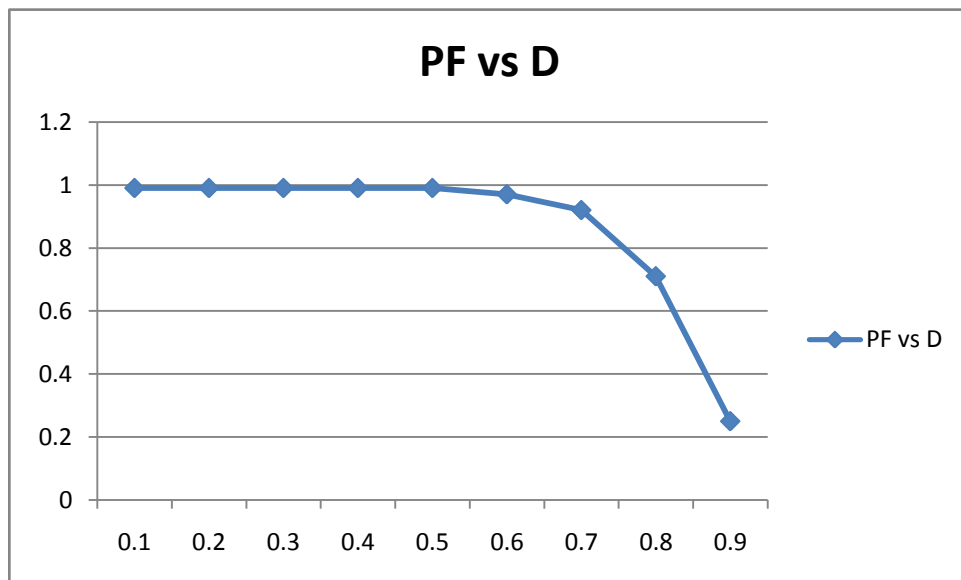
**Fig. 4.6.3.b Output and input of wave shape for duty cycle 0.5 with 30KHz frequency**



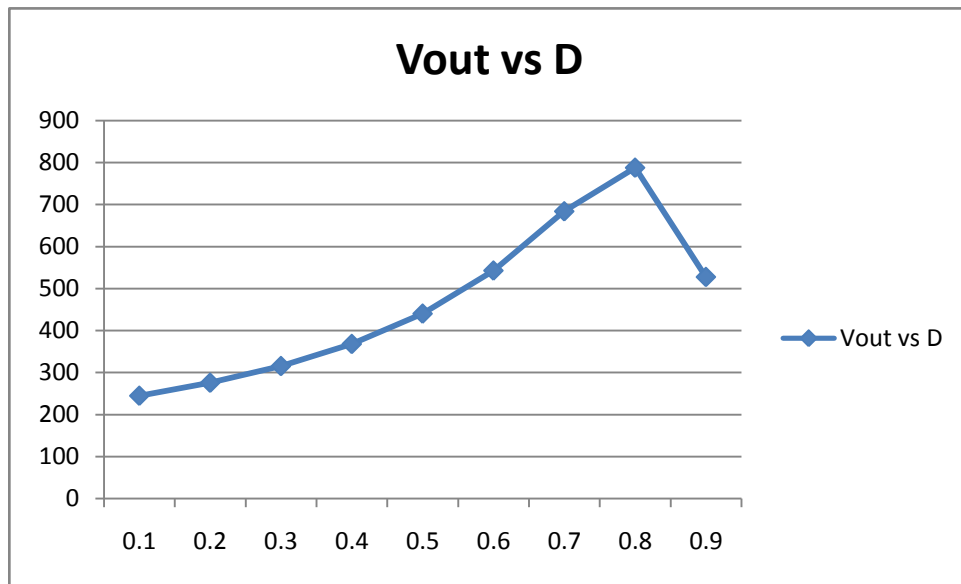
**Fig. 4.6.3.c Output and input of wave shape for duty cycle 0.6 with 30KHz frequency**



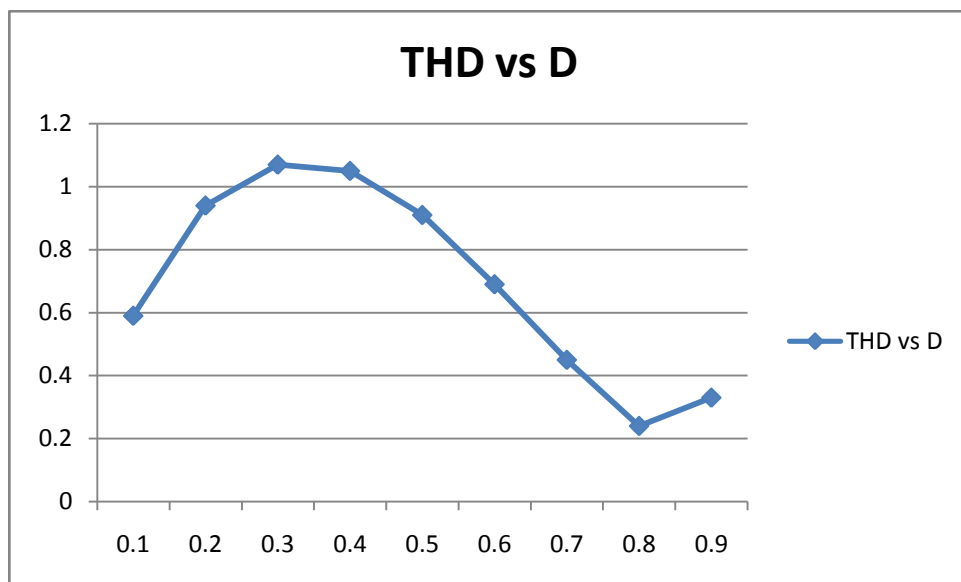
**Fig.: 4.6.3.d Efficiency Vs Duty Cycle at 30 kHz**



**Fig.: 4.6.3.e Power Factor Vs Duty Cycle at 30 kHz**



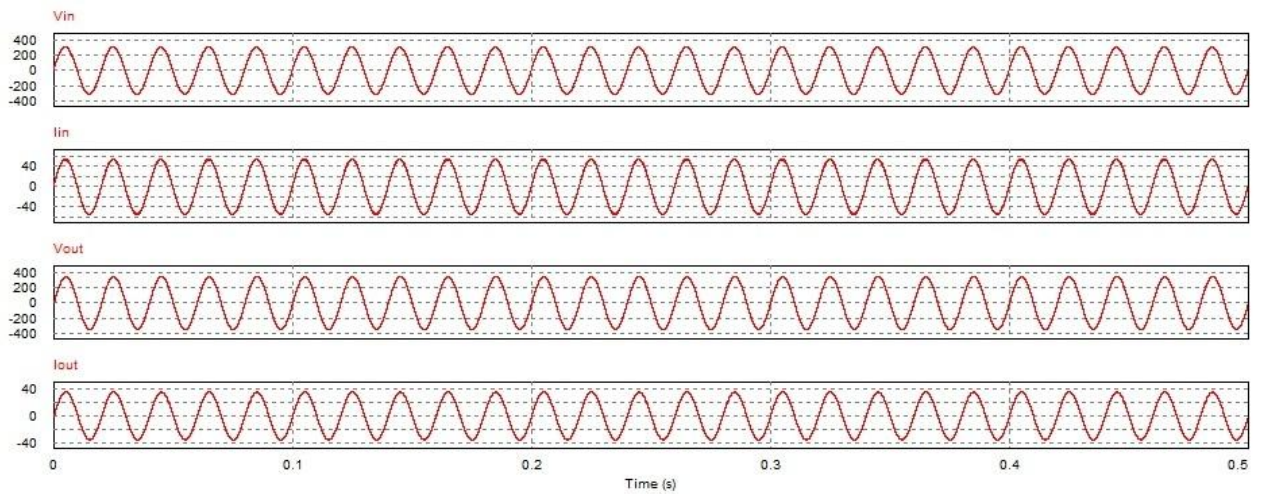
**Fig.: 4.6.3.f Output Voltage Vs Duty Cycle at 30 kHz**



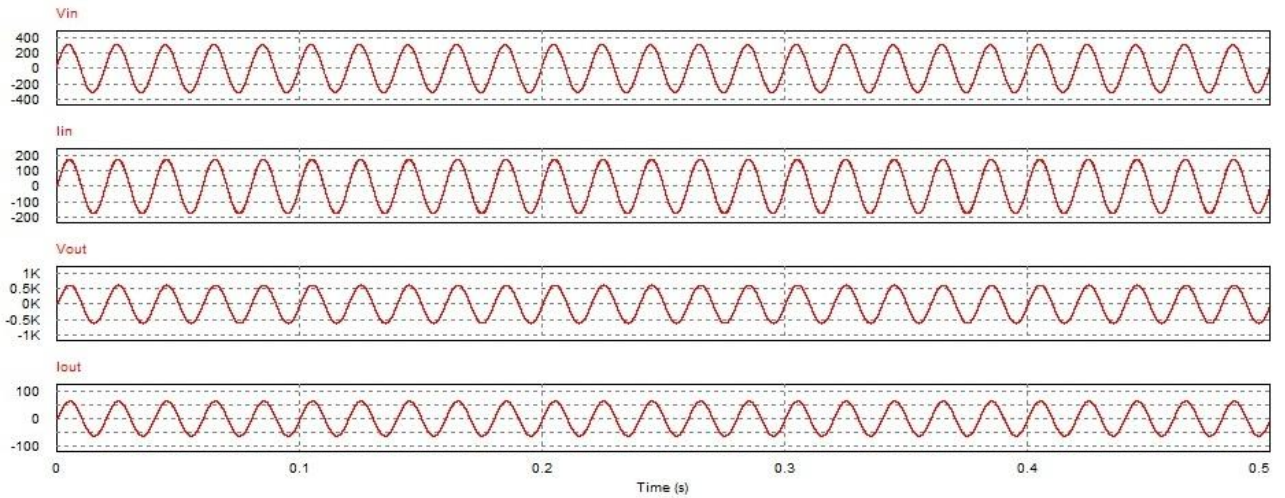
**Fig.: 4.6.3.g THD Vs Duty Cycle at 30 kHz**

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & I/P Volatge) | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|--------------------------------|----------------|
| 0.1              | 0.9              | 36                | 38.32               | 24.48                | 244.85               | 0.41                  | 0.99                           | 71.13          |
| 0.2              | 0.8              | 72                | 48.6                | 27.58                | 275.82               | 0.65                  | 0.99                           | 71.2           |
| 0.3              | 0.7              | 108               | 63.57               | 31.55                | 315.48               | 0.75                  | 0.98                           | 71.26          |
| 0.4              | 0.6              | 144               | 86.54               | 36.78                | 367.86               | 0.73                  | 0.96                           | 71.31          |
| 0.5              | 0.5              | 180               | 124.18              | 43.95                | 439.53               | 0.63                  | 0.99                           | 71.36          |
| 0.6              | 0.4              | 216               | 190.97              | 54.02                | 540.32               | 0.48                  | 0.97                           | 71.39          |
| 0.7              | 0.3              | 252               | 318.16              | 67.46                | 674.62               | 0.32                  | 0.91                           | 71.36          |
| 0.8              | 0.2              | 288               | 535.59              | 75.64                | 756.43               | 0.16                  | 0.68                           | 71.02          |
| 0.9              | 0.1              | 324               | 698.66              | 49.3                 | 493                  | 0.02                  | 0.23                           | 68.83          |

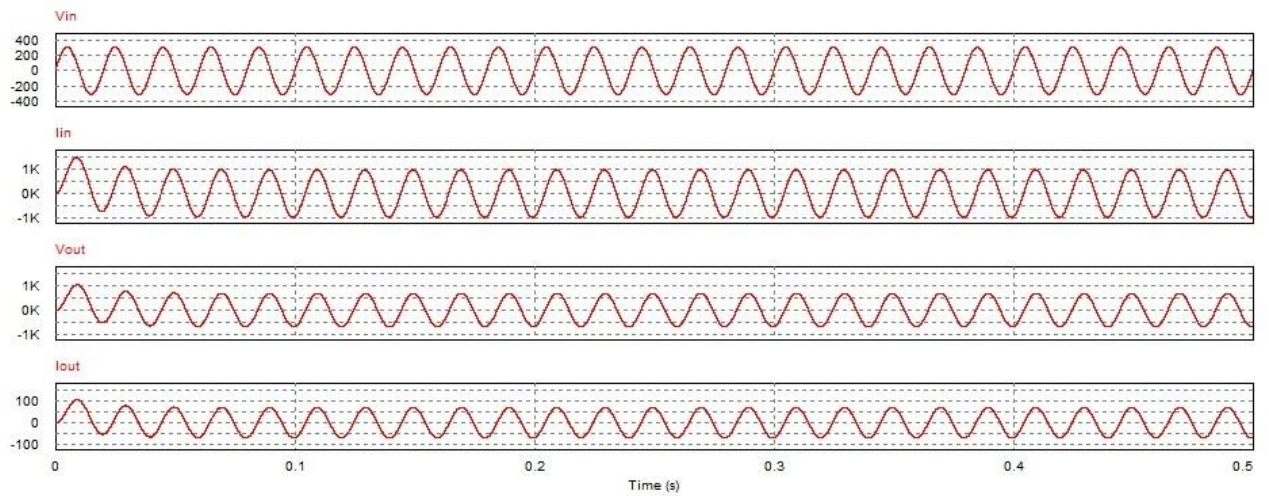
**Fig.: 4.6.4 Boost Topology with Filter Performance at 40kHz**



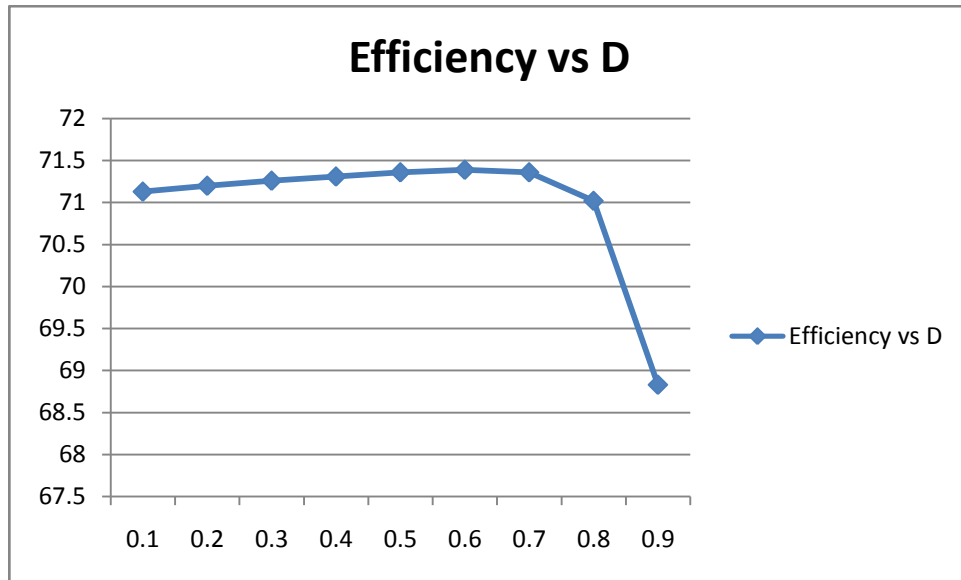
**Fig. 4.6.4.a Output and input of wave shape for duty cycle 0.1 with 40KHz frequency**



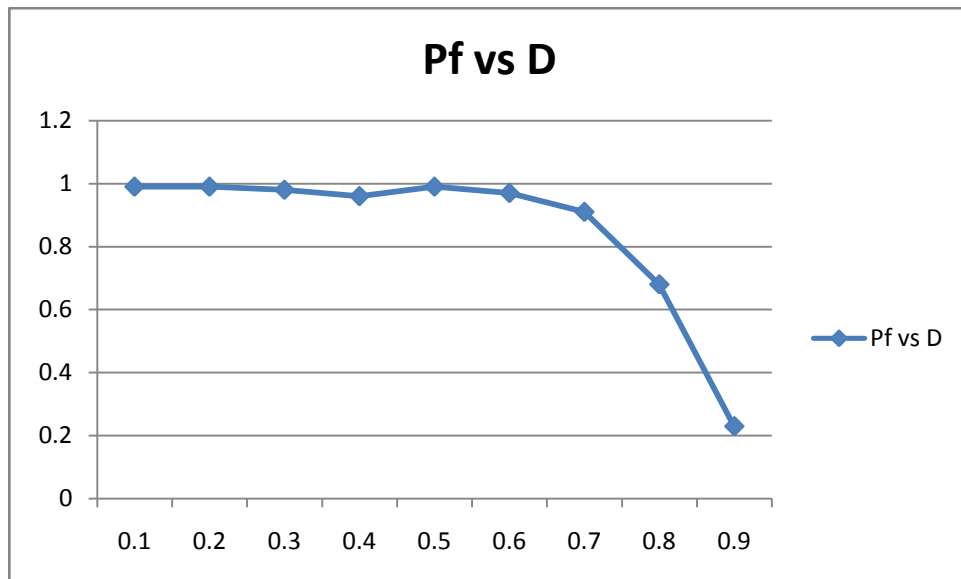
**Fig. 4.6.4.b Output and input of wave shape for duty cycle 0.5 with 40KHz frequency**



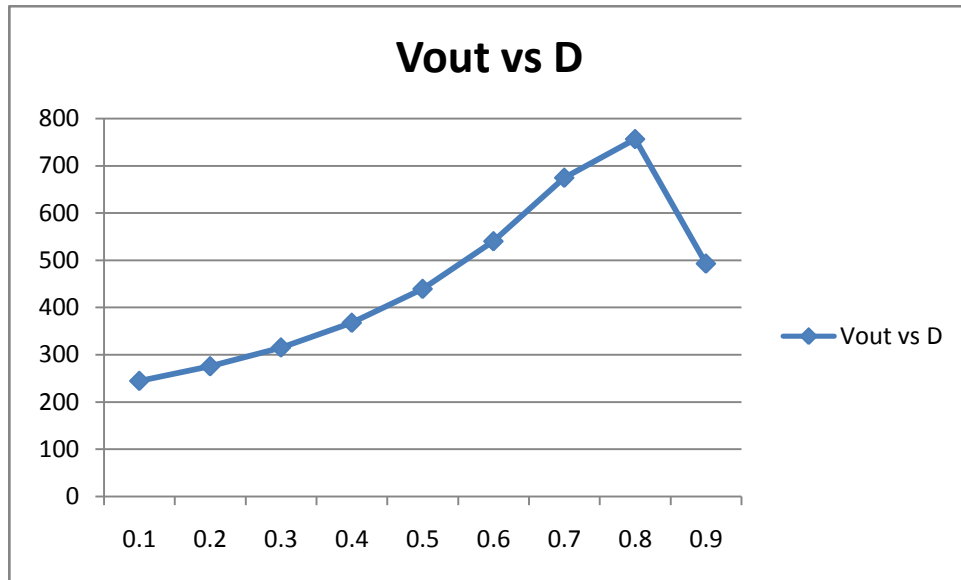
**Fig. 4.6.4.c Output and input of wave shape for duty cycle 0.9 with 40KHz frequency**



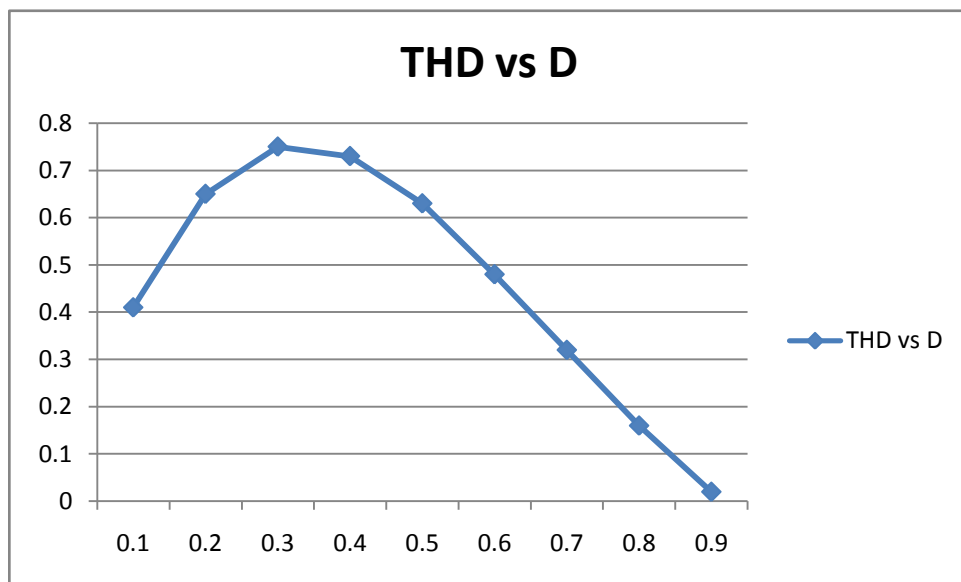
**Fig.: 4.6.4.d Efficiency Vs Duty Cycle at 40 kHz**



**Fig.: 4.6.4.e Power Factor Vs Duty Cycle at 40 kHz**



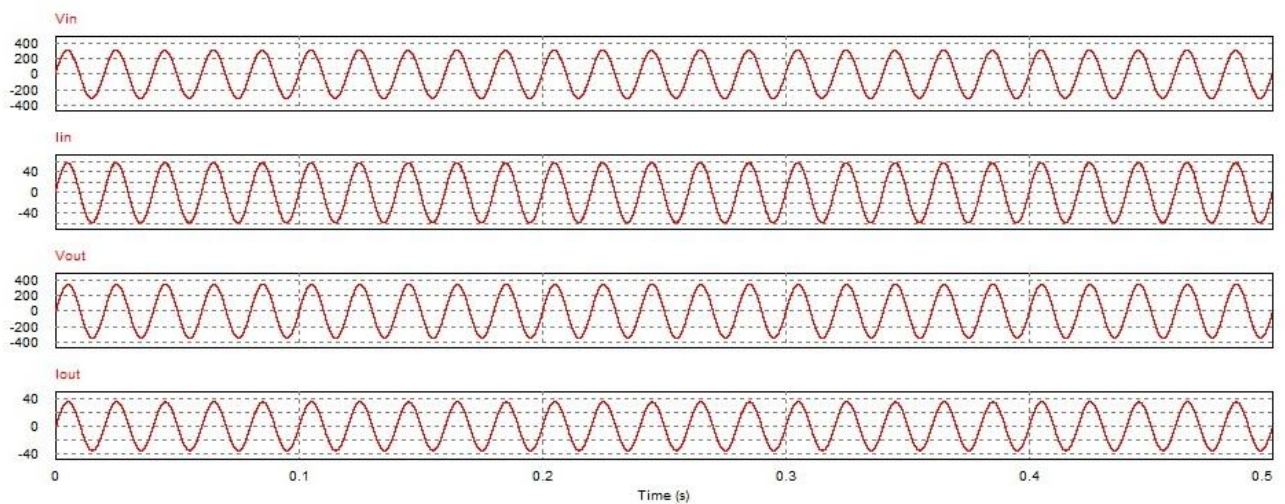
**Fig.: 4.6.4.f Output Voltage Vs Duty Cycle at 40 kHz**



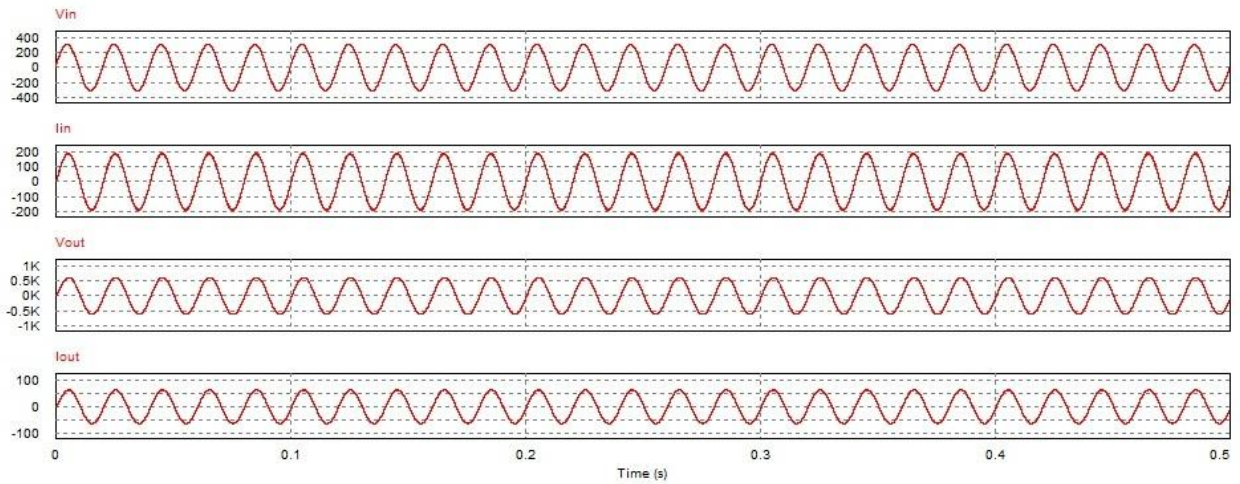
**Fig.: 4.6.4.g THD Vs Duty Cycle at 40 kHz**

| Duty Cycle (SW1) | Duty Cycle (SW2) | Phase Delay (SW2) | Input Current (rms) | Output Current (rms) | Output Voltage (rms) | THD (Input Current) % | P.F I/P Current & I/P Volatge) | Efficiency (%) |
|------------------|------------------|-------------------|---------------------|----------------------|----------------------|-----------------------|--------------------------------|----------------|
| 0.1              | 0.9              | 36                | 41.07701            | 24.48                | 244.8                | 0.31                  | 0.99                           | 66.35          |
| 0.2              | 0.8              | 72                | 52.07               | 27.57                | 275.73               | 0.49                  | 0.99                           | 66.42          |
| 0.3              | 0.7              | 108               | 68.09               | 31.53                | 315.3                | 0.56                  | 0.99                           | 66.49          |
| 0.4              | 0.6              | 144               | 92.64               | 36.74                | 367.48               | 0.54                  | 0.99                           | 66.55          |
| 0.5              | 0.5              | 180               | 132.74              | 43.85                | 438.56               | 0.47                  | 0.98                           | 66.61          |
| 0.6              | 0.4              | 216               | 203.47              | 53.74                | 537.47               | 0.36                  | 0.96                           | 66.65          |
| 0.7              | 0.3              | 252               | 335.78              | 66.47                | 664.78               | 0.24                  | 0.89                           | 66.64          |
| 0.8              | 0.2              | 288               | 550.75              | 72.64                | 726.41               | 0.12                  | 0.65                           | 66.32          |
| 0.9              | 0.1              | 324               | 700.82              | 46.19                | 461.92               | 0.000371              | 0.21                           | 64.26          |

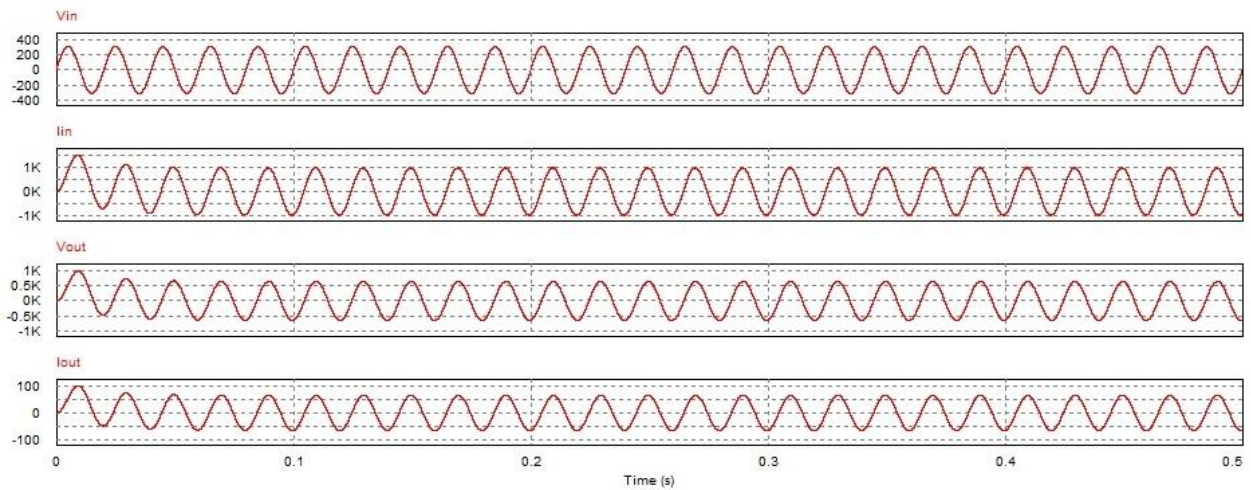
**Fig.: 4.6.5 Boost Topology with Filter Performance at 50kHz**



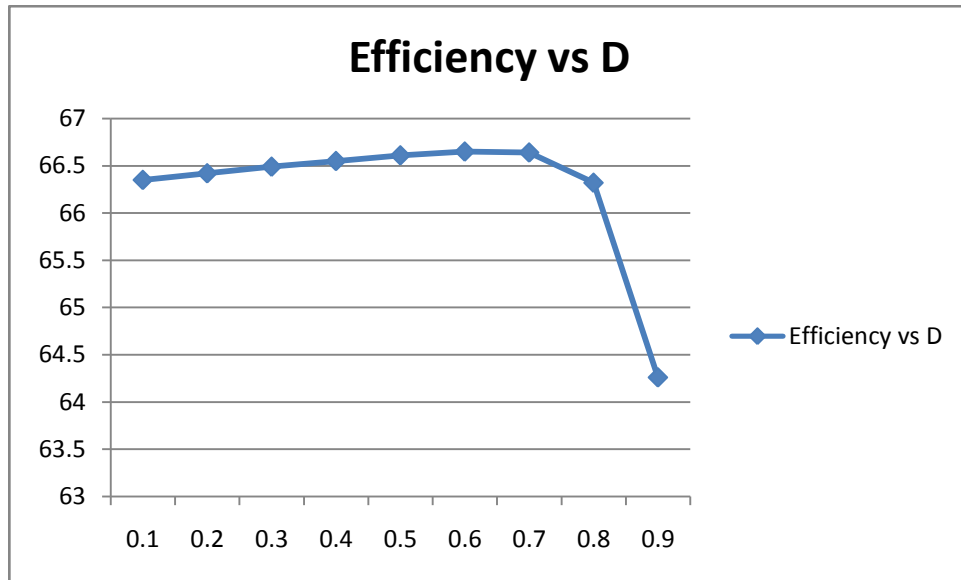
**Fig. 4.6.5.a Output and input of wave shape for duty cycle 0.1 with 50KHz frequency**



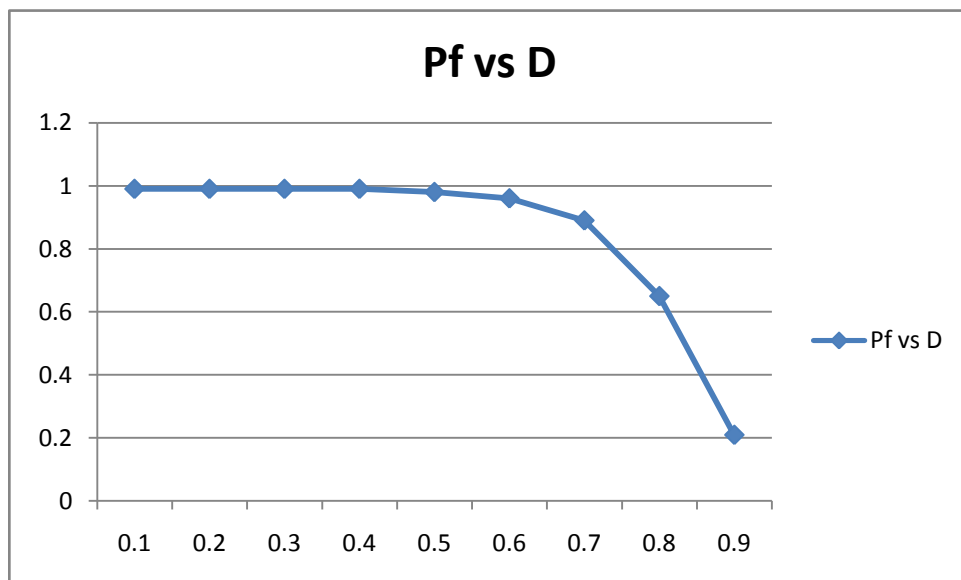
**Fig. 4.6.5.b Output and input of wave shape for duty cycle 0.5 with 50KHz frequency**



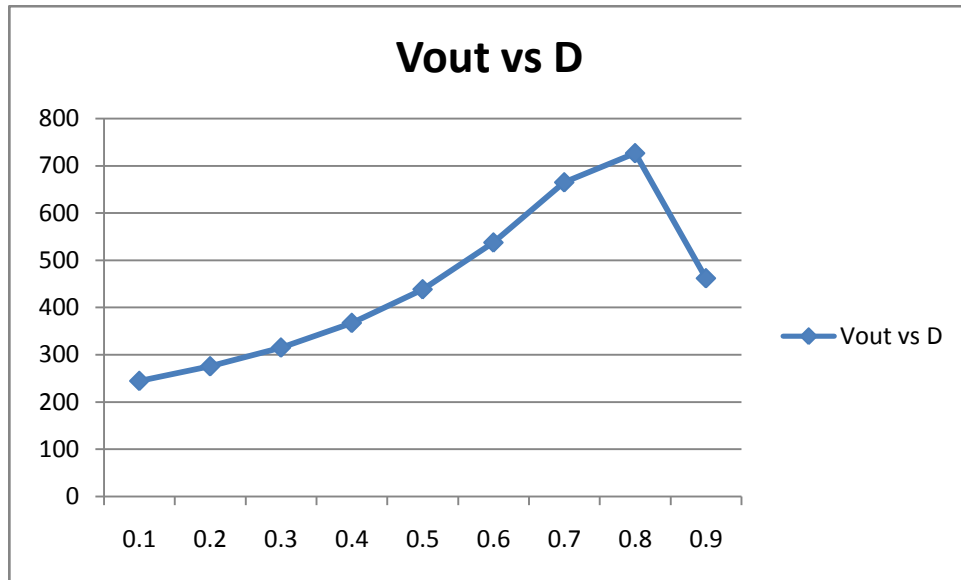
**Fig. 4.6.5.c Output and input of wave shape for duty cycle 0.9 with 50KHz frequency**



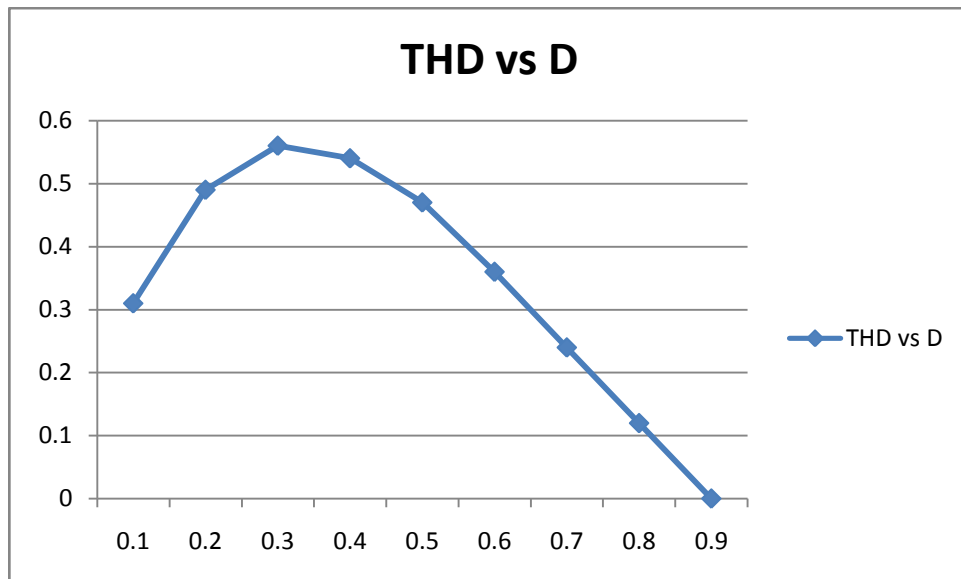
**Fig.: 4.6.5.d Efficiency Vs Duty Cycle at 50 kHz**



**Fig.: 4.6.5.e Power Factor Vs Duty Cycle at 50 kHz**



**Fig.: 4.6.5.f Output Voltage Vs Duty Cycle at 50 kHz**



**Fig.: 4.6.5.g THD Vs Duty Cycle at 50 kHz**

# **CHAPTER 5**

# **CONCLUSION**

## 5.0 CONCLUSION

In this study, single-phase AC-AC converter with filtering technique has been investigated.

We have calculated the parameters of the inductors and capacitors by using formulae and we have also invented the bi-directional switching method. Filtering techniques have been modeled and simulated by using POWER SIMULATOR. In these topologies we have used two bi-directional MOSFET switches to reduce power losses. In addition, we have designed BUCK and BOOST topologies. Without filtering, it is observed that the topologies have high harmonic content. However with filtering we have succeeded to eliminate the desired harmonic component.

### **Future Scope:**

Through this project work we have made an attempt to analyze efficiencies of BUCK and BOOST topologies by simulations. In future the hardware implementation of these two topologies can be done and its results obtained in real – time situations can be compared with the simulation results obtained in our thesis. By using these two topologies in future, the efficient BUCK-BOOST topologies can be designed. In future by using these two topologies efficient electronic appliances can be built.

# References:

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- <sup>3</sup> [http://en.wikipedia.org/wiki/Power\\_electronics](http://en.wikipedia.org/wiki/Power_electronics) reference
- <sup>4</sup> Power Electronics- Circuits, Devices and Applications *by* Muhammad Harunur Rashid
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