



Inspiring Excellence

Performance Evaluation of Advanced Solar Cells

Thesis submitted in partial fulfilment of the requirements for
the degree of Bachelor of Science in Electrical & Electronic
Engineering

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DECLARATION

We hereby declare that research work titled “*Performance Evaluation of Advanced Solar Cells*” is our own work. The work has not been presented elsewhere for assessment. Where material has been used from other sources it has been properly acknowledged/referred.

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Abstract

Generation of electricity from solar energy has been a sought-after field of research for the last few decades as the radiation of photons from the sun is an unlimited, clean source of energy. However, maximizing the effective conversion of electric energy from solar energy in a cost-effective way is still a challenge researchers are trying to overcome. The average efficiency of solar cells still needs to be improved by a large margin in order to compete with the fossil-fuel based energy-sources. The costs associated with the production and installment of solar panels need to be lowered as well. Silicon is the most used material for manufacturing solar cells for appurtenant reasons. In order to improve the efficiency while lowering the cost, the structure of silicon solar cells have been evolving since it was developed first in 1954. In this thesis, the performance of advanced solar cells is examined by simulation. In the simulation, two structural parameters of a solar cell, the cell thickness and the length of shading of finger are varied separately and the outcomes are observed. For the simulation, Quokka simulation software with MATLAB compiler were used.

Keywords: Silicon Solar cell, Advanced PV cell, Cell thickness, Finger shading, FRC and IBC cells, photovoltaic energy conversion efficiency.

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1. Preamble

Humans all over the world, at present, mostly depend on fossil-fuel based energy sources. As a result of unforeseen consumption of fossil-fuel based energy in extensive amount over the past century, global climate change and the Earth's atmosphere are significantly affected. To reverse the negative consequences of climate change, the reliance on fossil-fuel needs to be shifted to such a sustainable energy source which doesn't have adverse effects on the Earth. Moreover, the amount of fossil-fuel available on Earth's crust is very limited and highly insufficient with respect to the exponential growth in the demand of energy worldwide. On the other hand, sunlight is the largest energy flux incident on earth's surface which is over 1.6×10^{17} W of solar radiation (1). It is the most abundant source of renewable energy. With effective mechanism, if this power can be captured, it will surpass the total demand of energy all over the world by approximately 10^4 (2,3). Solar cells or photovoltaic cells are the devices that can absorb the energy from photons radiated from the sunlight and generate electricity by converting the energy.

The photovoltaic cells that are developed till now have a limited efficiency with a comparatively high manufacturing and installment expense. Solar cells are mainly implemented on pure silicon wafers. Silicon is highly abundant in nature in the form of Silica. The extraction of pure silicon from silica is done by reduction reaction. The reduction occurs in high temperature which involves a costly process. The reduction process also emit CO_2 to the atmosphere, however far less than the combustion of fossil-fuel does. Therefore, the reduction of cell thickness is an active area of research and development to reduce the silicon usage as well as the material cost (4).

The ongoing processes of enhancing solar cell efficiency while minimizing the cost are designed considering a number of external and structural factors. Optimization amongst these factors is needed to keep up the progress in solar cells' performances for better commercialization and mass use of solar panels.

1.1 Scope of the Thesis

In this thesis, the performances of advanced solar cells are evaluated by analyzing simulation results. Two structural parameters, cell thickness and length of shading of finger are varied separately and the simulations were run. The effects of these structural parameters on the significant electrical parameters on solar cell such as open circuit voltage, short circuit current density, fill factor and efficiency were observed. The specific objectives of this thesis are structured as follows:

1. In chapter 2, the basics of formation of PN junction, current-voltage relationship of PN junction and recombination mechanisms are reviewed.
2. The implementation of PN junction in the structure of solar cell and the operational mechanism and the current-voltage relationship of solar cell are addressed in chapter 3.
3. Chapter 4 covers the significant structural and electrical parameters of Silicon photovoltaic cells which are the variables the efficiency depends on.
4. The simulation data are documented and results are analyzed. The output data from simulation is plotted into graphs and the changes of the variables corresponding to the changes in cell thickness and length of shading of finger are explained.
5. Last of all, a conclusion wraps up the thesis with some insights attained from analyzation of the results.

2. Literature Review on Silicon PN Junction

Silicon is the second most adequate component in the world, discovered for the most part as Silicon dioxide (SiO₂). For its availability, variety in physical forms and electronic properties as a semiconductor, it is the most suitable material to be used to manufacture cost effective solar cells. A solar cell is essentially a PN junction. This chapter discusses the structure and properties of PN junction as well as the mechanism of charge carrier generation and conduction through the PN junction.

2.1 Semiconductor Materials

Semiconductors are utilized as a part of hardware circuits broadly. As the name recommends, semiconductor can conduct current, but partially. The electricity of a semiconductor is in the midst of an insulator and a conductor. Insulator contains almost no conductivity while, a conductor contains almost full conductivity. Semiconductor's resistance, unlike metals', decreases when heat is given or the temperature is increased (5). The conducting properties of a semiconductor relies upon the pollutant or impurities or dopant added to it.

The semiconductor components are from the periodic table of group-IV, or either group-III combined with group-V or group-II combined with group-VI. The extensively used semiconductor is Silicon. Silicon belongs to group-IV of the periodic table. Silicon is the basic structure of the integrated circuits (ICs).

Silicon has a unique property which is, it has four electrons in its exterior shell or valence shell. Silicon has an atomic number of 14 and the electron configuration of Si is $2+8+4=14$. The outermost shell is named as valence shell. Because of this property Si can form crystals. A crystal is a periodic arrangement of particles- atoms, molecules or ions. The four electrons of the valence shell form covalent bonds with four neighboring atoms and thus form a lattice.

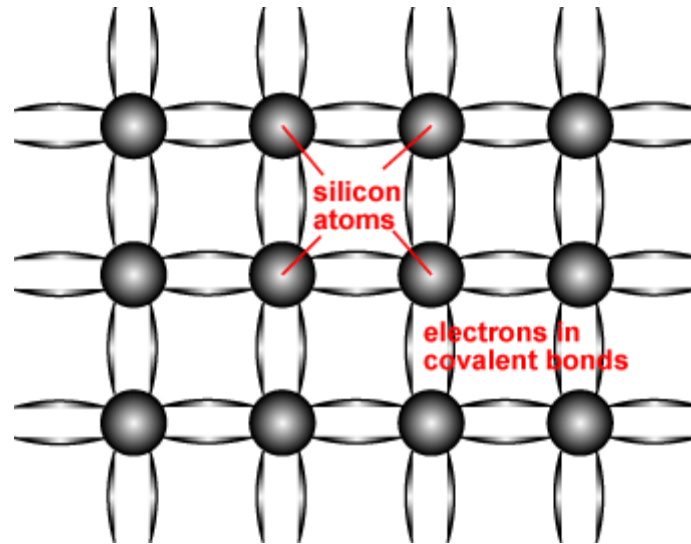


Figure 1: Structure of Silicon lattice

Silicon lattice form a bond with neighboring four atoms and hence, there remain no space to flow or conduct any electric current. However, through a procedure termed doping the properties could be changed. Doping is the process of introducing impurities or foreign atoms to a crystal deliberately. The injected components are called a dopant. Silicon crystals can be changed into two particular sorts of conductors by utilizing the doping procedure and dopant.

1. N-type semiconductor
2. P-type semiconductor

2.1.1 N-type semiconductor

N-type dopants are the components of group-V of the periodic table, which means the valence shell are contain of five electrons. In N-type doping, Phosphorus or Arsenic is added as dopant in a small amount with silicon. Phosphorus and arsenic both have five valence electrons and the fifth electron does not have anything to bond with so, it becomes free electron (6). A very small portion of impurity can create a huge amount free electron which leads to flow electric current in Silicon. Majority carrier of N-type semiconductor is electron and minority carrier are holes.

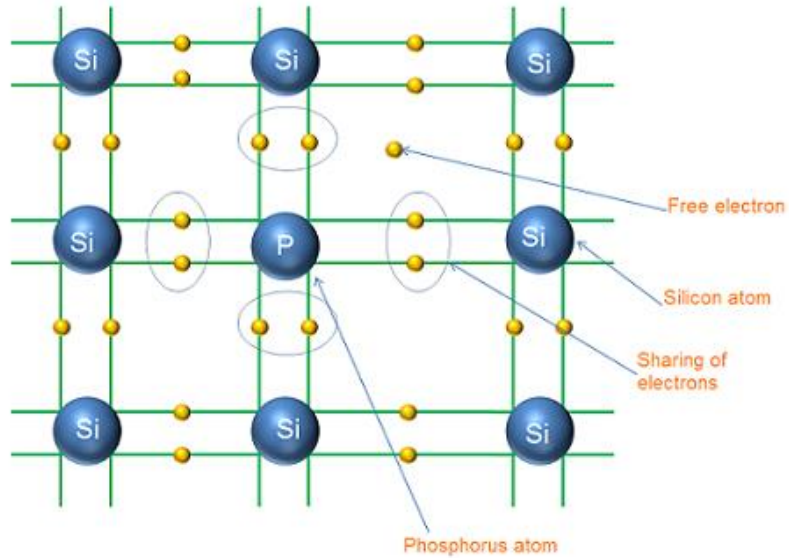


Figure 2: N-doped silicon

2.1.2 P-type semiconductor

P-type dopants are the components of group-III of the periodic table, which means the valence shell are contain of three electrons. Boron or Gallium is added as dopant in a small amount with silicon in P-type doping. Boron and Gallium both have three valence electrons and the third electron does not have anything to bond with so, when it added with Silicon it forms a hole as in the lattice an electron of silicon has nothing to do (6). Current could be conducted by holes. Majority carrier of P-type semiconductor is holes and minority carrier are electrons.

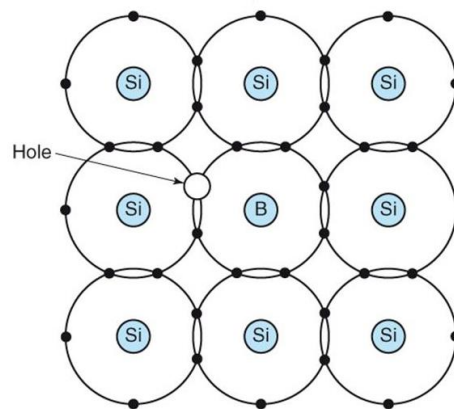


Figure 3: P-Doped Silicon

2.2 PN-Junction

A PN-junction is the combination of a N-type substantial and a P-type substantial (8). P-type substantial incorporate plenty of holes while N-type substantial incorporate plenty of electrons. While these two types are fused together with each other it allows current to pass through the junction in one direction and thus create a basic diode. This junction has been named as PN-junction.

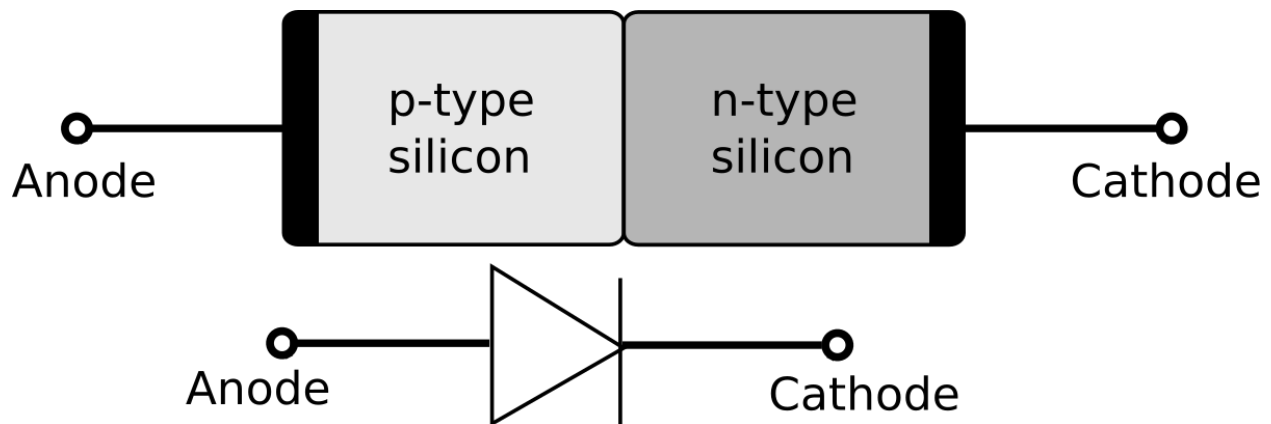


Figure 4: PN junction

2.3 Depletion region

PN-junction incorporate both P-type and N-type substance. N-type contains plenty of electrons. These huge amount of electrons are free electron. Thus, these huge amount of electrons try to move from high concentration region (n-type) to low concentration region (p-type). In the edge of the junction both the holes and electrons are very close to each other. According to Coulombs law, there exist a force of attraction between opposite charges (9).

Hence, free electron from n-side move towards p-side as attracted by the holes. Thus, from n-side to p-side electron move. Similarly, from p-side to n-side holes shift.

The free electrons shift to p-side; which increases the number of electron in p-side that creates negative ion in p-side. Similarly, holes shifted to n-side and increased the number of proton in n-side and creates positive ion in n-side.

In this way in p-side a negative charge has been created and in n-side a positive charge has been created. This net negative charge does not allow to flow any electron from n-side so as, any positive charge from p-side.

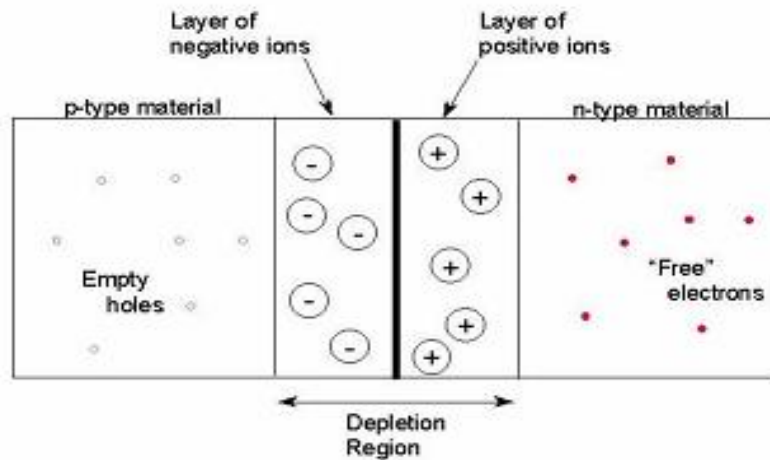


Figure 5: Depletion region in PN junction

Thus, the static positive charge at n-side and static negative charge at p-side on the edge of the crossing behaves as a barrier or wall which stops the further flow of electron and holes. The portion on the edge of the crossing where movement of charges carriers is lessened over a particular time and leads in vacant charge carriers or full of static charge carriers has been named as depletion region (9).

The depletion region is preferably known as depletion zone, depletion layer, space charge region, or space charge layer too.

2.4 Barrier Voltage

The n-type and the p-type substances are electrically neutral before free electrons and holes has crossed the crossing. When the free electrons and holes have crossed the PN-junction, the p-type semiconductor and the n-type semiconductor become charged. While the atoms have unequal number of electron and hole or proton, then the atom is said to be charged (10). This charged atom could be negative or positive. When the atom has more electron than holes or proton the atom is

said to be negatively charged. On the contrary, the atom which has more number of proton or holes than electron is said to be positively charged. As, in the PN-junction free electron shift from n-side to p-side and make p-side negatively charged. Similarly, free electron moving towards p-side leaving holes in the n-side and thus making n-side positively charged. As, n-side has majority on protons or holes.

This negative charge at p-side prohibits the flow of electron. Similarly, the net positive charge at n-side prohibits the flow of holes or proton. Hence, positive charge in n-side and negative charge in the p-side of the PN-crossing performs as barrier between p-type and n-type semiconductor.

This is how, a barrier is built between the n-type and p-type semiconductor which prohibits any additional flow of free electron and holes. The negative charge created at p-side of the crossing is called negative barrier voltage and the positive charge created at n-side of the crossing is called positive barrier voltage and the total charge constructed at the p-n junction is named as barrier voltage, barrier potential or junction barrier.

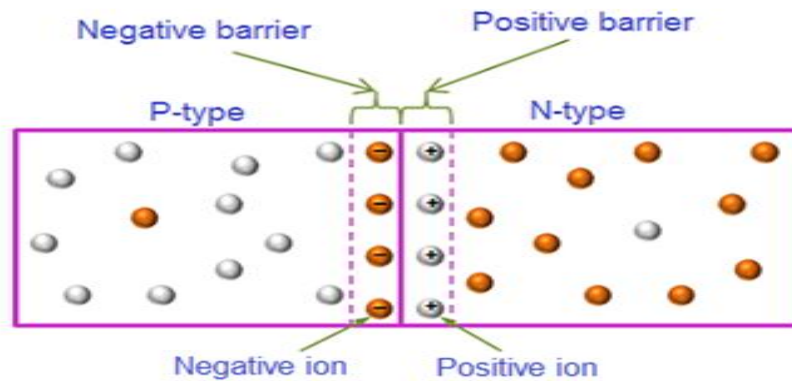


Figure 6: Barrier potential in PN junction

There are some elements on which the barrier voltage is dependent such as; the chunk of doping, crossing temperature and type of substance used. The barrier voltage for silicon is 0.7 volts and for germanium is 0.3 volts (10).

The barrier voltage restrains the movement of majority carrier and allow the minority carrier to flow. That means, barrier voltage at PN-junction will oppose the flow of free electron from n-side to p-side. But any free electron (minority carrier) produces at p-side due to thermal energy will be attracted towards the positive barrier at the n-side of the PN-junction and will crosses from p-side to n-side of the semiconductor.

Similarly, any holes (minority carrier) produced at n-side due to thermal energy will be attracted towards the negative barrier at the p-terminal of the PN-crossing and will cross from n-side to p-side of semiconductor.

Hence, it means that barrier voltage allows the conductivity of minority carriers at PN-junction of semiconductor.

2.5 Drift Current

Due to the movement of the charge bearer a current is produced while an electric field has been activated over the semiconductor, which is called drift current. When voltage is applied in the semiconductor the free electron flow to the positive side of the external voltage source and the protons or holes ploy to the negative side of the external voltage source. This happens, as same charges drive away each other while opposite charges attract each other.

Electrons always try to ploy in a line but, as they keep on colliding with each other the atoms change their direction frequently. This irregular gesture is not controllable through the voltage which has been applied but, it leads those electrons to drift to the positive terminal.

Drift velocity is the velocity which could be get through the applied voltage or electric field (10).

The drift velocity of electrons is followed by,

$$V_n = \mu_n E \dots\dots\dots 1$$

The drift velocity of holes is followed by,

$$V_p = \mu_p E \dots\dots\dots 2$$

Here,

V_n = drift velocity of electrons

V_p = drift velocity of holes

μ_n = mobility of electrons

μ_p = mobility of holes

E = applied electric field

Due to free electrons, the drift current density is (11),

$$J_n = en\mu_n E \dots\dots\dots 3$$

Due to holes, the drift current density is (11),

$$J_p = e p \mu_p E \dots \dots \dots 4$$

Here,

J_n = drift current density due to electron

J_p = drift current density due to hole

e = charge of an electron = 1.602×10^{-19} Coulombs (C)

n = number of electrons

p = number of holes

The total drift current density is,

$$J = J_n + J_p = e n \mu_n E + e p \mu_p E$$

$$J = e (n \mu_n + p \mu_p) E \dots \dots \dots 5$$

2.6 Diffusion Current

Charge carriers tend to move from high concentration zone to low concentration zone in a semiconductor. As a result, a flow of current produces which is preferably known as diffusion current.

Higher concentration zone contains high amount of electron while, lower concentration zone contains lesser number of electron. This movement of the bearers produced current designated as diffusion current. In any uneven semiconductor diffusion could be found (9).

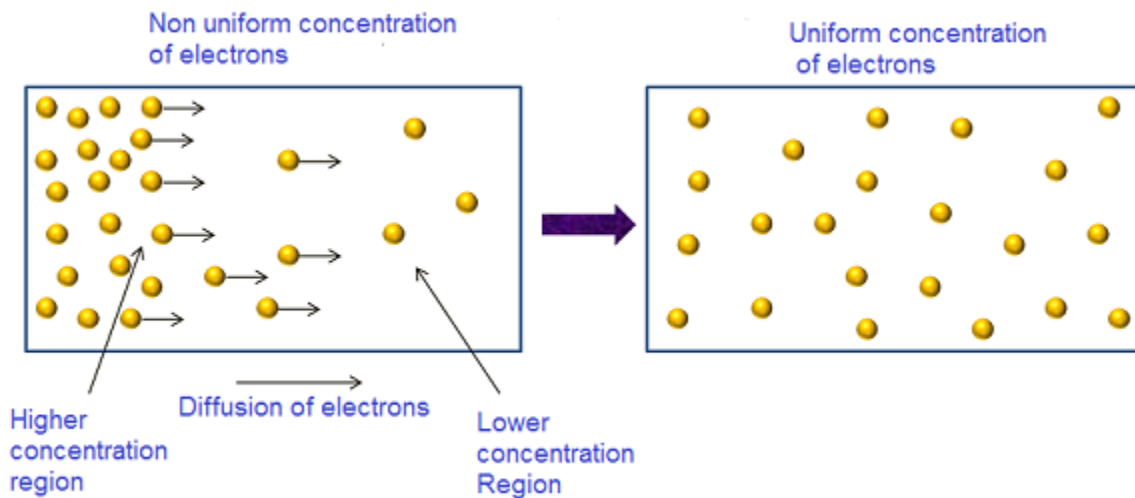


Figure 7: Diffusion of charge carriers

To become even from uneven semiconductor, electrons will start moving to the right side. This movement will lead to a current flow which is named as diffusion current.

In a semiconductor device, both drift and diffusion current is produced. Diffusion current occurs without an external voltage or electric field applied, but not in a conductor. The direction of diffusion current is same or opposite to that of the drift current.

2.6.1 Concentration gradient

The diffusion current density is directly proportional to the concentration gradient. Concentration gradient is the difference in concentration of electrons or holes in a given area. Diffusion current density will be high if, concentration gradient is also high. Similarly, diffusion current density will be low because of low concentration gradient.

The concentration gradient for n-type semiconductor is (11),

$$J_n \propto \frac{dn}{dx}$$

The concentration gradient for p-type semiconductor is (11),

$$J_p \propto \frac{dp}{dx}$$

Here,

J_n = diffusion current density due to electrons

J_p = diffusion current density due to holes

2.6.2 Diffusion current density

The diffusion current density because of electrons is (11),

$$J_n = +e D_n \frac{dn}{dx} \dots\dots\dots 6$$

Here,

D_n is the diffusion co-efficient of electrons.

The diffusion current density because of holes is (11),

$$J_p = -e D_p \frac{dp}{dx} \dots\dots\dots 7$$

Here,

D_p is the diffusion co-efficient of holes.

The total current density because of electrons is the summation of drift and diffusion currents (11).

$J_n = \text{Drift current} + \text{Diffusion current}$

$$J_n = en\mu_n E + e D_n \frac{dn}{dx} \dots\dots\dots 8$$

The summation of drift and diffusion currents is the total current density due to holes is (11).

$J_p = \text{Drift current} + \text{Diffusion current}$

$$J_p = ep\mu_p E + e D_p \frac{dp}{dx} \dots\dots\dots 9$$

The total current density due to electrons and holes is (11),

$$J = J_n + J_p \dots\dots\dots 10$$

2.7 Diode current equation

Diode current equation shows the connection of the current flowing across the diode as a function of applied voltage across it. The ideal diode current equation is (12),

$$I = I_0(e^{\frac{qV}{kT}} - 1) \dots\dots\dots 11$$

Here,

I = the net current flowing through the diode

I_0 = "dark saturation current", the diode leakage current density in the absence of light

V = applied voltage across the terminals of the diode

q = absolute value of electron charge

k = Boltzmann's constant = $1.38 \times 10^{-23} \text{ JK}^{-1}$

T = absolute temperature (K)

2.8 I-V characteristics of PN Junction

The I-V graph of PN junction indicates how current shifts exponentially with the adjustments in a voltage applied.

2.8.1 I-V characteristics in forward bias

In forward biased p-n junction diode, positive side of the battery is joined to p-type semiconductor substance while the negative side of the battery is joined to the n-type semiconductor substance (14). The amount of voltage applied across the crossing determines the amount of electron and holes to be produced. This extensive number of free electrons and holes cut down the width of depletion region. Hence, the current of PN-junction diode rise exponentially.

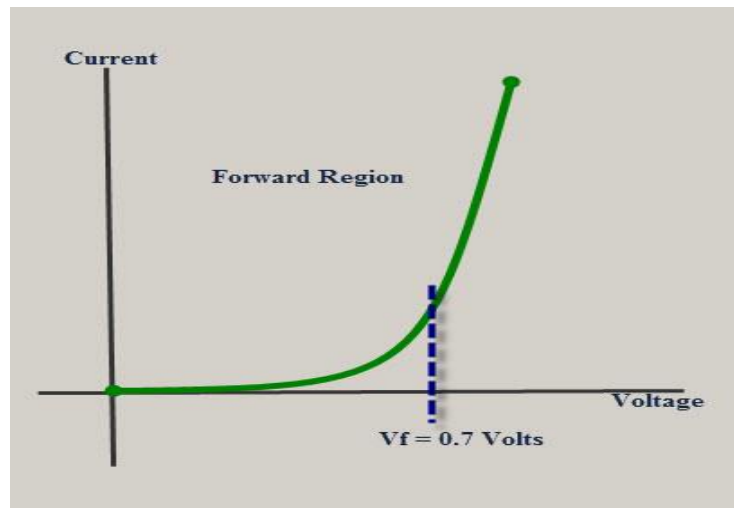


Figure 8: I-V plot in forward biased silicon PN junction

In forward bias condition, if the biasing voltage of silicon is 0.7 volts or 0.3 volts for germanium then the diode could be activated and thus, started flowing current.

2.8.2 I-V characteristics in Reverse bias

In reverse biased p-n junction diode, negative side of the battery is joined to p-type semiconductor substance while the positive side of the battery is joined to the n-type semiconductor substance. Increased reverse biased voltage leads to the isolation of electron and holes from the crossing (14). Eventually creates an expansion of the width of PN-junction. So, when the voltage is increased the width of depletion region get expanded.

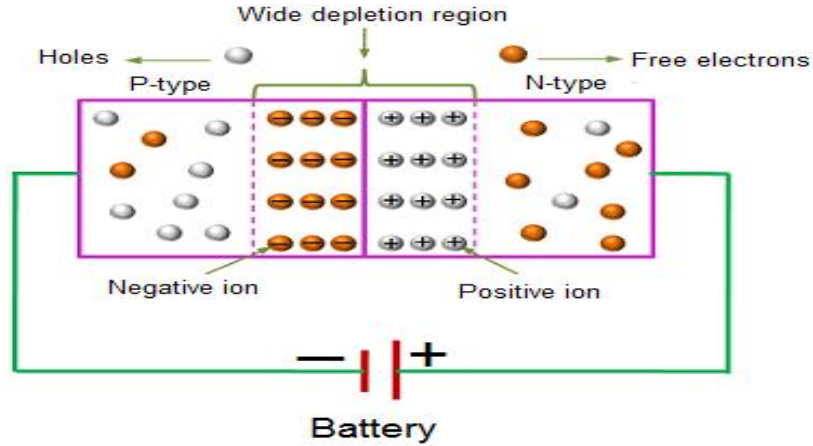


Figure 9: PN junction in reverse bias

The expanded depletion region of reverse biased p-n junction diode totally prevents majority charge bearer current and allows minority charge bearer current. On a particular point of increasing reverse biasing voltage, the positive side of the battery drives the protons headed to the p-type semiconductor. Similarly, negative side of the battery drives the free electrons headed to the n-type semiconductor. The positive charge bearers are captivated by the negative side of the battery and negative charge bearers are captivated by positive side of the battery. And leads the electric current to conduct in reverse bias. The particular reverse biased voltage, at which current start flowing, is called the breakdown voltage. The minority charge bearer has a current which flows through the diode is named as reverse current (14).

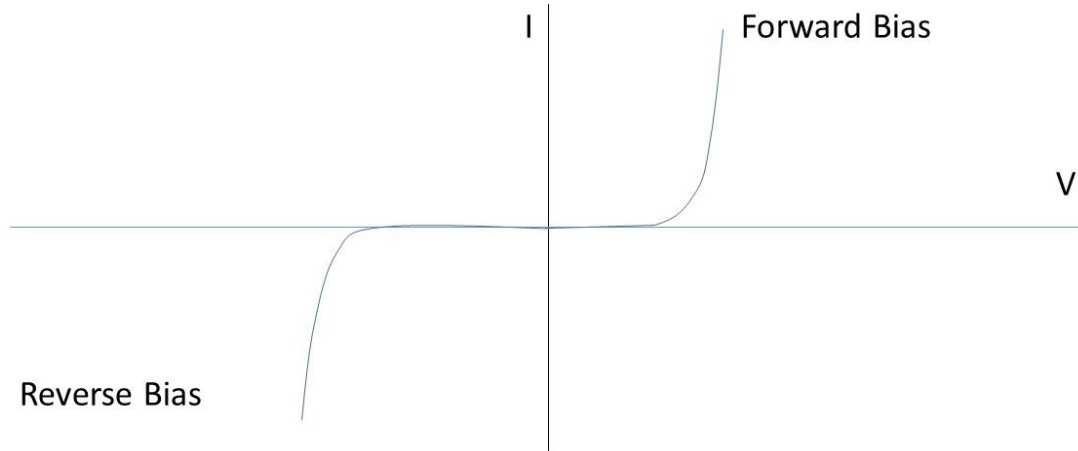


Figure 10: I-V plot of PN junction in both forward and reverse bias

There still remains a very tiny number of minority charge bearer in n-type and p-type semiconductors. So, to drive away those minority bearers a small amount of voltage is applied on the diode across the crossing. So that, any further increment of the outer voltage cannot affect the flowing current. This flowing electric current has been called reverse saturation current. Reverse saturation current could be found at the maximum point of current flow where any increment of the voltage would not affect the flowing current (14). Reverse saturation current relies on temperature.

2.9 Recombination Mechanisms

2.9.1 Recombination

Electrons existing in the conduction band are in a meta-stable state. These electrons, after some time, stabilize themselves by returning to the valence band. It does so by moving into an unoccupied state in the valence band, hence, simultaneously removing a hole. This phenomenon is known as recombination (15).

There are three ways by which recombination takes place. These are discussed next.

2.9.2 Shockley-Read-Hall recombination

It happens due to manufacturing defects in the semiconductor material. First, a charge carrier is captivated by an energy state of the forbidden band gap, which is caused by a glitch in the silicon lattice. If a charge carrier of opposite charge goes up to the exact energy state earlier than the trapped charge carrier can be re-emitted into the conduction band thermally, it recombines.

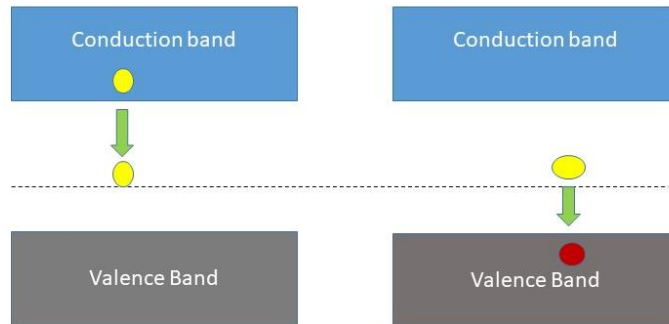


Figure 11: SRH recombination

2.9.3 Auger recombination

Auger recombination takes place involving 3 charge carriers. An electron and a hole recombine with each other and instead of emitting the energy in any other form, the recombining charge carrier gives the energy to a third carrier, which is another electron staying in the conduction band. This electron moves down to the conduction band edge thermally. Auger recombination is very significant when the carrier concentrations made by heavy doping or high level injection are high under concentrated sunlight (15). Recombination of this type cuts the lifetime and conclusive efficiency of silicon solar cell short.

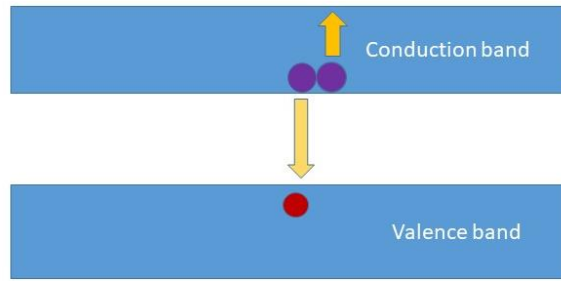


Figure 12: Auger Recombination

2.9.4 Radiative recombination

It happens in semiconductors with direct bandgap (for example, GaAs). Electron of the conduction band straightly recombines with a hole of valence band and expels energy in the form of photons. It is not applicable for silicon diodes (15).

2.10 Summary

This chapter describes the fundamental theoretical concepts regarding the structure and operational mechanism of PN junction. It also discusses important parameters contributing to the generation of electric current in PN junction like depletion zone, barrier voltage, drift current, diffusion current, I-V characteristics in forward & reverse bias and recombination mechanisms. All these concepts and theories are relevant for this thesis work.

3. Structure and Operation of Solar Cell

Silicon solar cell was first developed by engineer Daryl Chapin, chemist Calvin Fuller, and physicist Gerald Pearson at Bell Laboratories, USA in 1954 (16). Later, selling of commercial silicon PV technologies started in 1956 by Western Electric, USA (17). The structures of commercially available Si PV cells at present are comparatively simple than the structures of those used for specialized research purposes. Next, in this chapter, the structure of basic solar cells and structures of commercially available solar cells are briefly discussed. Later in this chapter, the mechanism of photovoltaic energy conversion in the photovoltaic cells and I-V characteristics of the PV cells in different conditions are discussed.

3.1 Basic structure of a standard solar cell

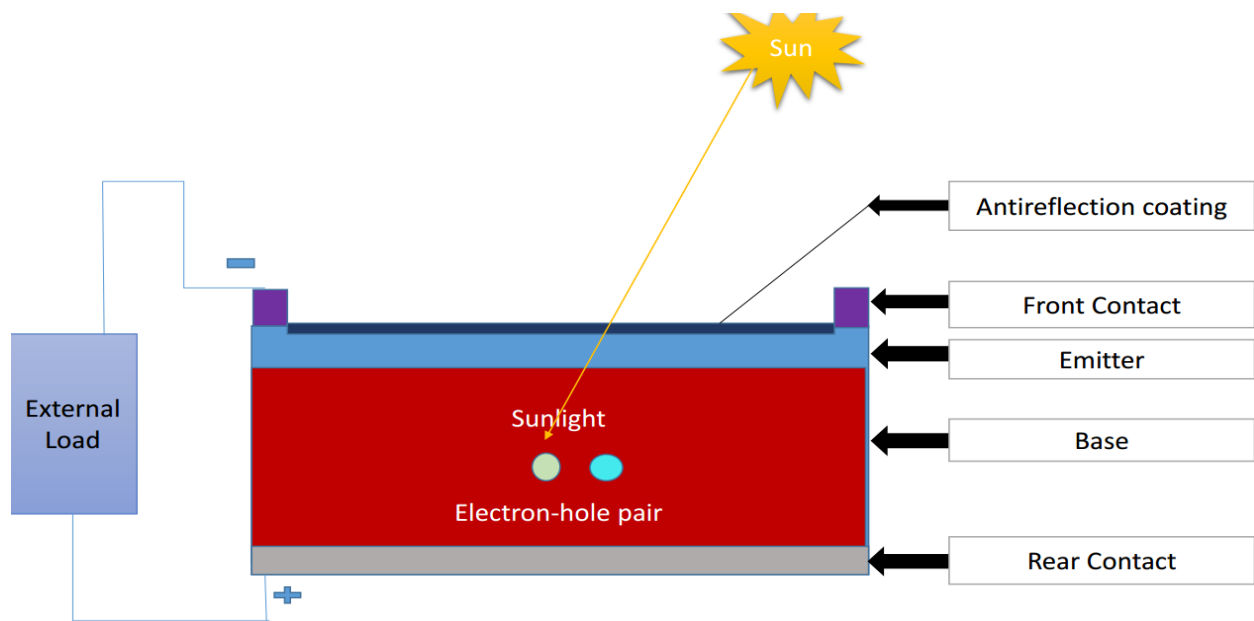


Figure 13: Structure of a Standard Silicon Solar cell

Figure13 shows the basic structure of a standard solar cell. In the PN junction of the solar cell, the base is comprised of P-type Silicon and the emitter is made of N-type Silicon. The width of the

base is much greater than that of the emitter to ensure that photons are absorbed by the P-type region as well as the N-type region. An anti-reflection coating (ARC) is applied on top of the cell to increase cell's efficiency by reducing the amount of reflected photons (18). The back contact is formed by a metal electrode, for example aluminum. On the other hand, the front contact is usually formed of silver paste applied with screen-printing on the top of the ARC layer (19), to increase the conductivity of the cell and to collect the charge carriers generated in the PN junction through the absorption of photons.

3.2 Industrially produced solar cells of different structures

The present commercial market of Si PV cell offers mainly two types of PV cells. These are:

- i. Front and rear contact cells
- ii. Interdigitated Back contact cells

3.2.1 Front and rear contact(FRC) cells

The structure of FRC cell is same as the structure of standard Si PV cells described in the section 3.2. The manufacturing process of FRC cells are the least complex amongst that of all the varieties of PV cells developed till date.



Figure 14: Structure of FRC cell [20]

3.2.2 Interdigitated Back contact (IBC) cells

As the name indicates, both positive and negative contacts are located at the rear surface of the IBC cells. Unlike FRC cells, the IBC cells do not have gridlines at the front as there is no front contact [21].

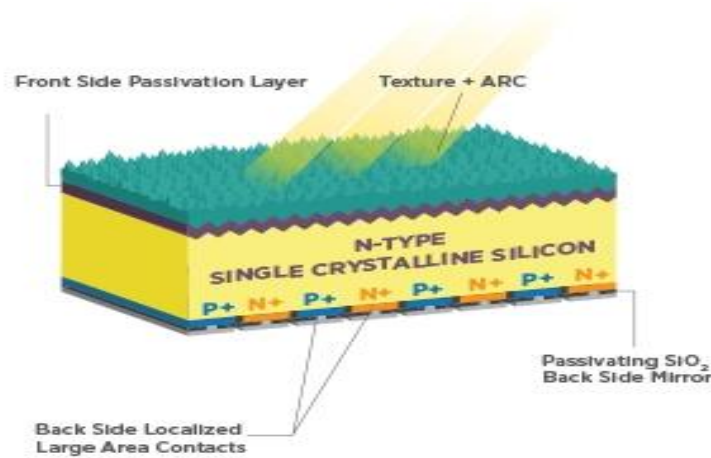


Figure 15: Structure of IBC cell [20]

3.2.3 Differences between FRC cells & IBC cells

FRC cells	IBC Cells
1. The base is made of P type silicon	1. The base is made of N type silicon.
2. Emitters (front conductive boundary) have N type doping and the rear conductive boundary have high P type doping.	2. Inter-digitated positive and negative contacts are situated on the rear surface.
3. Comparatively higher recombination loss.	3. Localized contacts & passivating silicon dioxide layer reduce the recombination loss.
4. Lower efficiency due to higher recombination, resistance and front finger shading loss.	4. Higher conversion efficiency.
5. Comparatively simple and very convenient fabrication process making the production cost cheaper.	5. Manufacturing process is highly complex resulting in increased manufacturing cost, making it hard to challenge the market price of conventional solar cells (FRC cell).

Table 1: Differences between FRC cells & IBC cells

Therefore, considering the existing economic benefit, this thesis is done focusing on FRC cells and improving the efficiency of FRC cells.

3.3 Fabrication of Single Crystal Solar cells

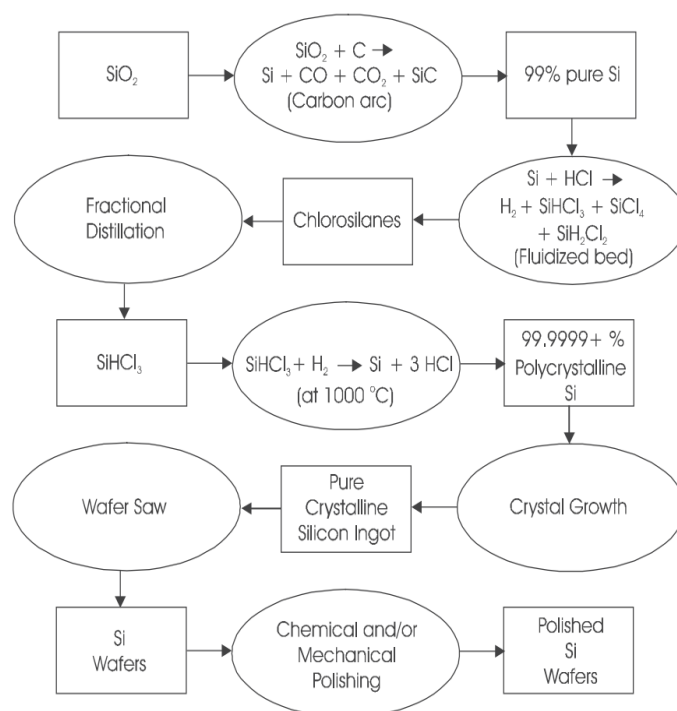


Figure 16: Production of single crystal silicon wafers from sand [22,39]

To start, SiO_2 is collected by mining it from Earth's crust. Oxygen is removed from Silicon by reduction reaction in presence of Carbon in an arc furnace. The product obtained is 99% pure metallurgical grade silicon. However, this 1% impurity is not acceptable and it is further purified to reduce the impurity to approximately 1 part in every 10^7 parts of silicon atoms (22). This purification is done by reacting the metallurgical grade silicon with HCl forming trichlorosilane (SiHCl_3). Fractional distillation is done afterwards on the trichlorosilane to attain the desired 99.99999% pure polycrystalline silicon (22). In order to get single crystal silicon, this polycrystalline electronic grade silicon is then melted and recrystallized.

When melted, the p-type and n-type crystals are made by introducing boron or arsenic in required amount to the melted silicon, to obtain the desired doping concentration (22). Upon solidification, special saws are used to cut the silicon feedstock into wafers.

Afterwards, the PN junctions are created in solar cells mostly by diffusion (22). Then, back and front contacts are established. Screen printing process is followed to form the fingers on the front with silver paste (23). Next, antireflection coating is applied to the cell.

3.4 Mechanism of Conversion of Photovoltaic Energy

The generation of current from sunlight is divided into two key processes:

- i. Electron-hole pairs are generated by absorbing energy from photons.
- ii. Generated charge-carriers are gathered to generate a flow of electricity.

The energy of photons from sunlight is greater than the energy band gap of silicon. So upon the absorption of energy from photons, electron-hole pairs are produced in the emitter. The electrons in the P-type region and the holes of n-type region last as long as the duration of minority carrier life time on average. After that, these carriers will recombine and there will be no more current generation from those.

The collection of these electrons and holes by the p-n junction prevents recombination. The electron in the emitter cannot move across to the base for the electric field in the depletion layer. The hole when goes near to the depletion layer, it is swept across by the electric field to the base (p region), for it being the majority carrier there. If the N region and the P region are connected together, the electron will move through the external circuit and will combine with the hole in P region and hence current will be generated. Thus conversion of photovoltaic energy is done in PV cells (24).

3.4.1 Collection Probability

The probability of a light-generated carrier in a particular region of the solar cell being accumulated by the P-N junction and hence resulting in current generation is known as the collection probability. This probability depends on the distance the carrier is needed to cover in comparison to the length of diffusion and the surface passivation of the device. The collection

probability of light-generated carriers is unity at the depletion zone and it reduces towards the edges. [25]

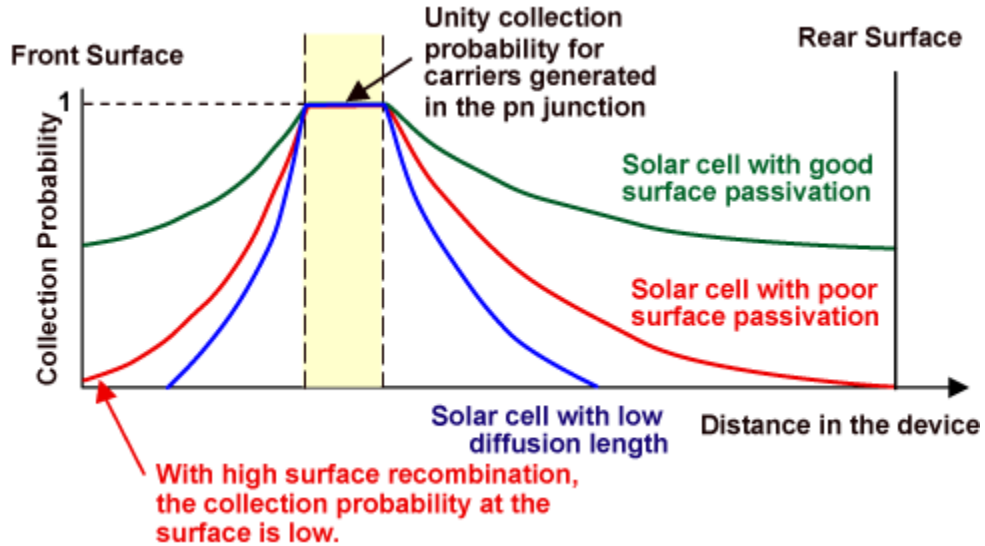


Figure 17: Impact of diffusion length and surface passivation on collection probability [25]

3.4.2 The photovoltaic effect

The photovoltaic effect process of generating voltage in a solar cell. Due to the collection of light-generated carriers in the p-n junction, movements of electrons in N region and holes in P region increases. If there is no external circuit connecting the emitter and the base, the carriers will not be able to leave the device and this will increase the numbers of electrons in the N region and that of holes in the P region. The increment of charge carriers will reduce the net electric field in the depletion layer. As a consequence, the forward bias diffusion current increases. (26)

3.5 Current-Voltage (I-V) Relationship of Solar Cell

The accession of the IV curve of a solar cell without illumination and the light-generated current is the IV curve of a solar cell. When photon is absorbed, the IV curve shifts down into the fourth quadrant (27). With the diode under illumination, the light-generated current is added to the "dark" currents. Hence the diode equation becomes:

$$I = I_0 \left[\exp \left(\frac{qV}{nkT} \right) - 1 \right] - I_L \dots\dots\dots 12$$

where I_L = current generated by light.

3.5.1 Current-Voltage (I-V) Relationship of Solar Cell in dark

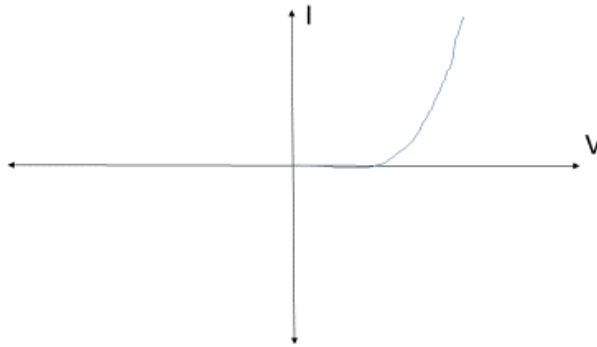


Figure 18: I-V curve of PV cell in dark

3.5.2 Current-Voltage (I-V) Relationship of Solar Cell Under Illumination

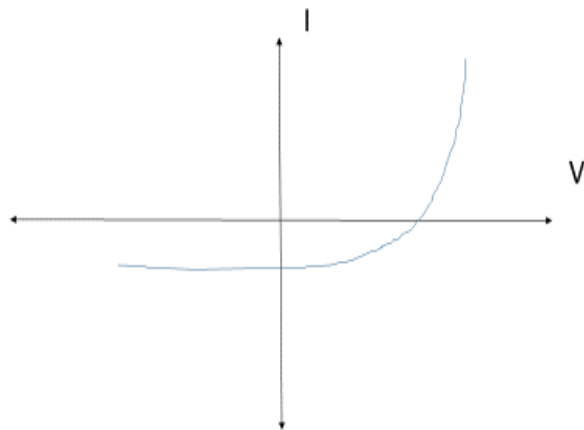


Figure 19: I-V curve of PV cell under illumination

3.6 Summary

The fundamental processes of photovoltaic current generation and the I-V characteristics of PV cell are discussed in this chapter. This chapter also covers the structures of two types of PV cells (FRC and IBC cells) commercially available in the market. The reason behind focusing on FRC cell in this thesis is also mentioned.

4. Structural and Electrical Parameters Contributing to Conversion of Photovoltaic Energy

Effective conversion of photovoltaic energy in PV cells depends on a number of structural factors as well environmental factors. The key structural factors of PV cells which play significant roles in photovoltaic current generation are briefly discussed next in this chapter. After that, electrical parameters associated with efficient photovoltaic energy conversion are discussed.

4.1 Front Contact

The initially developed solar cells did not have any front surface metallization (28). However, the solar cells manufactured at present have front contacts on the top surface over the ARC layer. There are grids of metallic fingers connected to busbars in the front contact. The fingers enhance the conductivity of the cell. It happens because the light-generated carriers are collected more effectively by the regularly spaced fingers. Front contact metallization enhances the efficiency of the cell by increasing collection of the light-generated carriers. On the other hand, series resistance and shading of the metal fingers and contact resistance on the silicon- metal interface increases resistance losses and shading loss (29).

4.2 Back contact

The back contact is formed with metal electrode through which it is connected to the external load or the battery where the DC current generated by light is stored. Heavy P-doping is done the base - back contact interface to reduce surface recombination loss (29).

4.3 Cell thickness

Cell thickness refers to the combined thickness of N region and P region in a PV cell. Standard thickness of silicon wafer used to manufacture PV cells ranges from 200microns to 500microns (30). Experimentally it has been found that, at 10 mm thickness, essentially all the photons with energy above the band gap is captured. However, increasing thickness of the wafer rises the manufacturing cost as well. Hence, optimal cell thickness is important to maximize cell efficiency and minimize production cost.

4.4 Finger shading

The fingers of metalized grid on the front contact cause to create shadow on the cell when light is not projected at a right angle on the PV module. Shadowing results in less absorption of light (31). Hence the width of finger as well as the width of shadow of the finger should be such that shadow loss and series resistance loss are minimized whereas the conductivity is maximized.

4.5 Electrical parameters associated with Solar cell's performance

- **Short circuit current density (I_{sc}):**

The short-circuit current is the current through the solar cell when the terminals of the solar cell are shorted. It is denoted as I_{sc} , the short-circuit current is pointed on the IV curve below.

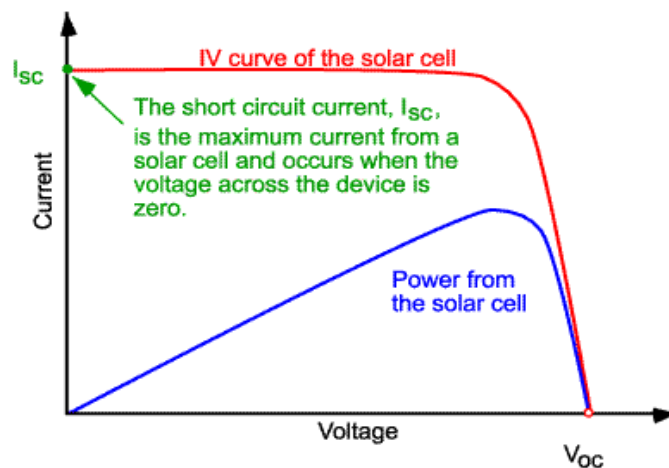


Figure 20: IV curve of a solar cell demonstrating I_{sc} (32).

The I_{sc} exists due to the generation and collection of light-generated carriers. It depends on various aspects (32) as mentioned below:

- the solar cell's area. In order to avoid dependence on the area, it is preferred to work with the short-circuit current density (J_{sc} in mA/cm²).
- the amount of incident photons.
- the air mass index. The standard spectrum is considered to be AM1.5.
- the absorption and reflection capabilities of the cell
- the collection probability.

• **Open Circuit voltage:**

The open-circuit voltage, V_{oc} , is the highest possible voltage across a device when the current is zero. The open-circuit voltage is adduced below (33):

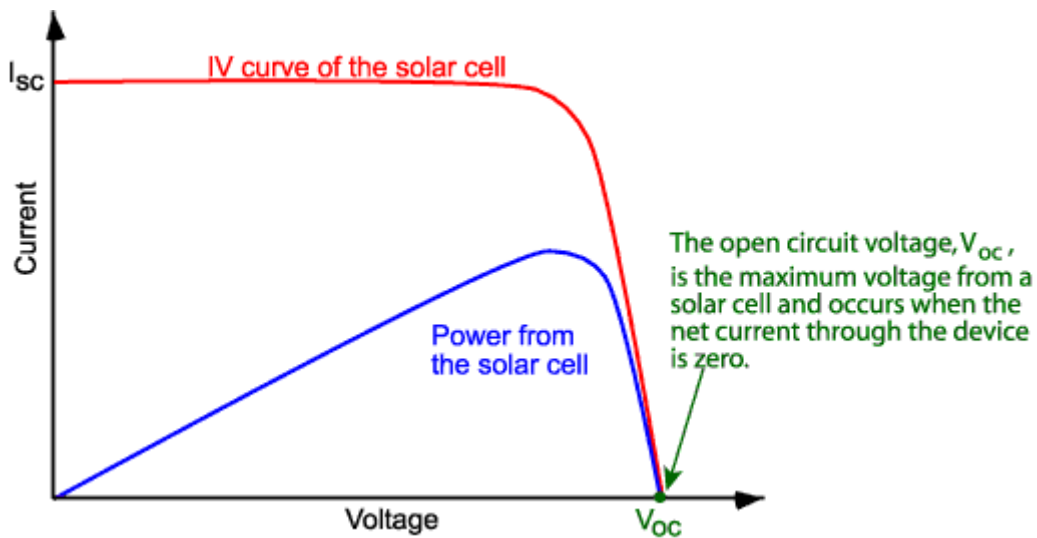


Figure 21: IV curve of a solar cell adducing the V_{oc} (33).

The equation for V_{oc} is deduced by putting the net current equal to zero in the equation no. 13, which comes out as:

$$V_{oc} = nkT \left(\frac{\ln\left(\frac{I_l}{I_0}\right) + 1}{q} \right) \dots\dots\dots 13$$

- **Fill factor (FF):**

Fill factor is a parameter used to determine the maximum power of a solar cell. It is a ratio of the product of maximum operating current and the maximum operating voltage to the product of short circuit current and the open circuit voltage (34).

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}} \dots\dots\dots 14$$

- **Efficiency of Photovoltaic Energy Conversion in Solar Cell (η):**

Solar cell photovoltaic energy conversion efficiency is the primary parameter to evaluate the performances of solar cells. The ratio of energy output from the photovoltaic cell to the input energy from photons radiated from sun equals as the efficiency. When the external and environmental factors are neglected, the efficiency is calculated as (35):

$$\eta = \frac{V_{oc} I_{sc} FF}{P_{in}} \dots\dots\dots 15$$

4.6 Summary

The significant structural parameters of Si PV cell and how these contribute to the ultimate performance of the PV cell are explored in this chapter. To evaluate a PV cell’s performance, several electric parameters are used which are discussed in this chapter as well. In the following chapter, it will be analysed how the physical and structural parameters influence the electric parameters and eventually the performance of solar cell, according to the simulations done for this thesis.

5. Results

At present, the efficiency of photovoltaic energy conversion in crystalline silicon PV cells are over 25% and over 20% for monocrystalline cells and multicrystalline cells respectively, in laboratories. However, the average efficiencies of the silicon solar cells commercially available in the market are between 15% to 20% (36). In this chapter, efficiencies of silicon PV cells have been analyzed varying two parameters of a cell. The cell thickness and the width of shading of finger are varied and the results are noted and analyzed.

5.1 Advanced Solar Cells:

As the need for low-carbon energy keeps on increasing, it is becoming highly necessary to manufacture solar cell modules with higher conversion efficiency that are also feasible in economic ways for large-scale deployment. Extensive researches are being done on advanced PV cells which are different in structures from the conventional silicon PV cells and have the potential to provide higher conversion efficiency at a lower manufacturing cost. The idea of thin Si cells is highly compelling due to the potentiality of reduction in cost (1).

5.2 Methodology:

Conventional Si PV cells are comprised of around 300microns thick wafers on average. Here, the cell thickness of the “thin” cells for simulation is ranging from 400nm to 300microns. The width of half-width of shading of fingers is ranging from 10 microns to 70 microns. Using the Software Quokka 2.0 and the MATLAB 2013b compiler, the simulations are done and the data are noted.

5.3 Data Analysis:

5.3.1 The effect of cell thickness on Voc, Jsc, FF and efficiency

Cell Thickness	Voc (mv)	Jsc (mA/ cm ²)	FF	η
400nm	620	14.8	82%	7.51%
500nm	619	14	82%	7.12%
600nm	618	13.5	82%	6.86%
700nm	617	13.2	82%	6.67%
900nm	616	12.7	82%	6.4%
1 μ m	616	12.5	82%	6.3%
50 μ m	642	33.6	81%	17.5%
100 μ m	644	35.5	80.8%	18.5%
150 μ m	645	36.4	80.8%	19%
200 μ m	645	36.9	80.7%	19.3%
250 μ m	646	37.2	80.7%	19.4%
300 μ m	647	37.4	80.7%	19.5%

Table 2: Simulation results of FRC (Front and rear contact) cell varying cell thickness

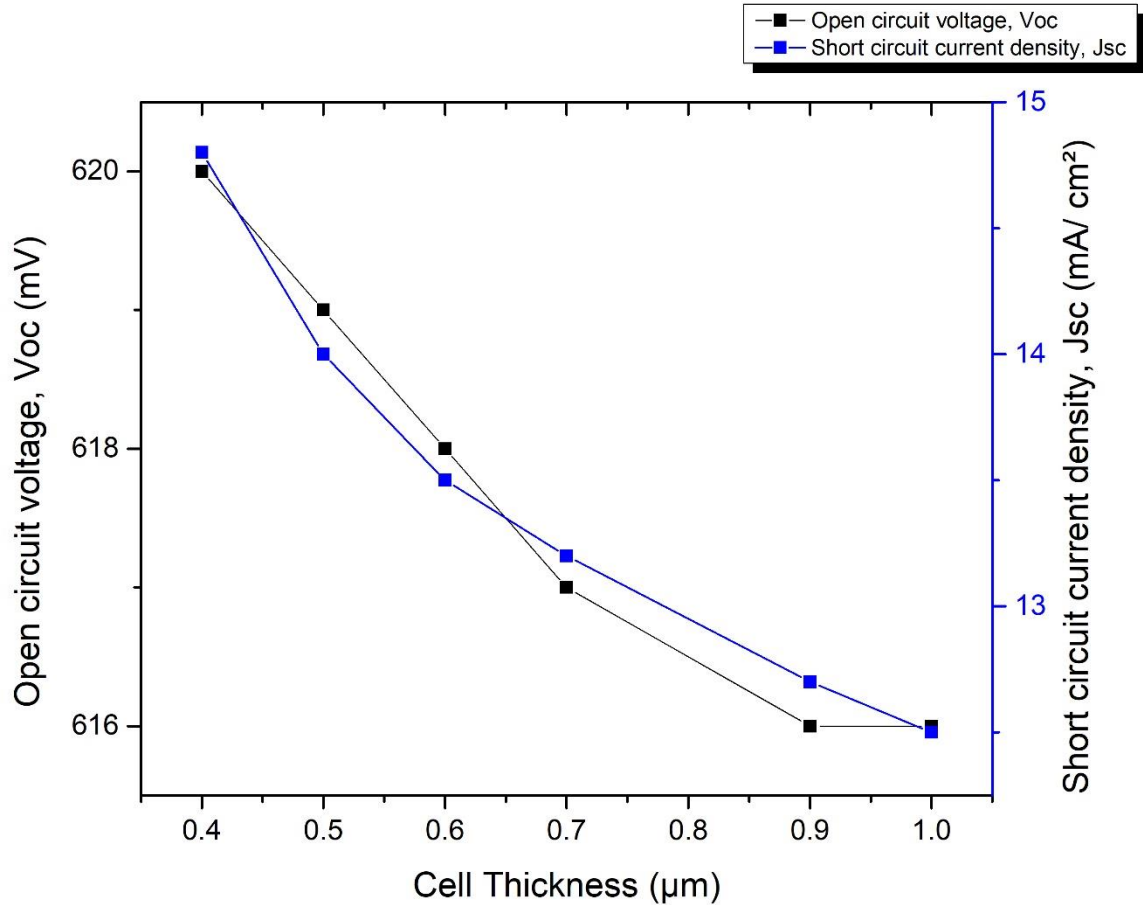


Figure 22: Plot of Voc & Jsc corresponding to cell thickness from 0.4 μm to 1 μm

Discussion:

Respective Voc and Jsc are plotted against the corresponding cell thickness ranging from 0.4 micron to 1 micron in figure22. The Jsc is found to be higher as the cell thickness is reduced due to increased light trapping in thinner cells (29). Light trapping is enhanced due to texturizing and maximizing reflection at the back surface which contribute to achieve optical path length greater than the thickness of the cell (29).

The Voc is also higher as the cell gets thinner. The thinner the cell, the less is the bulk recombination (23). Hence, Voc is increased with the reduction in bulk recombination (SRH, Auger).

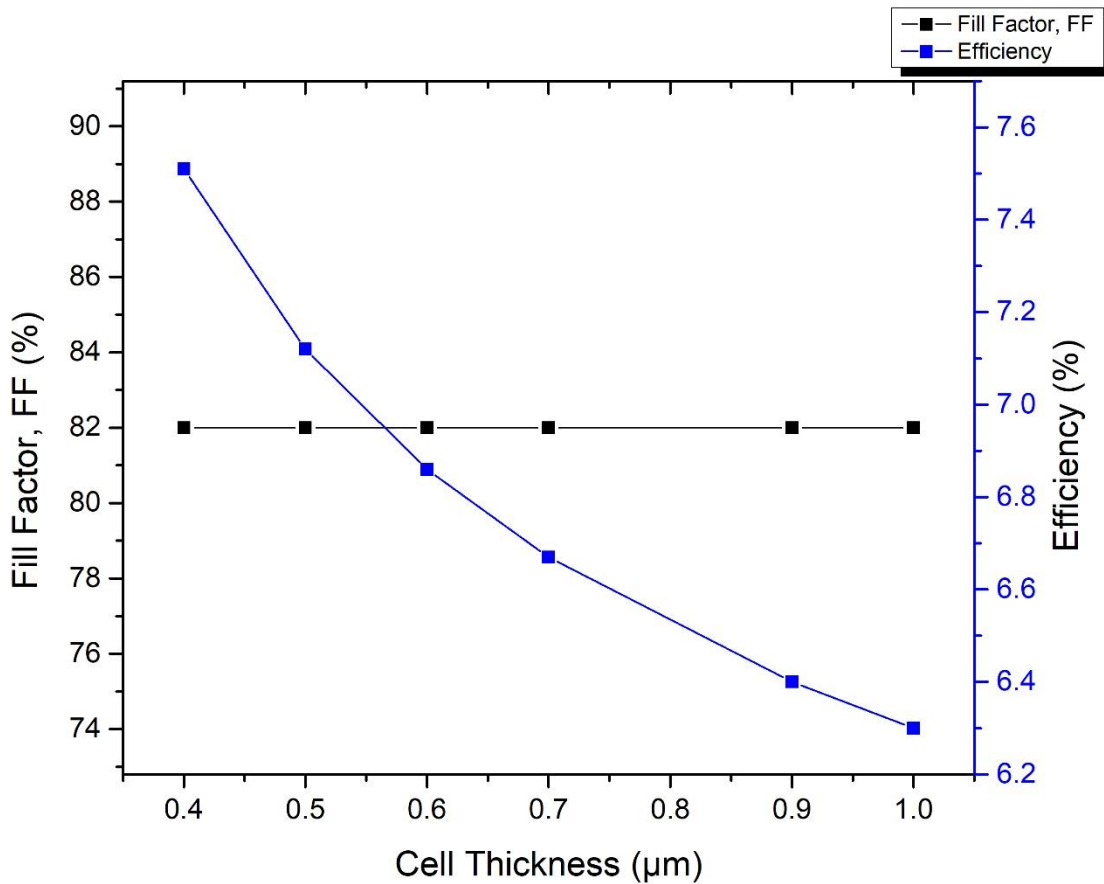


Figure 23: Plot of FF & efficiency corresponding to cell thickness from 0.4 μm to 1 μm

Figure23 shows the FF and efficiency as two functions of cell thickness which ranges from 0.4 micron to 1 micron. The FF remains constant throughout the range at 82% which means the ratio of product of V_m & I_m and that of V_{oc} & I_{sc} are also not changing for this range. It is seen in fig5.1 that V_{oc} and J_{sc} decreases as the cell thickness increases. Hence it is evident that, as the FF is constant, the V_m & I_m also decrease when cell thickness increases.

The efficiency is found to be decreasing while the cell thickness is increased in this range. V_{oc} & J_{sc} are two of the factors on which the efficiency is directly depended on. Hence, the efficiency is decreased as the V_{oc} and J_{sc} decrease.

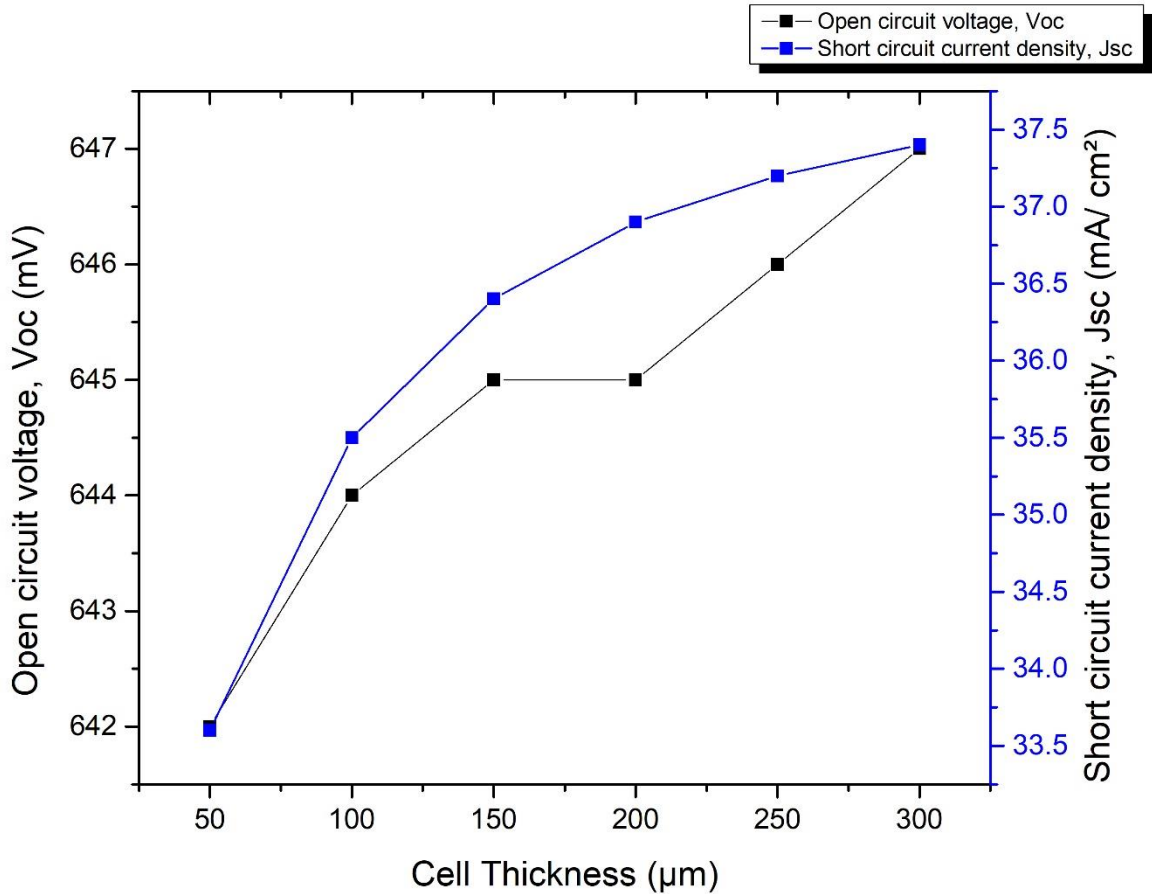


Figure 24: Plot of Voc & Jsc corresponding to cell thickness from 50 μm to 300 μm

On the other hand, in figure24, for cell thickness from 50 microns to 300 microns, both Jsc and Voc are found to be increasing with the increase in cell thickness. In this range, as the wafer thickness increases, it enhances the interaction probability between photon and the cell (37). The higher the interaction probability, the more electron-hole pairs are generated, resulting in higher Jsc. Light absorption is also enhanced with the enhanced wafer thickness, which means more photons are absorbed for charge carrier generations. Furthermore, Voc also increases along with Jsc, as Voc is logarithmically dependent on the light generated current.

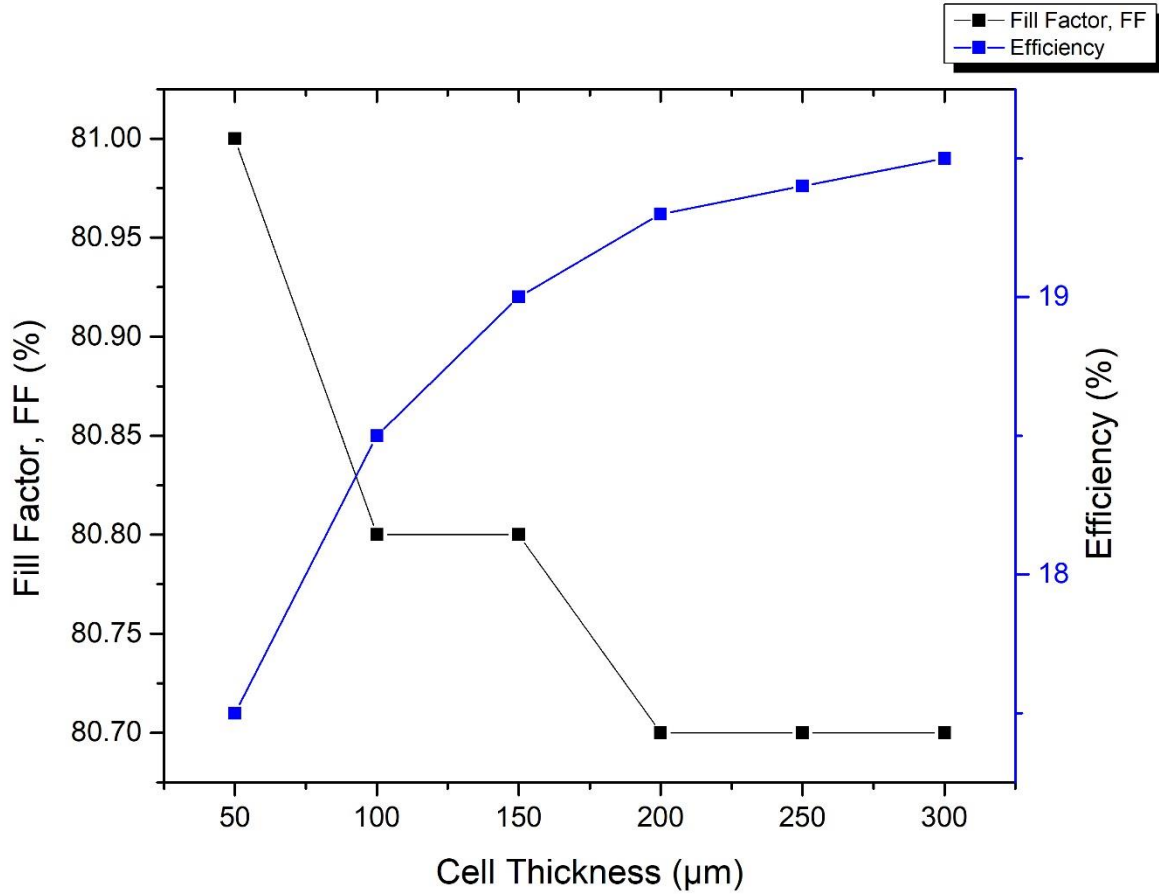


Figure 25: Plot of FF & efficiency corresponding to cell thickness from 50 μm to 300 μm

Figure 25 plots FF and efficiency as two separate functions of cell thickness. In figure 24, it is seen that V_{oc} and J_{sc} rises as the cell thickness increases from 50microns to 300 microns. Efficiency, being directly proportional to V_{oc} and J_{sc} , also increases from 17.5% to 19.5%.

However, the FF decreases with the increases in cell thickness over this interval. Hence, it is assumable that, though V_{oc} & J_{sc} rises, the product of V_m & I_m remains unchanged, causing the FF to fall.

5.3.2 The effect of width of finger shading on Voc, Jsc, FF and efficiency

Half-width in x-direction for shading of fingers	Voc (mv)	Jsc (mA/ cm ²)	FF	η
10 μm	647	38.8	80.6%	20.3%
20 μm	646	38.3	80.7%	20%
30 μm	646	37.8	80.7%	19.7%
40 μm	646	37.2	80.7%	19.4%
50 μm	645	36.7	80.7%	19.2%
60 μm	645	36.2	80.8%	18.9%
70 μm	644	35.7	80.8%	18.6%

Table 3: Simulation results of FRC (front and rear contact) cell varying width of shading of fingers on front contact

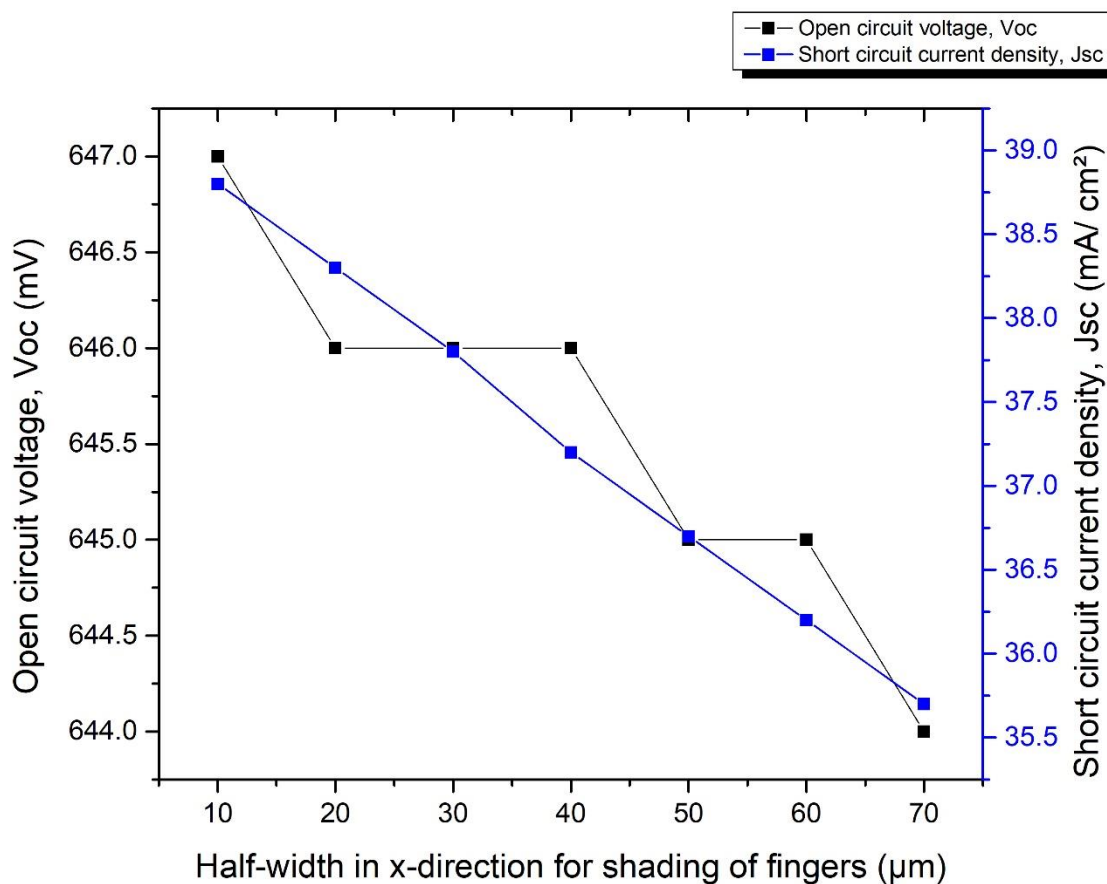


Figure 26: Plot of Voc & Jsc corresponding to width of shading of fingers from 10 μm to 70 μm

Discussion:

Reducing the width of the finger reduces the shading by the finger, which eventually reduces the shading loss. So minimizing the width of the finger shading is a way to enhance the efficiency of the solar cell. However, with fingers of less width, more closely spaced fingers will be needed to obtain higher conductivity of the front contact. More fingers with lesser width, on the other hand, will increase the series resistance loss. Hence, optimizing between minimum finger width and spacing of the fingers is necessary to maximize the efficiency.

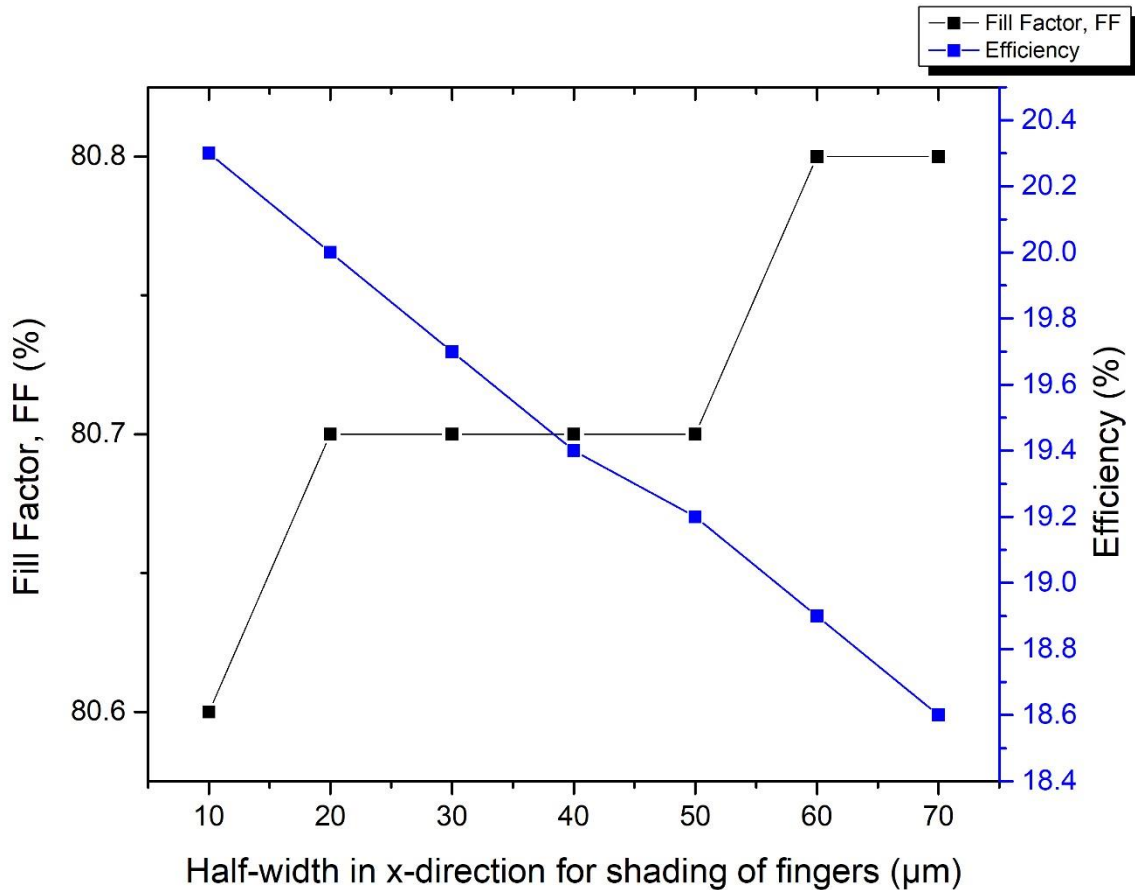


Figure 27: Plot of FF & Efficiency corresponding to half-width of shading of fingers from 10 μm to 70 μm

Here, it is found that, the lesser the finger width, the higher the Voc, Jsc and efficiency. Hence, the shading loss is reduced and conductivity of the front contact is increased with reduced finger width.

The half-width of shading of finger is optimized at $10\mu\text{m}$, as the efficiency is also maximum at this point, indicating the series resistance loss is not too high to curtail the gain of V_{oc} and J_{sc} .

The changes in FF with varying the half-width of shading of finger is rather less significant here. It indicates that, the maximum power of the cell doesn't change significantly as the V_{oc} and J_{sc} reduce, resulting in minor increase in FF.

6. Conclusion

For conventional Si PV cells, 300microns is an optimum thickness of cells, where the maximum efficiency is found. However, using thin wafers reduce the cost significantly. It is found through the simulations that, 0.4micron is the optimum thickness for thin Si PV cells, where the efficiency is maximum, keeping all the other settings as like as the conventional one's. The efficiency of 0.4micron thick cell is still nowhere near that of conventional Si PV cell of 300microns thickness. Therefore, it is needed to focus on other parameters than cell thickness to enhance the efficiency of Si PV cells. On the next step, the effect of minimizing half-width of shading of fingers on V_{oc} , J_{sc} , FF and efficiency is evaluated. While changing the half-width of shading of fingers, the cell thickness was kept constant at 180microns. As it is found, the V_{oc} , J_{sc} and efficiency enhance significantly with the minimization of half-width of shading of fingers. Therefore, in a cell of moderate thickness, higher efficiency can be achieved by an optimized half-width of shading of fingers, which is found to be 10 microns in these simulations.

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