Performance Evolution of Spin Valve Transistor

Course No: EEE 400

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Submitted to

Department of Electrical and Electronic Engineering

In partial fulfillment of the requirements for the degree of Bachelor of Science in

Electrical and Electronic Engineering

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August, 2018

DECLERATION

This is to certify that the research work presented in this thesis is a result of investigation carried out by the authors under the supervision of Md. Anamul Hoque, Lecturer II, Department of Electrical and Electronic Engineering, BRAC University as a requirement of undergraduate degree completion.

It is declared that the findings in this thesis are done the authors by going through several academic resources which is thoroughly mentioned in the reference section.

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Acknowledgement

The authors are thankful to Mr. Md. Anamul Hoque, Lecturer II, Department of Electrical and Electronic Engineering, BRAC University for his tremendous support and direction throughout the exploration process. The authors are also thankful to BRAC University as several resources have been used to prepare this paper.

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Abstract

A necessity of new alternative for electronic devices are arising in which spin property of electron will be engaged for better energy efficiency. Combination of both ferromagnet and semiconductor materials opens the new era of efficiency though faces a challenging route. The spin valve transistor (SVT) is the first among such working hybrid devices which can be the eligible alternative of current semiconductor transistors. This review projects the basic science of spin valve transistor and how current semiconductor transistors are limited by new arising challenges.

Keywords: Spin valve, Hybrid device, Transistor, Ferromagnet, Semiconductor.

Chapter 1

Introduction

Standard information technology is based on charge carriers such as electron and holes. Storing and processing of information can be done by influencing charge carriers. Size of the devices is decreasing along with increasing density every year with the help of current fabrication techniques. Diminution in size enables better performance but also prompt physical size limitation. Smaller structures unveil quantum effects leads to gate tunnel leakage current resulting performance loss. Higher device density provides higher current density hence greater heat dissipation occurs. Therefore energy wastage is also a limitation in traditional technologies.

Spintronics allows minimizing the energy consumption and for information storing and processing in a single device it uses quantum effects. Spin is carried by elementary particles like electrons, holes and nuclei. In traditional devices high carrier concentration express the logical ON (1) state and low carrier concentration express OFF (0) state. But in spintronic on and off state depends on spin current direction and spin polarization. Spin-up defines ON state and spin-down OFF state. Energy required to alter a spin state is much smaller than the energy required for changing the position of charge carriers. Therefore spictronics is preferable.

In 1936 Mott introduce the idea of a spin dependent transport in FM (ferromagnetic) metal which is applicable in devices based on GMR (giant magnetoresistance) and TMR (tunnel magnetoresistance) effect. Different magnetic states can be detected by magnetoresistance effect with the help of magnetization direction. Non-volatile information can be read and write on magnetic disks with the help of magnetoresistance effects. It was the beginning of the information storage development. Then in 1976 Arnov proposed the idea of a non-equilibrium spin distribution in NM (non magnetic) materials. Johnson and Silsbee established the first spin injection and spin transport in aluminum after a decade. This helps in the development of spin-based logic devices. Metal has fixed carrier concentration and very short diffusion length hence it is not very suitable for spintronic. On the other hand semiconductor has variable carrier concentration and long spin consistency. Therefore it is very preferable for spintronic studies.

Spin field effect transistor (SFET) was first introduced by Datta and Das in 1990. Spin transportation and accumulation were studied in metal from then. Host material plays very important role in spintronic device. Materials having low SOC (spin-orbit coupling) like silicon and graphene, provides long spin lifetime and diffusion length. Long spin lifetime and diffusionlength is very useful go spin logic arrays. Again material with large SOC like indium arsenide and gallium arsenide, enables dephasing of the spins.

Chapter 2

Outlook and Review

Semiconductor materials have an electrical conductivity more than insulator but less than conductor. The conductivity of semiconductors can be varied by temperature, impurity contents and optical excitation. Consequently, semiconductors are a prominent choice for electrical devices due to its variability of wide range of electrical properties. Another important property of semiconductor is energy band gap. A wide range of material and devices can be developed with the help of band gap engineering. Transistor is one of those remarkable inventions which is the basic building block of modern day electronic devices. A transistor is a semiconductor device which can be used as amplifier or switch for electronic signals and electronic power. Transistors are very small in size and consume very less energy to operate. A very common field effect transistor is MOSFET (metal oxide semiconductor field effect transistor). Conductivity of the device is determined by an insulated gate voltage. MOSFET needs relatively low input current to control the load current. The invention of MOSCAP (metal oxide semiconductor capacitor) later on leaded to MOSFET. MOSCAP is a two terminal device consists of three layers including a semiconductor body or substrate, an insulator film and a metal electrode. This device operates using the field effect.

2.1 MOSCAP

Transistors are the mostly common used components in any electrical device. They are mainly used as an amplifier or as a switch to control the power of an electrical device. As amplifiers they are used for voltage gain, high or frequency stage, oscillation etc. they are used as a switch in digital circuits. Sizes and prices of electrical circuits decreased dramatically for past few decades due to the implementation of transistors. There are two kinds of transistors available. One is bi-polar junction transistor(BJT) and field effect transistor(FET).

MOS or metal-oxide-semiconductor is called the heart of MOSFET. Whether, there is a variation in type where high conductive polycrystalline silicon is used as a substitute of metal in MOS capacitor. The basic structure of MOS capacitor is a semiconductor substrate with a thin layer of oxide with a metal contact on top of it. The metal contact works as a capacitor. This is known as gate. Another metal contact layer exists on the opposite side of semiconductor which creates an Ohmic contact with semiconductor, is known as bulk contact.

2.2 Basic working principle of MOSCAP

Flat band voltage is an important term of MOS capacitor. It refers as the capacitor is has no electric charge and the oxide layer contains no static electric field across it. A voltage that applied on the gate is called gate voltage. This voltage induced an electric field between two plates. The magnitude of electric field between two plates is defined as –

$$E=v/d$$

Where v is voltage applied to the gate and d is the distance between two plates.

The capacitance per unit area is defined as-

$$C=e/d$$

Here, 'e' is denoted as permittivity of the insulator.

There are three different mode of MOS operation – accumulation, depletion and inversion. And they depend on the three different kind bias voltages- flat band voltage(V_B), gate voltage(V_G) and threshold voltage(V_T).

When the applied gate voltage (V_G) is less than flat band voltage (V_B) then a negative charge induced in the gate and attracts the holes to the oxide semiconductor interface from semiconductor substrate. This operation is known as accumulation and the layer that is created under the oxide layer is called accumulation layer.

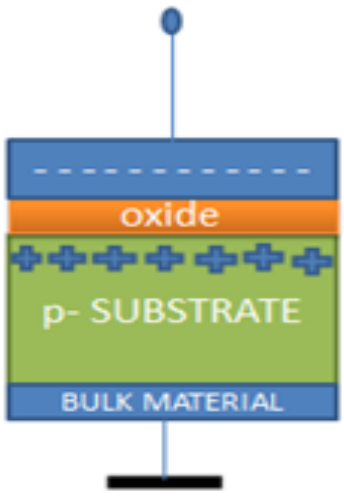


Figure 2.2.1: Vg<Vb (Accumulation)

Depletion occurs for positive voltage that is applied to the gate. Hence, the gate voltage is larger than the flat band voltage(Vb). The positive voltage from the gate will ripple the positive charge of the

semiconductor substrate and create a space charge region keeping negative charges. So the semiconductor is depleted of the mobile carriers at the interface and the region is named as the depletion region.

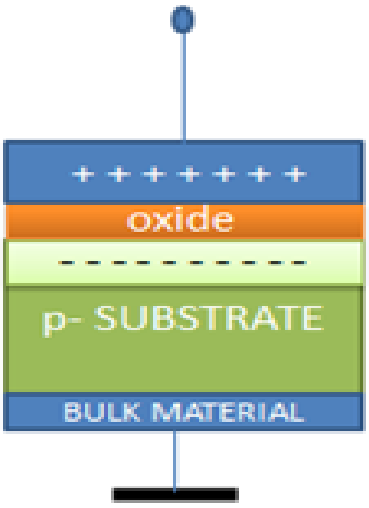


Figure 2.2.2: Vb<Vg<Vt (Depletion)

If a large amount of positive charge is applied to the gate than an inversion layer occurs in addition to the depletion region. In this case, gate voltage is larger than the threshold voltage. Inversion layer occurs due to the existence of negatively charged minority carrier under oxide layer. Minority carriers are attracted to the interface by positively charged gate voltage.

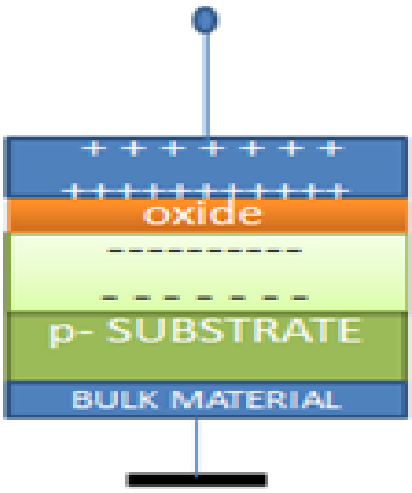


Figure 2.2.3: Vt<Vg (Inversion)

2.3 Energy band diagrams of MOSCAP

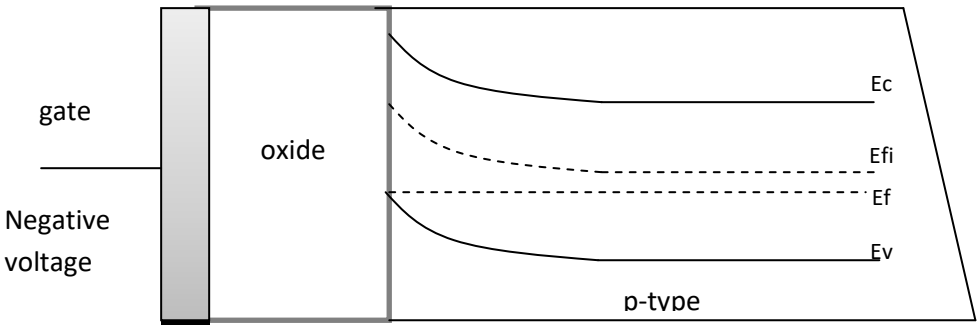


Figure 2.3.1: The energy band diagram of the MOS capacitor with a p-type substrate for a negative gate bias.

When a negative charge is applied to the gate of a MOS capacitor with p-type substrate, valance band moves closer to the Fermi level at oxide-semiconductor region rather than bulk material. That implies the accumulation of holes. Fermi level remain constant since there is no current through the oxide with thermal equilibrium.

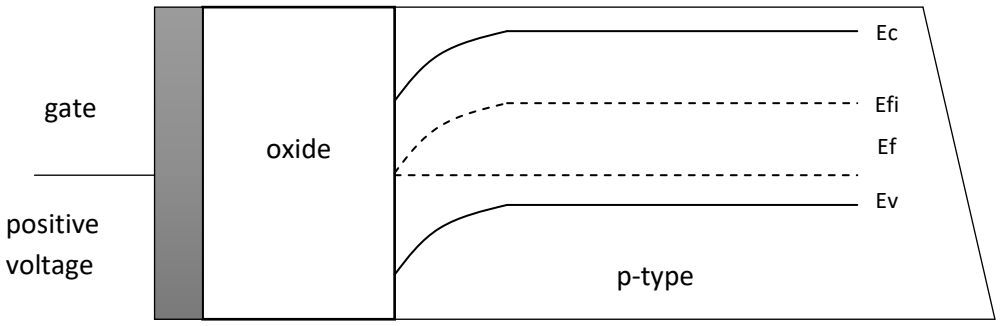


Figure 2.3.2:The energy band diagram of the MOS capacitor with a p-type substrate for a moderate positive gate bias.

In case of positive charge applied to the gate, intrinsic Fermi level and conduction band level bend opposite and move closer to the Fermi level. A space charge region is formed under oxide layer.

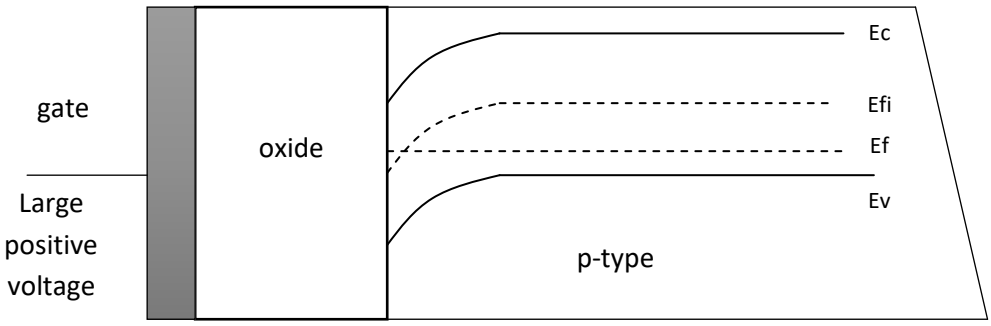


Figure 2.3.3: The energy band diagram of the MOS capacitor with a p-type substrate for a large positive gate bias.

Applying large positive voltage causes greater space charge region and more band bending. So the intrinsic Fermi level goes under the constant Fermi level and inversion layer is exposed to invert the p-type semiconductor layer to n-type.

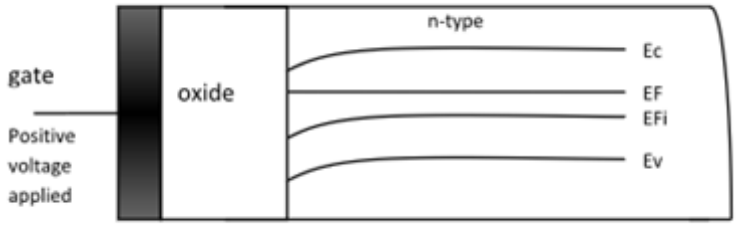


Figure 2.3.4: The energy band diagram of the MOS capacitor with an n-type substrate for a positive gate bias.

When a positive charge is applied to the gate of a MOS capacitor with n-type substrate, conduction band moves closer to the Fermi level at oxide-semiconductor region rather than bulk material. That implies the accumulation of electrons. Fermi level remain constant since there is no current through the oxide with thermal equilibrium.

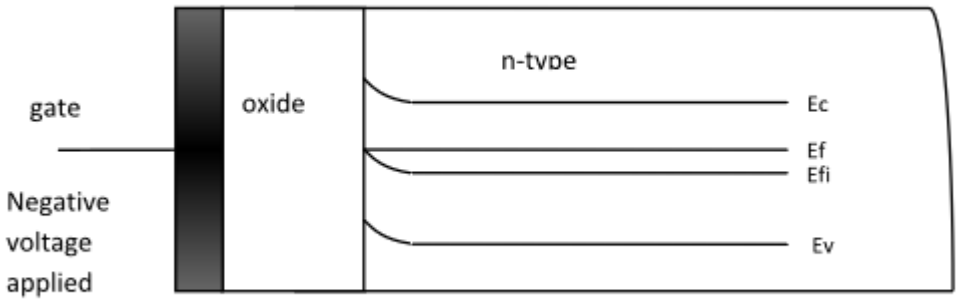


Figure 2.3.5: The energy band diagram of the MOS capacitor with an n-type substrate for a moderate negative gate bias.

In case of negative charge applied to the gate, intrinsic Fermi level and valence band level bend opposite and move closer to the Fermi level. A space charge region is formed under oxide layer.

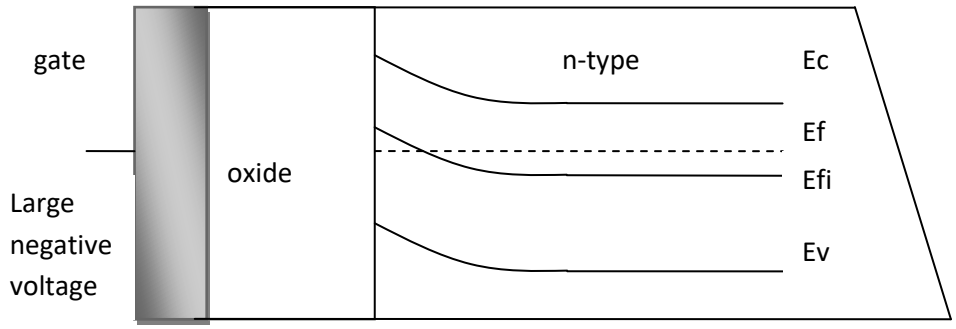


Figure 2.3.6: The energy band diagram of the MOS capacitor with an n-type substrate for a large negative gate bias.

Applying large negative voltage causes greater space charge region and more band bending. So the intrinsic Fermi level goes over the constant Fermi level and inversion layer is exposed to invert the n-type semiconductor layer to p-type.

2.4 MOSFET

MOSFET (Metal Oxide Semiconductor to Field Effect Transistor) is a semiconductor device usually fabricated by the controlled oxidation of silicon. It is a four terminal device with source, gate, drain and body. There basically two types of MOSFET 1) Depletion type and 2) Enhancement type. In enhancement

type MOSFET if the gate voltage is increased the conductivity of the device will also be increased. In depletion type conductivity of device will decrease if gate voltage is increased. MOSFET is used as a switch in electronic signals or used to amplify the signal. It is a unipolar transistor that contains only one type of charge carriers. Comparing to bipolar transistors it requires almost no input current to get a high load current.

2.5 Structure of MOSFET

The MOS structure is obtained by making a thin layer of silicon oxide (SiO2) on the top of the body and a metal layer on the top of SiO2 layer. To make it p-type material the body which is also known as substrate is doped with p+ region. To make n-channel source and drain is doped with n+ region. To make it n-type material the body which is also known as substrate is doped with n+ region and to make n-channel source and drain is doped with n+ region. There is a layer of metal on the top of source and drain terminals.

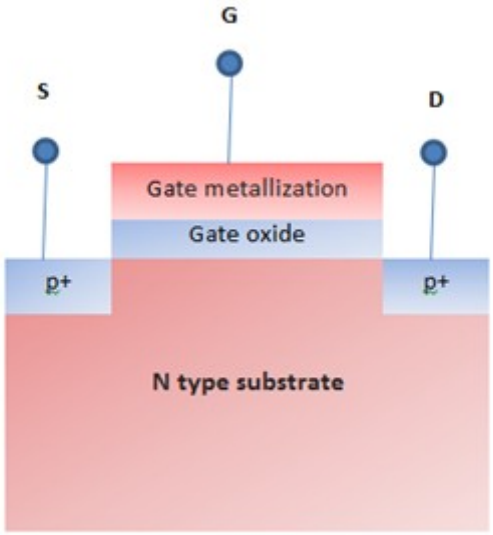


Figure 2.5.1: Structure of N-type MOSFET

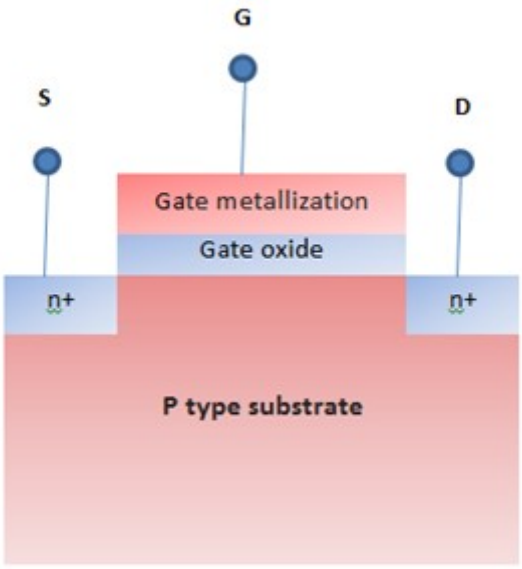


Figure 2.5.2: Structure of p-type MOSFET

2.6 Working Principal of N-Channel MOSFET

As the body is p-type so the majority charge carriers of body is hole and minority carrier is electron. If positive gate voltage is applied; because of its voltage positive charge will be pushed away from the gate terminal and a depletion region will be created. Negative charge will be attracted near the surface and the region will become n-type. This is called inversion. This inversion layer will connect the source and drain region. Channel width and conductivity increase when the voltage of gate to source terminal is increased. After the conduction electron will flow from the source terminal to drain terminal.

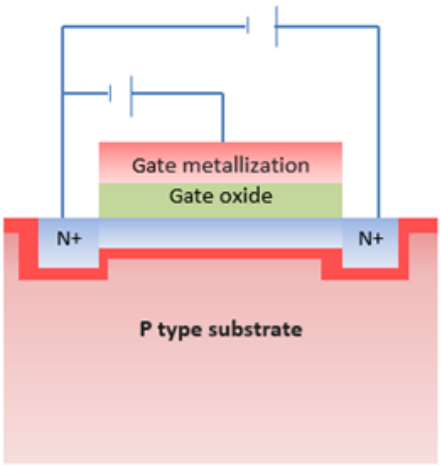


Figure 2.6.1: N channel enhancement mode MOSFET

If little amount of voltage is given at drain terminal current will start to flow. The direction of this current flow is from drain to source terminal. At this case the depletion region is uniformed. For this little amount of drain voltage the characteristics of channel region is given by

$$I_D = g_d V_{DS}$$

Here g_d is the conductance of the channel. No drain current will flow if threshold voltage is above the gate voltage and no inversion layer will be created. When this one is higher than the threshold voltage, inversion layer form and the conductance increase. If we increase the value g_d it will give a larger slope of theI_D versus V_{DS} graph.

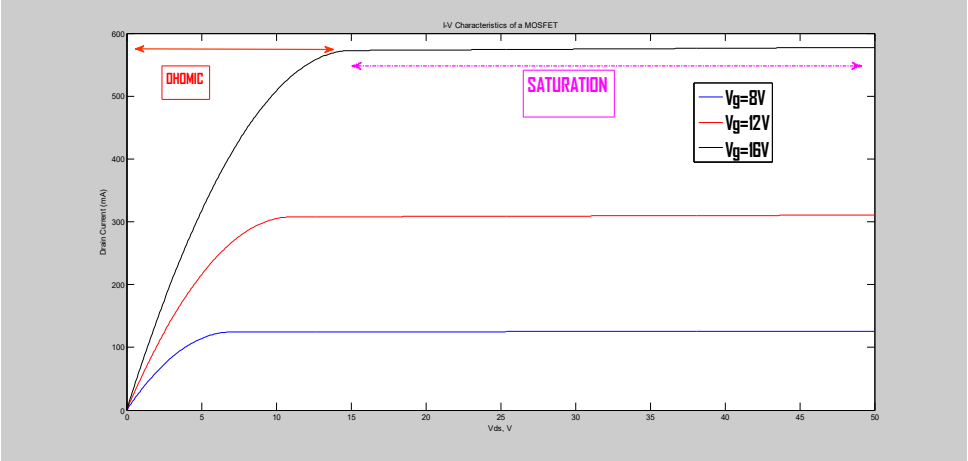


Figure 2.6.2: Current-voltage characteristics of MOSFET

When no drain voltage is applied; gate to drain voltage and gate to source voltage are equal. But for a increased value of drain voltage; drain will become more positive and the depletion region will be no longer uniformed. This will make the width of channel reduced and width of depletion layer increased near the drain terminal. If drain voltage is increased in such a way that the gate to substrate potential at the drain terminal becomes smaller than threshold voltage; therefore the channel thickness at drain terminal becomes zero which is known as pinch off condition. The current I_D reaches its saturation point at the value just prior to pinch off. At that point at drain terminal inversion charge density which is induced will be zero and the slope of Id versus V_{DS} will be zero. The curve reaches at its saturation region.

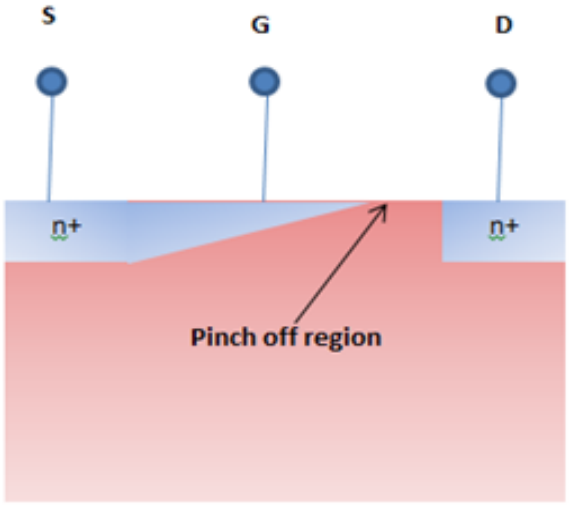


Figure 2.6.3: Pinch off region

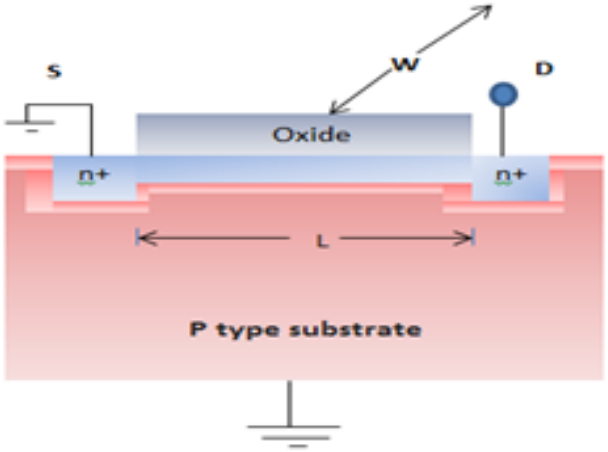


Figure 2.6.4: Cross section of N channel MOSFET

$$V_{DS}(sat) = V_{GS} - V_T$$

Therefore three operation region for MOSFETs are:

1) Cut-off region: (n-MOS):

$$V_{GS} < V_{TH}$$

$$I_D = 0$$

2) Linear region: (n-MOS):

$$V_{GS} > V_{TH}$$

$$V_{DS} < V_{GS} - V_{TH}$$

$$I_D = \frac{W\mu_n C_{ox}}{2L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]$$

3) Saturation region: (n-MOS):

$$V_{GS} > V_{TH}$$

$$V_{DS} > V_{GS} - V_{TH}$$

$$I_D = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_{TH})^2$$

2.7 Working Principal of P-Channel MOSFET

As the body is n-type so the majority charge carriers of body is now electron and minority carrier is hole. If negative voltage is applied to the gate terminal; from this terminal negative charge will be pushed away for this voltage and a depletion region will be created. Positive charge will be attracted near the surface and the region will become more like p-type. So inversion layer will be created. This inversion layer will connect the source and drain region. Channel width and conductivity will increase if the gate to source voltage is increased. After the conduction the direction of flow of hole is from the source to drain terminal and current will follow the direction of hole`s movement.

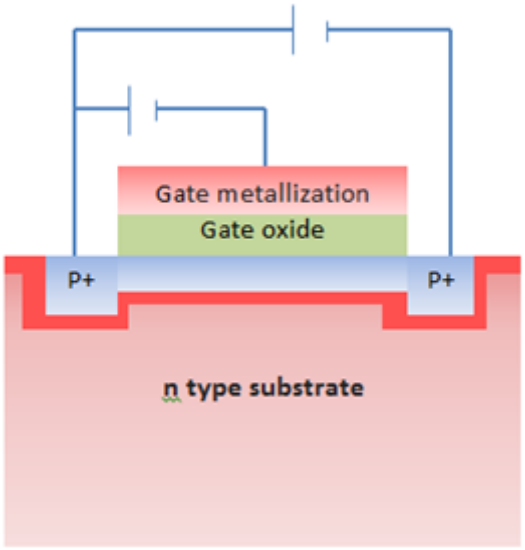


Figure 2.7: P channel enhancement mode MOSFET

2.8 Working Principal of Depletion Mode MOSFET

Unlike enhanced mode, MOSFET channel is present before any voltage is applied in depletion type MOSFET. Maximum conductance of the channel will occur when voltage is applied on the gate terminals zero and if voltage is applied the conductivity of channel will start to decrease.
When no gate voltage is applied and at drain positive voltage is applied current will start to flow through the channel. An increment of positive voltage in drain terminal will increase flow of current. If this voltage is more increased the depletion region at drain terminal will also increase and will leave the channel being narrow and will limit the flow of electron.

If negative gate voltage is applied it will attract holes and electron will be pushed away and the conductivity will decrease.

If positive gate voltage is applied minority charge carrier from body will attracted to the channel and collision will occur between the accelerating particle and new carrier will be established and drain current will increase rapidly.

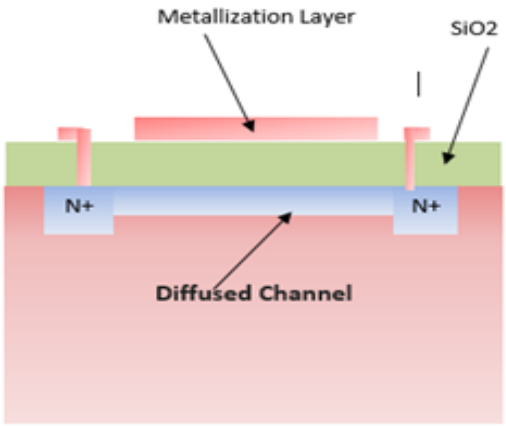


Figure 2.8: Depletion mode MOEFET

2.9 Schottky barrier diode

Schottky barrier diode is formed when metal and moderately doped n-type semiconductor makes contact. The forward voltage drop of this diode is between 0.15 and 0.45 volts which is much lower than normal diodes (0.6-1.7) volts. As the voltage drop is very less schottky diode provides better system efficiency and very fast switching. In between semi-conductor and metal a metal semiconductor junction is developed where metal acts as anode and semi-conductor acts as cathode.

(a) (b)

Figure 2.9: (a) Symbol of schottky diode and (b) internal structure of schottky barrier diode.

2.10 Schottky diode construction

At one side a metal semiconductor junction is forms which is a unilateral junction and at the opposite side another junction is formed which is known as an ideal ohmic bilateral contact. It is a perfectOhmic two-

sided contact without any potential existing within metal and semiconductor. It is non-rectifying. The implicit potential over the open circuited Schottky obstruction diode portrays the Schottky barrier diode. It is a component of temperature and doping. It diminishes with expanding temperature and doping fixation in N-type semiconductor. The regular metals utilized to produce Schottky barrier diode are molybdenum, platinum, chromium, tungsten, aluminum, gold etc. The semiconductor utilized is N-type silicon.

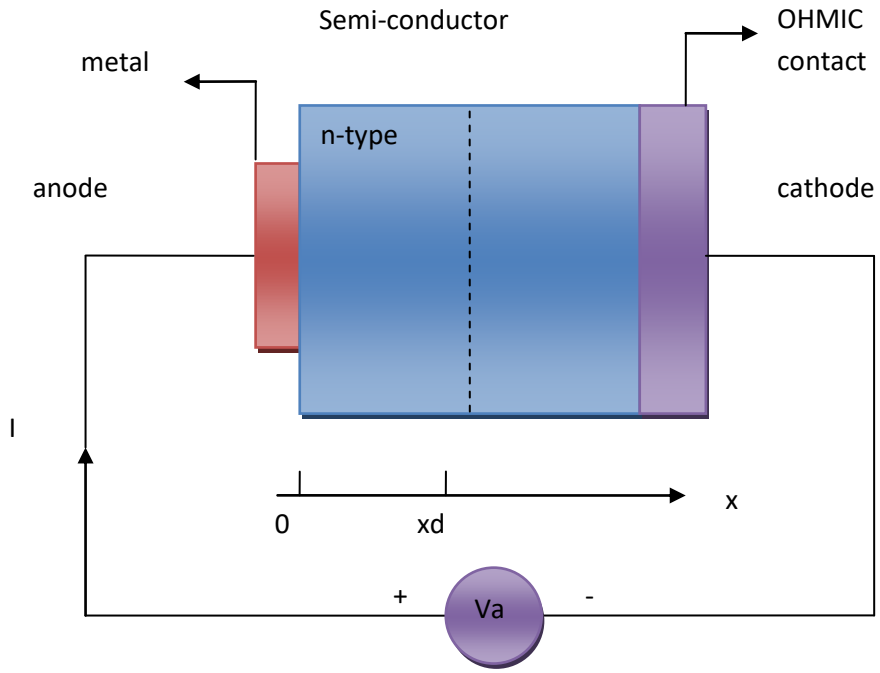


Figure 2.10: Physical construction of Schottky diode.

2.11 I-V characteristics of Schottky barrier diode

I-V characteristic of Schottky diode and normal PN junction diode is similar but the forward voltage drop of Schottky barrier diode is less. If the doping concentration of N-type semi-conductor increases than the forward voltage drop also increases.

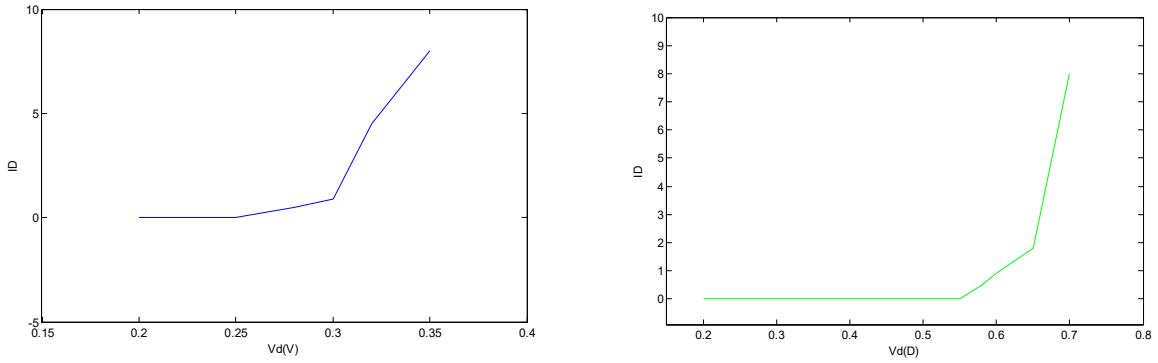
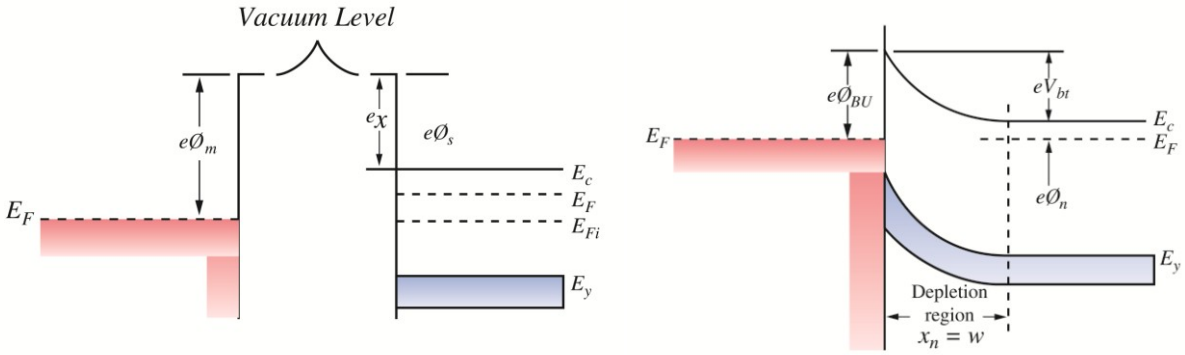


Figure 2.11: Schottky diode v/s normal diode IV characteristics.

2.12 Energy-band diagram of Schottky diode

Here, the vacuum level is used as a reference level. Φm is metal work function and ϕs is semiconductor work function and X is electron affinity. Here ϕm>ϕs therefore to achieve thermal equilibrium electron from semiconductor flow in to metal. Positively charge donor atom remains in semiconductor and creates a space charge region.



(a) (b)

Figure 2.12:1 (a) Energy-bnd diagram of a metal and semiconductor before contact; (b) ideal energy-band diagram of a metal-n-semiconductor junction for ϕm>ϕs.

ϕB0 is ideal barrier height. This barrier is called Schottky barrier.

$$\phi B0=(\phi m-X)$$

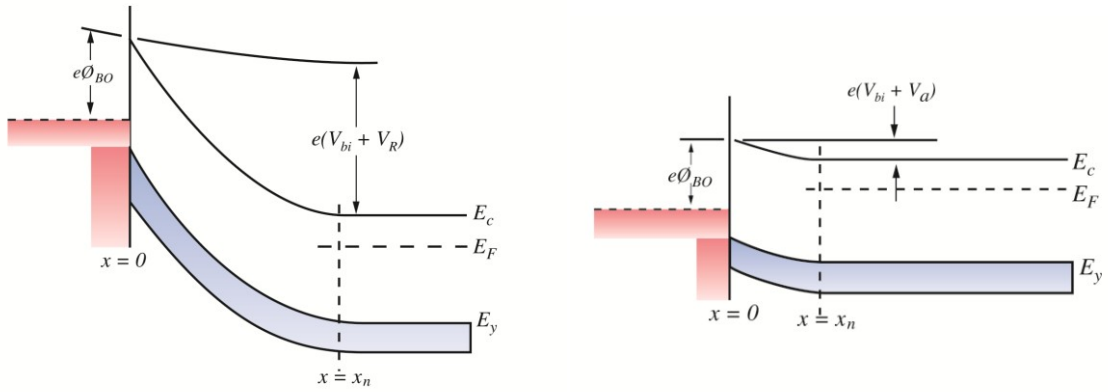
Table 2.12 shows schottky barrier for various materials,

Element	Work function,ϕm	Element	Electron affinity, X	Schottky diode	Schottky barrier (ϕb0=ϕm-X)
Platinum,Pt	5.65	Silicon,si	4.01	PtSi	1.64v
Palladium,Pd	5.12	Silicon,si	4.01	PdSi	1.11
Titanium,Ti	4.33	Silicon,si	4.01	TiSi	0.32
Tungsten,W	4.55	Silicon,si	4.01	WSi	0.54
Aluminium,Al	4.28	Silicon,si	4.01	AlSi	0.27
Silver,Ag	4.26	Silicon,Si	4.01	AgSi	0.25
Gold,Au	5.1	Silicon,Si	4.01	AuSi	1.09
Chromium,Cr	4.5	Silicon,Si	4.01	CrSi	0.49
Molybdenum, Mo	4.6	Silicon,Si	4.01	MoSi	0.59
Nickel,Ni	5.15	Silicon,Si	4.01	NiSi	1.14
Platinum,Pt	5.65	Germanium,Ge	4.13	PtGe	1.52
Palladium,Pd	5.12	Germanium,Ge	4.13	PdGe	0.99
Titanium,Ti	4.33	Germanium,Ge	4.13	TiGe	0.20
Tungsten,W	4.55	Germanium,Ge	4.13	WGe	0.42
Aluminium,Al	4.28	Germanium,Ge	4.13	AlGe	0.15
Silver,Ag	4.26	Germanium,Ge	4.13	AgGe	0.13
Gold,Au	5.1	Germanium,Ge	4.13	AuGe	0.97
Chromium,Cr	4.5	Germanium,Ge	4.13	CrGe	0.37
Molybdenum, Mo	4.6	Germanium,Ge	4.13	MoGe	0.47
Nickel,Ni	5.15	Germanium,Ge	4.13	NiGe	1.02
Platinum,Pt	5.65	Gallium arsenide,GaAs	4.07	PtGaAs	1.58
Palladium,Pd	5.12	Gallium arsenide,GaAs	4.07	PdGaAs	1.05
Titanium,Ti	4.33	Gallium arsenide,GaAs	4.07	TiGaAs	0.26
Tungsten,W	4.55	Gallium arsenide,GaAs	4.07	WGaAs	0.48
Aluminium,Al	4.28	Gallium arsenide,GaAs	4.07	AlGaAs	0.21
Silver,Ag	4.26	Gallium arsenide,GaAs	4.07	AgGaAs	0.19
Gold,Au	5.1	Gallium arsenide,GaAs	4.07	AuGaAs	1.03
Chromium,Cr	4.5	Gallium arsenide,GaAs	4.07	CrGaAs	0.43
Molybdenum, Mo	4.6	Gallium arsenide,GaAs	4.07	MoGaAs	0.53
Nickel,Ni	5.15	Gallium arsenide,GaAs	4.07	NiGaAs	1.08
Platinum,Pt	5.65	Aluminiumarsenide, AlAs	3.5	PtAlAs	2.15
Palladium,Pd	5.12	Aluminiumarsenide, AlAs	3.5	PdAlAs	1.62
Titanium,Ti	4.33	Aluminiumarsenide, AlAs	3.5	TiAlAs	0.83.

Element	Work function, ϕm	Element	Electron affinity, X	Schottky diode	Schottky barrier (ϕb0=ϕm-X)
Silver,Ag	4.26	Aluminiumarsenide, AlAs	3.5	AgAlAs	0.76
Gold,Au	5.1	Aluminiumarsenide,Al As	3.5	AuAlAs	1.6
Chromium,Cr	4.5	Aluminiumarsenide, AlAs	3.5	CrAlAs	1
Molybdenum, Mo	4.6	Aluminiumarsenide, AlAs	3.5	MoAlAs	1.1
Nickel,Ni	5.15	Aluminiumarsenide, AlAs	3.5	NiAlAs	1.65
Tungsten,W	4.55	Aluminiumarsenide,Al	3.5	WAlAs	1.05

Table 2.12: Schottky barrier for different materials

Applied positive voltage in semiconductor with respect to metal causes increase in barrier height. In ideal cases ϕb0 remains constant. This is called reverse bias condition. The semiconductor to metal barrier height can be reduced by applying positive voltage into metal. Φb0 remain constant. It is easy for electron to flow from semiconductor to metal in forward bias condition.



(a) (b)

Figure 2.12.2: (a) At reverse bias condition, Energy band diagram of a metal-semiconductor junction. (b) At forward bias condition, energy band diagram of a metal-semiconductor junction.

2.13 Metal-semiconductor ohmic contacts

Ohmic contacts are not rectifying and it is metal to semiconductor contacts.ohmic contact has low resistance and it provides conduction in both direction like metal to semiconductor or semiconductor to metal. There are two possible types of OHMIC contacts and they are non-rectifying barriers and tunneling barriers.

2.13.1 Ideal non rectifying barrier

In ideal non rectifying contacts work function of metal is less than work function of metal (ϕm<ϕs). To reach thermal equilibrium electron from metal will flow toward semiconductor and surface of semiconductor will become more n-type. Electrons can easily flow from metal to semiconductor when positive voltage is given to metal.Because the barrier height is very little and approximate height is (ϕbn=ϕn).

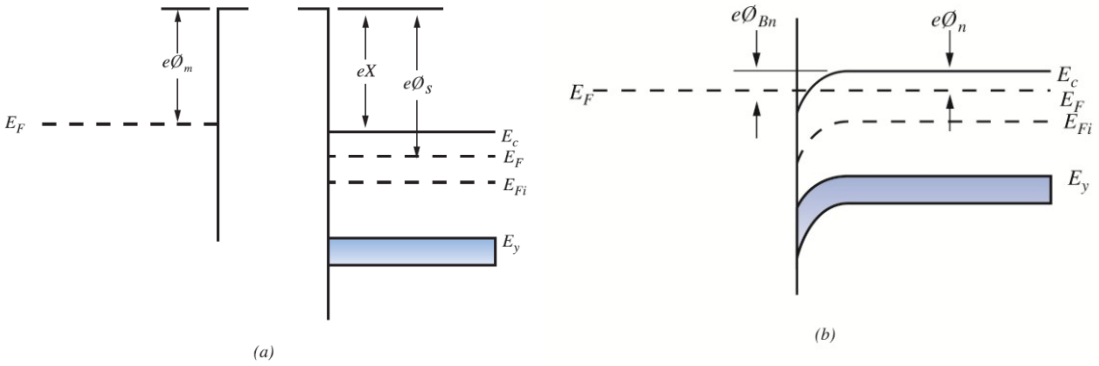


Figure 2.13.1: energy band diagram of a metal-n-semiconductor junction for ϕm<ϕs (a) before contact and (b) after contact.

2.13.2 Tunneling barrier

Width of the depletion region can be reduced by increasing semiconductors doping concentration. Therefore electron can easily flow from one side to another.

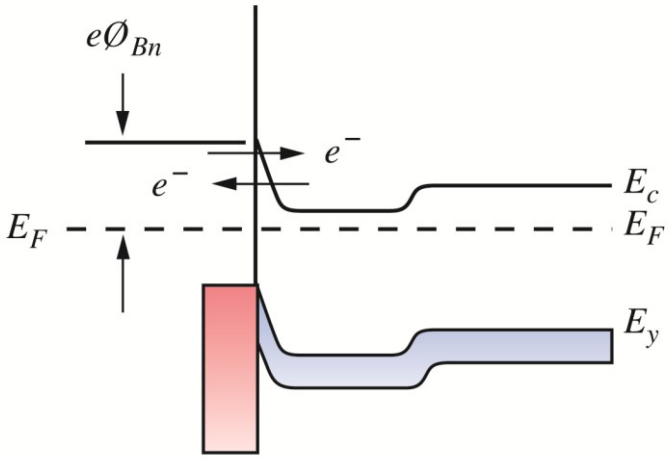


Figure 2.13.2: Energy band diagram of a heavily doped n-type semiconductor to metal junction.

2.14. Limitations of semiconductor transistor

Though transistor feature size has been scaled down over the year, voltage scaling did not follow the same trend. From the figure 2.14.1, it can be seen that feature size scaling down has been accelerated to every two years since 90 nm generation. On the other hand, operating voltage was reduced in proportion to feature size until the 130 nm node. Later on, it slowed down. From the figure 2.14.2, it can be observed that operating voltage is maintained at 5 volts by convention initially. A new convention of 3.3 volts was introduced when voltage reduction was required. Log space regression shows that voltage scale as the square root of feature size between the 0.6 um and 130 nm nodes. The phenomena shows that though transistor size can be made small to further extent, reduction of operating voltage is still a challenge.

On the other hand, MOSFET used in processors face some physical limitations as well. Along with the reduction of size, quantum tunneling affects the performance of the MOSFET severely. Additionally, heat emission of processor is another issue to resolve.

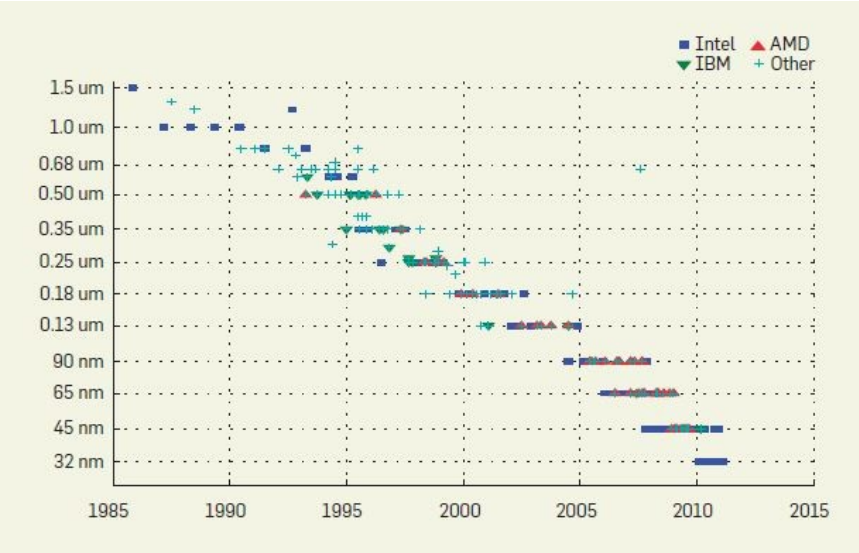


Figure2.14.1: Transistor feature size over time

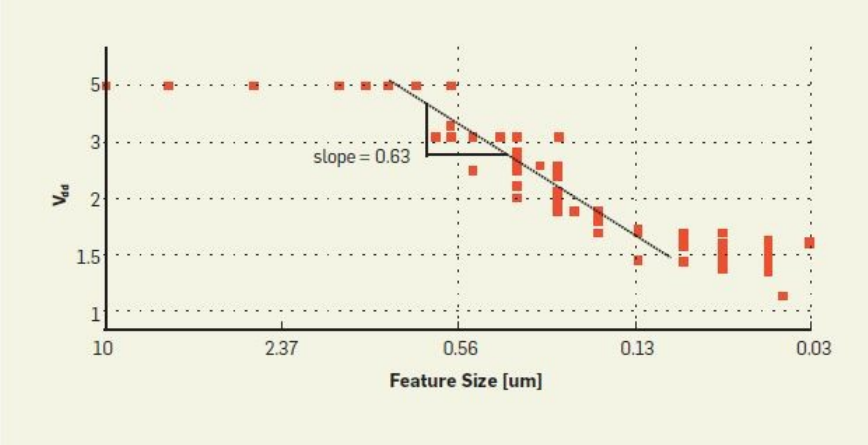


Figure 2.14.2: Voltage vs. Feature size

Chapter 3

Spin Valve Transistor

3.1 Spin based devices

Spintronics allows us to manipulate electron spin and resulting magnetic moment to achieve improved functionalities than conventional semiconductor transistors. An electron carries both charge and spin component. Generally, normal metals have an equal number of electrons with up and down spin. Hence, these materials can sustain a charge current with a zero net spin component in equilibrium condition. However, by passing a current from ferromagnet into metal can transfer spin between separate ferromagnets. Using magnetization dynamics induced by ferromagnetic resonance, spin current can be injected into semiconductors as well with a very high efficiency. Spintronics came into light by the advancement of Giant magnetoresistance (GMR). It was first introduced in 1988 where multilayered structure was constructed with layers of ferromagnetic metal separated by a normal metal layer. The resistance of such structure mainly depended on the magnetic orientation of neighboring magnetic layers. In early 1997, it was used into read-heads of magnetic hard disc recording systems. It was one of the main factors enabling increase in storage density. Later on, tunnel magnetoresistance (TMR) was introduced in 1995 where two ferromagnetic electrodes was separated by a thin layer of insulator. TMR was used to create magnetic random access memory (MRAM) which was non-volatile, had low power consumption and fast switching speed. Though spintronics gave some ground breaking advancement, core element of electronics which is transistor with its amplification was always missing. Conventional semiconductors allow precise tuning of carrier concentration and band gap engineering. Merging key benefits from both semiconductor and spintronics permits us creating improved transistors and memory devices. Hybrid devices are one of few structures that combine the properties of semiconductor and ferromagnetic materials. Magnetic film layer is grown over silicon substrate and a silicon layer above it.

Figure 3.1: Schematic representation of Hybrid Device

3.2 Spin valve transistor

The Spin Valve Transistor (SVT) is a hybrid device consisted of ferromagnets and semiconductors. The device has three terminals similar to conventional structure of bipolar transistor – emitter/base/ collector. The base region is constructed with at least two ferromagnets separated by normal metal layers. Relative magnetic orientation of these two ferromagnet layers determines the transmission of the base. These layers can be mentioned as electron spin polarizer and analyzer of the device. Consequently, collector current depends on magnetic layer of the base.

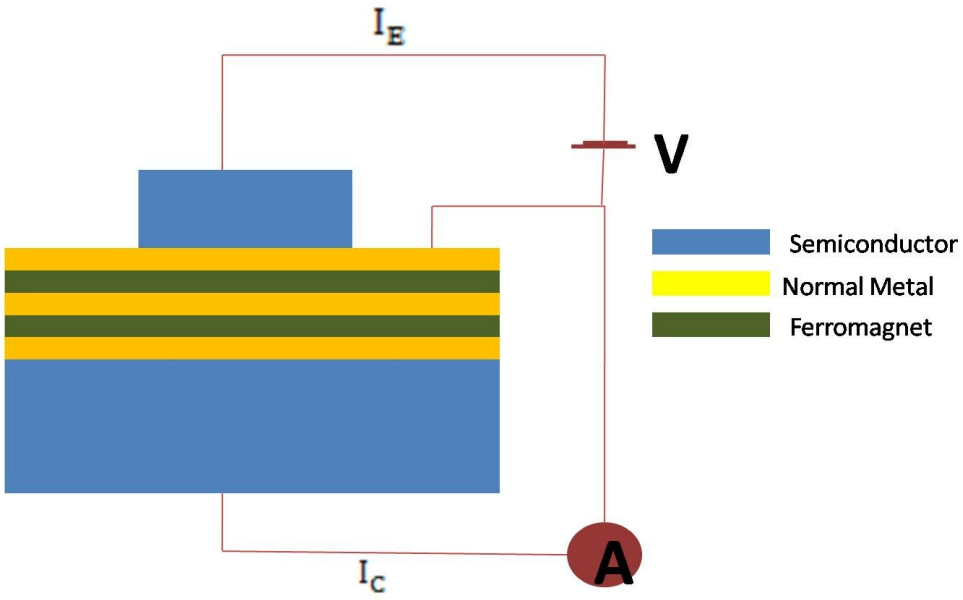


Figure 3.2.1: Basic layout of Spin Valve Transistor

SVT works because of a quantum property of electrons. It uses non-equilibrium spin dependent transport, known as hot electron. Silicon is used as semiconductor in SVT where it performs both as emitter and collector. $Ni_{80}Fe_{20}$ and Co are used as two ferromagnet layers separated by layers of Pt and Au respectively. At the semiconductor (Si) –metal (Pt) contact interface, a Schottky barrier is formed which hinders the flow of electrons from semiconductor to metal (Pt). Alternatively, a potential barrier is seen by the electrons of collector which hinders the flow of electron from semiconductor (Si) to metal (Au). Low doped Si and thin layers of Pt, Au are used to maintain a high quality of Schottky barrier with good rectifying behavior and the ionic emission domination.

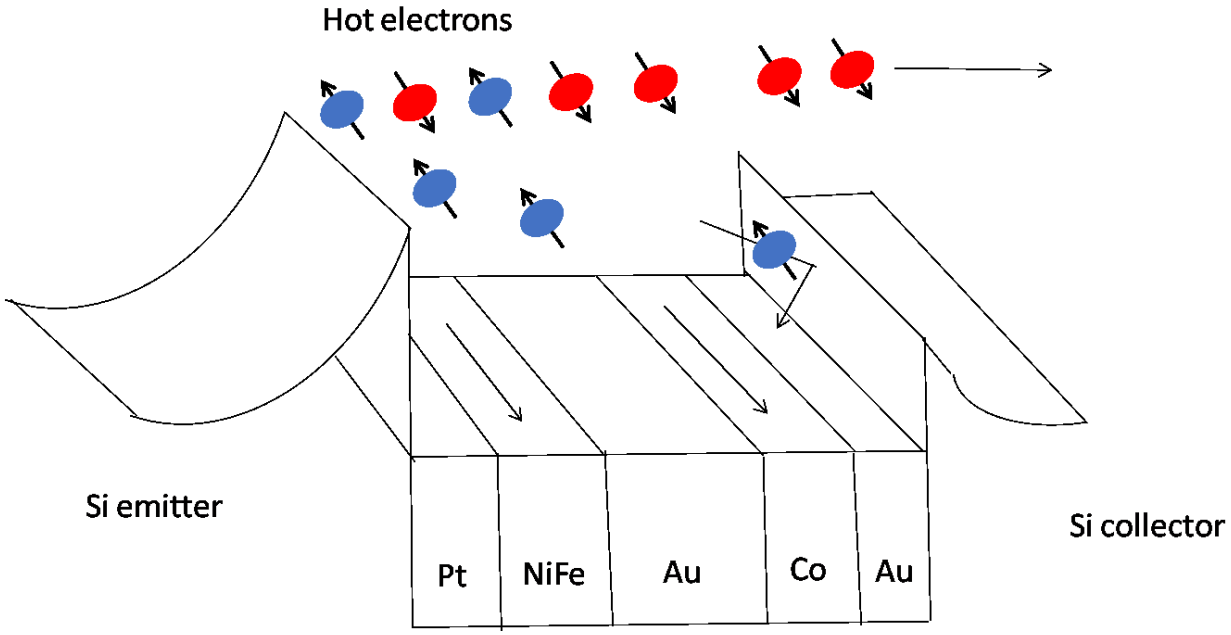


Figure 3.2.2: Schemetic layout and energy band diagram of a SVT, showing the semiconductor emitter (left) and collector (right) and the metallic base comprising a spin valve (middle).

A voltage between emitter and base results emitter current (I_E) which is applied perpendicularly to the layers of the structure. Though Fermi electrons cannot pass the Schottky barrier, non-equilibrium hot electrons enters the base. Schottky barrier height determines the energy of hot electrons. This barrier is determined by metal/semiconductor combination. Traversed electrons face inelastic and elastic scattering which changes their energy and momentum distribution. Hot electrons which overcome the barrier at collector side and match the momentum with that of one of the available states in semiconductor enter the collector. Collected electrons at collector end result collector current (I_C). Total scattering rate of hot electrons is controlled with an external applied magnetic field which moderates the relative magnetic alignment of the ferromagnet layers. Due to the difference of coercivity $Ni_{80}Fe_{20}$ acts as free layer (unpinned) and Co as fixed layer(pinned). Upon application an external magnetic field of appropriate strength, unpinned layers switch polarity, resulting two distinct states-parallel and antiparallel. If the alignment of magnetic moment of majority spin in passing current matches that of the ferromagnet layer, it passes through the layer relatively unhindered and vice versa. Hence, parallel alignment of magnetization of two ferromagnetic layers gives low resistance and antiparallel alignment gives high resistance. Parallel alignment gives largest collector current (I_C^P=11.2 nA) where antiparallel alignment gives relatively much lower (I_C^{AP} = 3.3nA) of that. Magnetic response of the SVT, magnetocurrent(MC) is defined by,

$$MC=\frac{I_C^P-I_C^{AP}}{I_C^{AP}}$$

Here, for the mentioned information relative magnetic response is MC=240%

3.3 Advantages

Initially, Spin valve transistor will use up and down spin state of electron to generate information which is more convenient than the traditional one. Traditional transistors use ON/OFF currents to generate binary bits. Secondly, spin valve transistor will use spin property for both logic and memory. At present,logic is carried out with electrons, while spin property is used for memory. Thirdly, amplification and switching property of electronicdevices can be controlled by applying external magnetic field in spin valve transistor which is more efficient than conventional transistor. Additionally, heatemission problem is much less in spin valve transistor than the traditional ones.

3.4 Application

Spin valve transistor can open the opportunity to create high sensitivity magnetic field sensors for automotive industry. Alongside this, data storage application is another one to be benefitted by spin valve transistor. A new application of this transistor can be applied in quantum computation, where, qubits are used instead of traditional computer's bits.Qubits use spin up and spin down state of electron as superpositions of zero and one. It has advantages over conventional semiconductor chips since power is not required to maintain the memory state. This may be used as amplifiers and mixers which are magnetically controlled.

3.5 Limitations of spin based devices

Though spin valve transistor creates new era of opportunity, few issues have to be taken care of. Spin property of electron is the fundamental idea of this device. Control of this spin for the long distance in the device is still a challenge. On the other hand, the spin which is injected into the semiconductor layer of the device is hard to measure. Injection and measurement of spin is comparatively difficult to master. Silicon, the semiconductor element used in the most of the spin based devices gives difficulty to control the spin. Last but not the least; interference of fields with nearest elements in the device is also a challenge to overcome.

Chapter 4

Result

4.1 Change in spin signal for different magnetization orientation

Non-local spin signal depends on gate voltage. For parallel and anti parallel magnetization alignments of gate and source non local spin signal shows different characteristics with change in gate voltage. For parallel magnetization alignments between gate and source positive non local signal is observed. For negative gate voltage (Vg=-40) higher non local signal is observed which is observed as ON state. Non-local signal decreases with increase value of Vg. For Vg>40 no non-local spin signal is observed and considered as OFF state. Change in spin signal observed for parallel magnetization is 15.7mΩ/V**.** For anti-parallel magnetiztion alingments of source and drain different scenerio is observed. For Vg=-40 negative non-local spin signal is observed which is ON state and smiliarly for Vg>40 no non local spin signal is observed which is OFF state. For anti-parallel magnetiztion change in spin signal is 22.227mΩ/V. So higher change in spin signal is observed for anti-parallel magnetization alignments of source and drain.

Spin state	**Δspin signal/ΔV_g(mΩ/V)**
Parallel	15.7
Anti parallel	22.2

Table 4.1: Change of spin signal for magnetization orientation

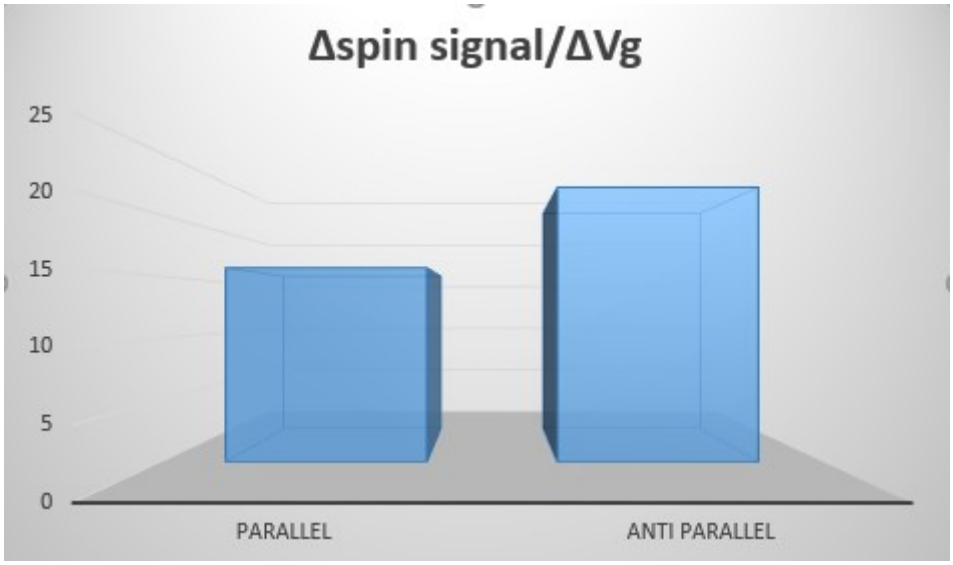


Figure 4.1: Change in spin signal due to gate voltage for parallel and anti parallel magnetization alignments of source and drain.

4.2 Change in spin signal at different temperature

In lateral spin valve (LSV) non-local resistance Rnl switches from high to low values when magnetization shifted from parallel (Rp) to anti-parallel (Rap). Spin signal is denoted by ΔRnl when ΔRnl= Rp-Rap. Change in spin signal is observed for different temperature. At first change in spin signal is observed in a graphene LSV without Mos2 at 50K and the observed result is 61.76mΩ/V. another change in spin signal is ovserved in a graphene/Mos2 LSV at 200k and the observed result is 51.62 mΩ/V. At 300k change in spin valve signal is 0.70 mΩ/V. Similiar change in spin valve signal is observed at 50K and 200K.

Temperature	**ΔRnl/ΔVg(mΩ/V)**
50K	61.76
200K	51.62

Table 4.2: Change of spin signal for differnet temperature

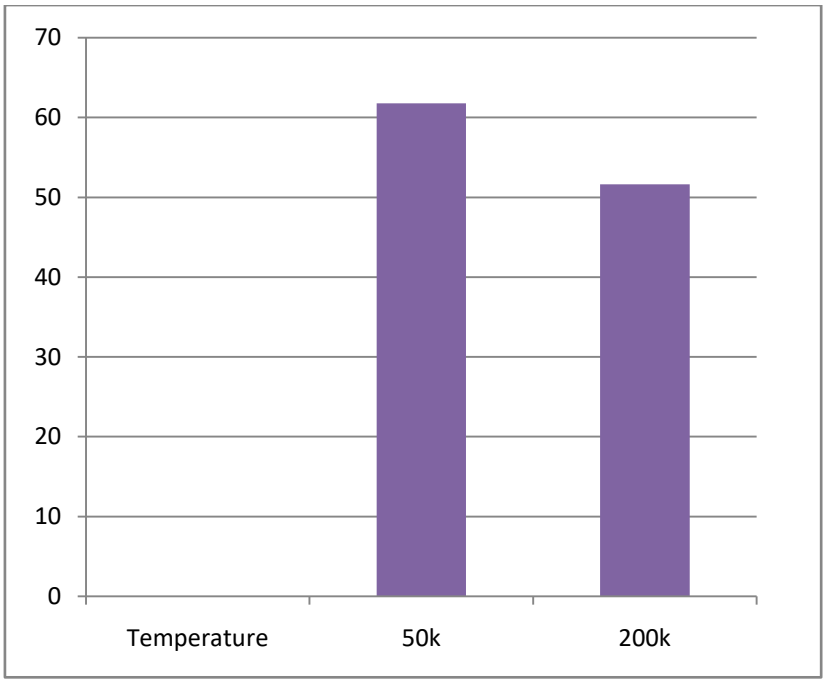


Figure 4.2: Change in spin signal at different temperature.

4.3 Magnetoresistance Ratio:

Spin Valve effect is observed by inspecting related magnetoresistance ratio (MR) of elements which is defined as,

$$\text{MR} = \frac{R(H) - R_p}{R_p}$$

Here, R(H) is the magnetic field-dependent resistance and R_p is the resistance corresponding to parallel alignment of magnetizations.

Tunnel magnetoresistance (TMR) is a magnetoresistive effect occurs in Magnetic Tunnel Juction (MTJ), where, two ferromagnets are separated by a thin layer. On the other hand, Giant Magnetorestance (GMR) occurs in multilayer device structure.

Temperature plays a significant role when it comes to variation of MR in different thermal condition. For instance, the magnitude of MR increases as the temperature is lowered down for both double and single layer graphene junctions. TMR also various for different elements along with several thermal

conditions.Hence, it can be inferred that temperature dependence has been observed in a variety of magnetic tunnel junctions.

Figure A and B show us MR and TMR of various elements respectively at 300K temperature.

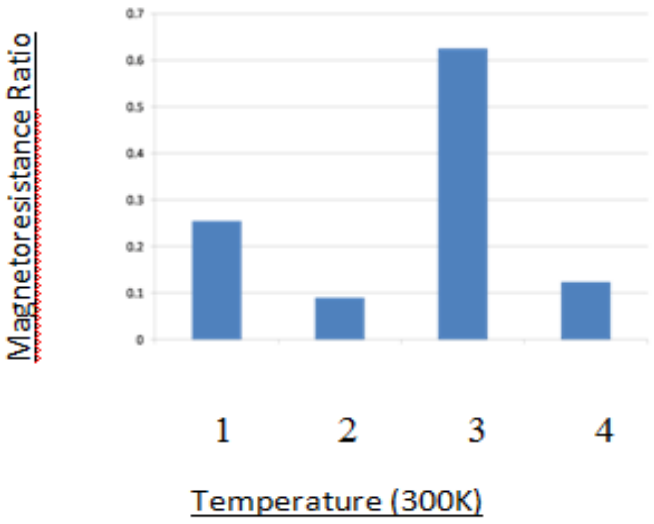


Figure 4.3.1: Magnetoresistance Ratio at 300K

Serial No.	Elements	MR(%)
1	Nife/graphene/NiFe (double layer)	25.5
2	Nife/graphene/NiFe (single layer)	9
3	NiFe/MoS_2/NiFe	62.5
4	$La_{1-x}(Sr_{1-y}Na_y)_xMnO_3$	12.4

Table 4.3.1 (Magnetoresistance Ratio at 300K)

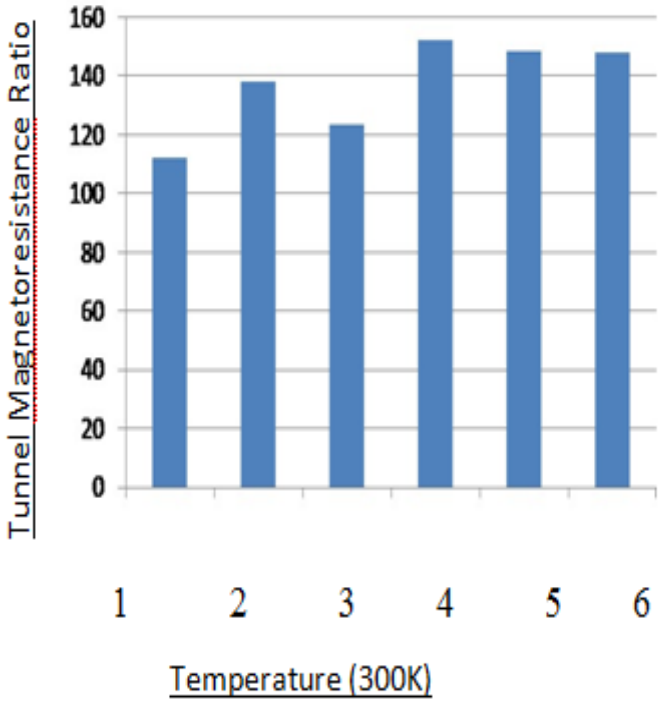


Figure 4.3.2: Tunnel Magnetoresistance Ratio at 300K

Serial No.	Element	TMR(%)
1	Co_2FeSi	112.5
2	$Fe_{1.25}Co_{1.75}Si$	138.25
3	$Fe_{1.5}Co_{1.75}Si$	123.75
4	$Fe_{1.75}Co_{1.25}Si$	152.25
5	Fe_2CoSi	148.75
6	MgO	148.25

Table 4.3.2Tunnel Magnetoresistance Ratio at 300K

Chapter 5

Conclusion

Spin valve transistor is being more popular as it is a hybrid electronic device that shows the value of functional integration of semiconductor and ferromagnetic material. The performance of this device is more energy effective. Extended improvement on this device is required to improve the magnetic sensitivity of the collector current. At this phase, it is a challenge for scientists and engineers to control all the spins of a whole circuit while it is being difficult to do it on a single transistor.

SVT explores new route of fundamental physics. Comparing to other semiconductor devices, collector current does not depend on spin independent scattering in spin valve transistor. Another feature of this study is to develop many other related devices. The study of transport of hot electrons in half-metallic ferromagnets and oxide helps to make new hybrid devices that is combination of ferromagnets and semiconductors. However, the factor is weather this technology worth the production cost and if it is affordable by using common materials.

REFERENCES

[1] Dankert, A. (2015). Spin transport in two-dimensional material heterostructures. Göteborg: Department of Microtechnology and Nanoscience, Chalmers University of Technology.

[2] Neamen, D. (2011). Semiconductor physics and devices. New York: McGraw-Hill Higher Education.

[3] Dankert, A. and Dash, S. (2017). Electrical gate control of spin current in van der Waals heterostructures at room temperature.Nature Communications, 8, p.16093.

[4] Iqbal, M., Iqbal, M., Lee, J., Kim, Y., Chun, S. and Eom, J. (2013). Spin valve effect of NiFe/graphene/NiFe junctions. Nano Research, 6(5), pp.373-380.

[5] Yan, W., Txoperena, O., Llopis, R., Dery, H., Hueso, L. and Casanova, F. (2016).A two-dimensional spin field-effect switch. Nature Communications, 7, p.13372.

[6] Jansen, R. (2003). The spin-valve transistor: a review and outlook. Journal of Physics D: Applied Physics, 36(19), pp.R289-R308

[7] Anil Kumar, P. and Lodder, J. (2000). The Spin-Valve Transistor - a New Magnetoelectronic Device. Acta Physica Polonica A, 97(1), pp.111-118.

[8] Danowitz, A., Kelley, K., Mao, J., Stevenson, J. and Horowitz, M. (2012). CPU DB: Recording Microprocessor History. Queue, 10(4), p.10.

[9] Danowitz, A., Kelley, K., Mao, J., Stevenson, J. and Horowitz, M. (2012). CPU DB: Recording

Microprocessor History. Queue, 10(4), p.10.