Graphene as a replacement for Si in nano-electronics

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DECLARATION

I hereby declare that this thesis or any part of the thesis has not been submitted elsewhere for any degree or any award.

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I would like to express my sincere and earnest gratitude to everyone who has made this thesis work possible. First of all, I would like to thank my supervisor Professor Dr. Mumit Khan without whose wise supervision and proper guidance this thesis would not be possible. With his profound knowledge and experience he has helped me throughout to achieve my thesis goal. Secondly, my thankfulness goes to my respectable teachers who always have appreciated, encouraged, helped and supported me with their knowledge. After that I would like to convey my gratefulness to my friends who have supported me with their sincere inspirations. Last but not the least I would like to thank my parents genuinely who have always stood beside me and believed in me with their constant support and encouragement to show me the right path.

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Abstract:

In this paper, device manufacturing as a whole has been explored to discover whether graphene could be a prospective material for device fabrication or not. As a part of this exploration, the current device manufacturing process and its limitations have been examined. According to Moore's law, the number of transistors per square inch on integrated circuits had doubled ever year since the invention of integrated circuit and is expected to continue so for future. To sustain Moore's law in semiconductor manufacturing industry, the size of devices have to be smaller and smaller in the near future. The use of Si in device manufacturing is going through its fundamental limitations including scaling limitation and mobility issue. Research has shown that when Si is cut into very narrow ribbons or layers, the mobility decreases significantly and at the same time silicon's characteristics vary considerably with the changes in temperature. Thus at this era of smaller and smarter devices, the researchers have started their venture of searching for an alternative for Si in nanoelectronics. If not an alternative then at least as a prospective material for future nanoelectronics, graphene has attracted the attention of many due to its superior mobility, excellent thermal conductivity, availability and low cost. Graphene being regarded as a "miracle material" has proved itself to be a probable replacement for Si in nano-scale device manufacturing as being cut into nano-meter size layers, the mobility remains high even at room temperature.

An absense of a proper bandgap in graphene making it impossible to turn the conduction off in graphene device, puts graphene-based device manufacturing under scrutiny.The research does not stop here as graphene has already exhibited its other outstanding characteristics which still open up the chances for graphene's use as an epitaxial layer on other semiconducting substrates in order to fabricate devices. Epitaxial layer on SiC/SiO_2 substrates is one of these prospective methods. However the limitations given, the approach towards fabricating all-graphene devices is on its way and thus the need of engineering a bandgap in graphene arises urgently. The matter of anticipation is that some prospective methods have been proposed by a lot of researchers around the world to obtain or induce a bandgap in graphene. Some of the approaches include Scanning Tunnelling Probe Microscope (STM) lithography, using Graphene Oxide (GO) sheets to bridge the gap between two epitaxial graphene layers, opening a tunable bandgap in Bi-layer graphene by doping the substrate electrically and so on. If an entire device fabrication process can be established which include obtaining graphene samples, attaining all-graphene layers and etching processes using different effective lithographic techniques, then the day is not far away when the "graphene-dream" would come into life with graphene reigning over the semiconductor fabrication industry.

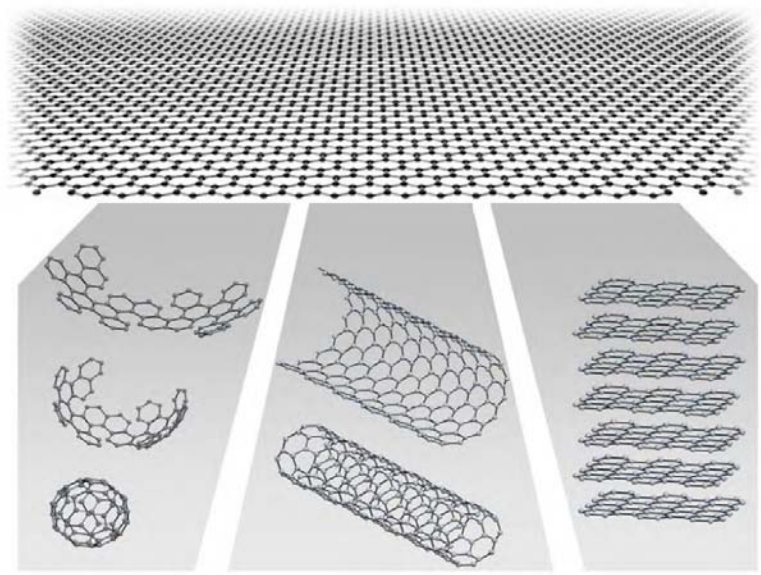
1.Introduction:

So far in semiconductor manufacturing industry, Si has been a reliable candidate. But in recent times, people have been looking for an alternative material for nano-scale device manufacturing because of some unavoidable limitations of Si in nano-electronics. These limits include the leakage of tunneling currents in very small-size Si devices, significant decrease in the mobility of Si while cutting it into nano-scale range and last but not the least temperature dependency of Si in device manufacturing. To emphasize the last one, it has been observed in some experiments that contamination occurs during high temperature behavior of Si [1]. As a result, the researchers and manufacturers had started their journey to search for an effective and dependable alternative that will outperform Si in nanoelectronics. Thus the discovery of a "wonder material" has led a new path towards nanoelectronics industry.

If we look back to the fields of solid-state physics and Semiconductor manufacturing industry, it is revealed that the exploration of carbon allotropes has always been attractive as well as influential. In 1993, after the discovery of carbon nanotubes (CNTs), numerous scientists and researchers had predicted that CNTs would be able to take over Si soon [16]. But CNT technology could not replace the well-established silicon technology because of some inevitable limitations. One major challenge with CNT is applying electrical contacts to the nanotubes on an industrial scale. Later in 2004, A research team including Andre Geim and Konstantin Novoselov established that single layers from graphite can be isolated which brought them the Nobel Prize for Physics in 2010. However graphene was treated as "the next big thing" [17] even before it's pioneers were awarded the Nobel Prize last year. Compared to CNTs, graphene, though being a carbon nano-particle, often has an area of several thousand μm^2. One key advantage of Graphene over CNTs in electronics exists in its planar 2D structure that allows circuit-design with standard lithography techniques [18].Thus the ability to pattern and contact graphene on an industrial scale paves a way to carbon-based electronics. Graphene nanostructures display stability even in nanometer size. Most importantly, graphene holds attractive electrical properties that can establish carbon based electronics far more superior to conventional silicon technology.

A matter of anticipation is that, the discovery of graphene has forced many of the researchers to start looking at Graphene as a prospective candidate for device manufacturing at the same time as a replacement for Si in device manufacturing industry. The reasons behind it is the ultra high mobility of Graphene, availability of Carbon and its allotropes in plenty, amazing high temperature behavior and low cost. Graphene is a flat monolayer of carbon atoms tightly packed into a two dimensional (2D) honeycomb lattice. It is actually a semi-metal having zero band-gap and has exhibited excellent electronic properties with carrier mobility between 3000 to 27000 cm^2/Vs. Graphene exhibits mobility >15000

cm^2/Vs at room temperature. Most importantly, Graphene has exhibited mobility 10 times higher than Si which has attracted many researchers to focus on Graphene as a successful replacement for Si in device manufacturing. Furthermore another mentionable and extraordinary feature of graphene is that its μ remains high even at the highest electric-field induced concentrations and is little affected by chemical doping[2]. These distinguished properties make a promising new category of carbon-based transistors and integrated circuits with performance superior to silicon, germanium and III-V compound semiconductors.



<u>Fig1:</u> All graphicitic forms. 2D Graphene that can either be wrapped up into 0D buckyballs or can be rolled into nanotubes. Also can be stacked to form 3D graphite[2].

In this paper, the main focus will be to look at graphene as a prospective candidate for future nano-scale devices, the methodology and fabrication, the challenges of graphene in device manufacturing and thus the ways to overcome challenges. The methodology discussed here includes solution processing of large-scale graphene, the epitaxial -graphene/graphene oxide junction. The latter one was used to fabricate all graphene devices. This integrated graphene technology has actually been proved to be a successful one which will lead to graphene-based nano-electronics in the near future.

Apart from the integrated grapheme technology, another aim of this paper is to explore an effective lithographic process that can be used to fabricate Graphene nanoribbons (GNRs) of few nanometers in width as well as to obtain complex graphene nano-architecture. Scanning Tunneling microscope (STM) lithography is such a process which has a 20 years old history in graphite surface modification.

Though graphene exhibits unique and distinct characteristics, due to some major limitations graphene based nanotechnology is still under consideration and has not flourished properly. Besides looking at fabrication and device manufacturing, this paper also looks at the limitations and tries to explore the ways to overcome those. The main limitation of graphene is an absence of bandgap. Thus inspite of having a high carrier mobility and significant current characteristics, the conduction in graphene devices cannot be switched off due to this absence of a bandgap. Therefore, graphene devices are not capable of being used as switching transistors which clearly indicates that large area graphene is yet to compete with the existing powerful Si technology in CMOS VLSI due to lack of considerable bandgap [20]. However, a matter of anticipation is that recent researches are focusing on switching or on/off characteristics of graphene devices, which can lead to a graphene-based semiconductor industry.

Some potential approaches of attaining a bandgap in graphene are discussed and demonstrated in this paper. One of the prospective ways to open a bandgap in graphene is patterning the graphene sheets into narrow ribbons [10]. STM lithography is a process through which a band gap of about 0.5eV can be achieved; turning the metallic graphene into a semiconducting material. The opening of an energy band gap can be possible if it is patterned into a narrow ribbon and the carriers can be confined to a quasi one-dimensional (1D) system. This energy gap largely depends on the width and crystallographic orientation of the graphene nanoribbons (GNRs) [19].

Considering the extraordinary characteristics of graphene and its advantageous properties, it can be assumed that soon graphene would reign over the electronics industry. Since graphene’s properties were exposed, numerous scientists and researchers have started working on projects relevant to graphene. In a BBC site, it has been stated that many people believe that graphene could bring the end for silicon and change the future of computers and other devices magically in the near future.

2.Background Research:

Papers on the use of Si in device manufacturing:

1.A Neutron Activation Analysis Study of the Sources of Transition Group Metal Contamination in the Silicon Device Manufacturing Process, P. F. Schmidt and C. W. Pearce, J. Electrochem. Soc. 128, 630 (1981), DOI:10.1149/1.2127472

This particular paper looks at some of the limitations of using Si in device manufacturing industry. In my paper, I'll look into this to explore the contamination occurred during high temperature behavior of Si. Thus comparison between the thermal conductivity of graphene and Si can be done thoroughly and as a result it will definitely give way to the researchers to think about graphene as a successful replacement for Si in nanoelectronics.

2.Frank, D.J.; Dennard, R.H.; Nowak, E.; Solomon, P.M.; Taur, Y.; Hon-Sum Philip Wong; *Device scaling limits of Si MOSFETs and their application dependencies, Proceedings of the IEEE* , vol.89, no.3, pp.259-288,Mar2001doi:10.1109/5.915374

The above cited paper focuses on the scaling limitations of Si CMOS technology. These scaling limits include leakage in tunneling current in Si MOSFETs and thermally generated subthresold currents.

Papers on high carrier mobility of graphene:

1. *The rise of graphene*. A. K. Geim S. Novoselov. Nature Materials 6, 183 - 191 (2007) doi:10.1038/nmat1849

This paper gives us a brief and precise idea about the potentials of Graphene and the future prospect of it in device manufacturing applications. Starting from the brief history of Graphene to its being a promising candidate for nano-electronics applications, the paper provides a very wide perspective to make us realize how Graphene can be an exceptionally superior choice as a candidate material to take over Si in device manufacturing industry.

2. *Current status of graphene transistors.* M.C. Lemme, 2009, Solid State Phenomena, 156-158, 499.

This paper focuses on the advantages of Graphene over CNTs. Some of the unique and promising properties of Graphene demonstrated in this paper are high carrier mobilities, high current carrying

capability exceeding $1X10^8$ A/cm^2, high thermal conductivity, high transparency and mechanical stability. In addition to that, this particular paper illustrates the three established fabrication methods for graphene; these are- Mechanical exfoliation, epitaxial growth from silicon carbide (SiC) substrates and chemical vapor deposition of hydrocarbons on reactive nickel or transition-metal-carbide surfaces. Moreover, this paper proposes a method that can overcome the limitation of Graphene being a zero band-gap material. The method includes creating a band gap in Graphene by cutting it into narrow ribbons of less than a few tens of nanometers.

3. *Mobility in graphene double gate field effect transistors.* M.C. Lemme, T.J. Echtermeyer, M. Baus, B.N. Szafranek, J. Bolten, M. Schmidt, T. Wahlbrink, H.Kurz, *Solid-State Electronics* Volume 52, Issue 4, April 2008, 514-518.

Carrier mobilities in single and double-gated graphene field effect transistors are compared in this paper. This research shows an astonishing result that reveals that even in double-gated graphene FETs; the carrier mobility exceeds the universal mobility of silicon. In addition to that, reported mobilities for ultra thin body silicon-on-insulator MOSFETs cannot compete with the graphene FET values which can give way to graphene-based nanoelectronics in near future.

Papers on epitaxial graphene:

1. *Ultrathin Epitaxial Graphite: 2D Electron Gas Properties and a Route toward Graphene -based Nanoelectronics.*Claire Berger, Zhimin Song, Tianbo Li,, Xuebin Li, Asmerom Y.

This paper focuses on the production of ultrathin epitaxial graphite films which exhibit remarkable 2D electron gas behavior. The films composed of typically 3 graphene sheets were grown by thermal decomposition on the surface of 6H-SiC. In addition to that, some of the key factors about this integrated graphene technology has been revealed in the paper which includes the potential of electronic device applications based on nano-patterned epitaxial graphene (NPEG).

Papers on thermal conductivity of graphene:

1. *Superior Thermal Conductivity of Single-Layer Graphene.* Alexander A. Balandin, Suchismita Ghosh, Wenzhong Bao, Irene Calizo, Desalegne Teweldebrhan, Feng Miao, Chun Ning Lau *Nano Letters* 2008 *8* (3), 902-907.

In this paper, the main focus is to trace the extremely high value of the thermal conductivity of graphene that makes it a reliable and promising material for future electronic applications. The outstanding thermal conductivity of graphene can also substitute carbon nanotubes in future nanoelectronics and device manufacturing industry. In addition to that, I will look at this paper to explore whether graphene can also outperform Si in nanoelectronics when it comes to thermal conductivity and performance.

Papers on process, methodology and device fabrication with graphene:

1. *Epitaxial graphene transistors on SiC substrates.* Jakub Kedzierski, Pei-Lan Hsu, Paul Healey, Peter Wyatt, Craig Keast, Mike Sprinkle, Claire Berger, and Walt de Heer. Georgia Institute of Technology, (1-25).

This paper looks straight into the fabrication of transistors using epitaxial graphene on SiC. In addition to that this paper illustrates the limitations of micron-scale devices fabricated using this method and a methodological comparison between Carbon faced and Silicon faced devices.

2. *Atomic-layer-deposited nanostructures for graphene-based nanoelectronics*. Y. Xuan, Y. Q. Wu, T. Shen, M. Qi, M. A. Capano, J. A. Cooper, and P. D. Ye, Appl. Phys. Lett. **92**, 013101 (2008); doi:10.1063/1.2828338 (*3 pages*).

This paper illustrates how insulating nanoribbons generated using atomic layer deposition process could be used as a hard mask for dry etching to create graphene nanoribbons. Looking at this paper gives an insight to the process of constructing an ideal building block for top-gate graphene transistors.

3. High-throughput solution processing *of large-scale graphene.* Vincent c. Tung, Matthew J. Allen, Yang Yang, and Richard B. Kaner,*Nano Letters 2008*,25-29.

This paper demonstrates a versatile yet effective as well as achievable solution-based process for producing large-scale single-layer chemically converted graphene over the entire area of a Silicon/SiO_2 wafer.

4. Xiaosong Wu, Mike Sprinkle, Xuebin Li, Fan Ming, Claire Berger and Walt A. de Heer. "The epitaxial-graphene/graphene-oxide junction, an essential step towards epitaxial graphene electronics." *Phys. Rev. Lett.* Vol.101, 2008.

This particular paper deals with the approach to fabricate all-graphene devices which means instead of using any other material as the substrate, only graphene is used. Graphene oxide (GO) flakes are deposited to bridge the gap between two epitaxial graphene electrodes which paves a way towards producing all-graphene devices. At the graphene/GO junction, a presence of Schottky Barrier (SB) can be identified which signifies the existence of a band-gap in GO. The barrier height found here is almost upto 0.7eV. Not only that but also this band-gap is tunable which can be reduced after thermal annealing. So by changing the level of oxidation, the band-gap can be tuned. Lower limit of GO mobility was measured as 850 cm^2/Vs which is easily compatible with Si.

Papers on lithographic processes in graphene-based devices:

1. Levente Tapasztó, Gergely Dobrik, Philippe Lambin & László P. Biró. "Tailoring the atomic structure of graphene nanoribbons by scanning tunnelling microscope lithography." *Nature Nanotechnology*.vol.3, pp.397-401,June2008.

From this paper, we get to know about a prospective and quite useful lithographic process through which graphene devices can be patterned in such a way that results in opening of "confinement gaps" up to 0.5eV. Moreover, this method enables room-temperature operation of graphene nanoribbon-based devices. For room-temperature operation, GNRs of just a few nm widths are required to obtain energy gaps as energy bandgap is inversely proportional with ribbon width. But, with the traditional e-beam lithography, this is not possible and it gives rise to a scaling limitation. Scanning probe microscope lithographic process can provide a solution to this problem. Scanning Tunneling Microscopy (STM) method is capable of "atomic-resolution imaging" with the ability to locally modify the surface of the samples.

2. Péter Nemes-Incze, Gábor Magda, Katalin Kamarás and László Péter Biró. Crystallographically Selective Nanopatterning of Graphene on SiO_2." *Nanores.* Vol. 3, pp. 110-116, December2009.

This paper demonstrates how graphene ribbon with zigzag edges can be obtained through an "anisotropic, dry etching" process. A controllable patterning anisotropic process has been demonstrated here. The advantage of this method is that the "crystallographic orientation dependent etching of graphite by metal nanoparticles" can be implemented on graphene surface instead of implementing on a conducting surface. The patterning experiments were done with micromechanical cleavage to obtain graphene samples. Then single crystal silicon wafers having a 90-nm thick SiO_2 top layer. Once the graphene samples were prepared, those were exposed to an oxygen-nitrogen atmosphere at 500^0c in the Electronic Supplementary material (ESM). This treatment produces circular pits on the graphene surface shown in AFM image in Fig-(2a). Then the process was followed by a subsequent etching step that consists of annealing the sample under a continuous flow of Ar gas at 700^0c. After this step, the existing circular pits continued to grow in size. Hence the hexagonal etch pits are derived (Fig- 2b).

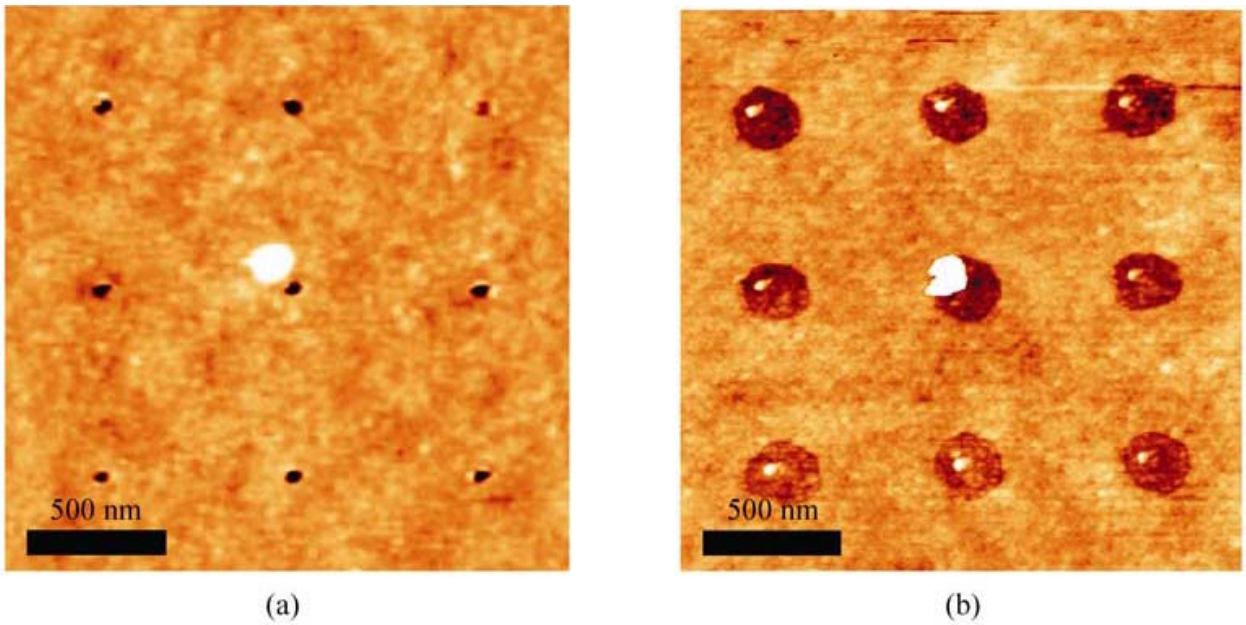


Fig-2: (a) The result fo AFM indentation of a 3 × 3 matrix of holes in graphene. (b) AFM micrograph of the hexagonal holes grown from the defects induced by indentation. Protrusions inside the hexagons are remnants of the AFM indentation process [13]

Thus, it has been proposed in the paper that the “main mechanism” used here to form hexagonal pits is the “carbothermal reduction” of the substrate SiO2 by the carbon in the graphene edges:

$$SiO_2 + C \xrightarrow{700\ ^\circ C} SiO(g) + CO(g)$$

Overall this paper proposes that this carbothermal process demonstrated here should be coupled with other lithographic techniques such as electron beam lithography or AFM tips to produce desired graphene nanostructures with zigzag orientation of the edges. Another positive aspect of this process is that after the etching treatment the high crystallinity of graphene is preserved and through this technique, very narrow graphene ribbons (e.g. 35nm or below) can be achieved.

3.Methodology:

Until now, numerous methods and fabrication processes have been proposed and adopted by different researchers and manufacturers.

When it comes to device manufacturing with graphene, two major steps have to be taken by the manufacturers. These are stated below:

1. **To generate Graphene in large scale to be used as a "raw-material" for making devices**

Producing graphene in large quantities is the first and foremost step towards graphene-based electronics. Some established approaches for producing graphene sheets include mechanical cleavage of graphite, epitaxial growth, bottom-up organic synthesis and chemical exfoliation of graphite [19].
As graphite is available in plenty as well as quite inexpensive, large-scale production from graphite or graphitic forms has captured the attention of many researchers. However direct exfoliation of graphite has been a challenge which has given way to the hydrophilic methods that is discussed below. In this method graphite- oxide is used instead of graphite. To demonstrate, individual and stable graphene oxide sheets are exfoliated from graphite-oxide. Later through "deoxygenation via chemical reduction" [19] conductive graphene sheets are achieved from insulating graphene oxide.

2. **Ultimate device manufacturing with Graphene**

In this paper, ultimate device manufacturing with graphene can be done in two ways. The first one is producing epitaxial layer on SiC/SiO_2 substrates. The other one is fabricating "all-graphene" devices. Fabricating "all-graphene" devices is based on Epitaxial graphene/Graphene-oxide junction. Both the processes have been illustrated in the next section.

3.1.Process:

3.1a Producing large scale graphene

Though it is difficult to produce single-layer samples of graphene, but a solution-based process for large scale production of single-layer chemically converted graphene over the entire area of a silicon/SiO_2 wafer has drawn the attention of many researchers. This versatile process is known as "High-throughput solution processing of large-scale graphene" and has been achieved by dispersing graphite oxide paper in pure hydrazine. The chemically converted graphene sheets that were produced have the largest area reported till now (up to 20X40μm). Conventional photolithography has been used to fabricate field-effect devices from these chemically reduced graphene sheets. In these experiments, currents higher than three orders of magnitude than previously reported values for chemically produced graphene have been achieved (Tung 25). Successful dispersion of graphene enables the use of low-cost solution processing techniques to fabricate various useful graphene-based materials [19].

3.1b Integrated Graphene technology:

Epitaxial graphene on SiC substrates

[6] demonstrates the systematic evaluation of arrays of a large number of transistors entirely produced using standard microelectronics methods. This method focuses on creating a substrate of graphene on which an electronic device technology can be based. In this method the graphitic films on SiC substrates were prepared by solid-state decomposition of single crystal 4H-SiC (001) in vacuum. After that, before the integration, G/SiC chips were characterized using optical and AFM measurements. Once the characterization was done, G/SiC chips were mounted on 150-nm silicon carrier wafers using epoxy bonding. Then firstly, alignment marks were defined with standard g-line lithography and etched into the G/SiC with a Cl_2/He plasma etch. Following the alignment mark etch, the resist was stripped in 80®c sulfuric acid. After that the active MEG layer was patterned using a low energy O_2 plasma etch. The source/drain layer was deposited directly on the MEG layer and it consisted of 2nm Ti and 20 nm of Pt. Next by using thermal evaporation, a 40 nm HfO_2 layer was deposited over the entire chip (Heer 2).

This whole process was actually used to generate multilayer epitaxial graphene (MEG) on SiC substrate. Through this process hundreds of carbon based devices have been successfully fabricated.

Fabricating "all- graphene" devices

The method of fabricating all graphene devices is opening a new horizon for graphene based nano-electronics. Through this method, Graphene Oxide (GO) flakes have been deposited to bridge the gap between two epitaxial graphene electrodes [11]. The advantages of this method include producing multi-layered epitaxial graphene and converting the semi-metal into a semiconductor. Compared to single-layer epitaxial graphene (EG), multilayer EG definitely has some virtues that makes multilayered EG superior to single-layer EG. To emphasize, in multilayer EG,

1. The patterned structures are more robust
2. The interior layers are protected from the environment and surrounding
3. The layered structure allows intercalation[11]

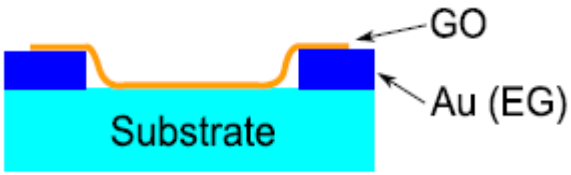


Fig3: A side view of the layout of GO devices

To carry on this process, at first, suspensions of ~1µm GO flakes were obtained. To deposit these flakes over pairs of Au electrodes patterned on an oxidized Si wafer, or over patterned EG electrodes, an ac dielectrophoresis method was used. The electrodes were separated by 400,500 or 1400nm gaps. During the process it was observed that an ac voltage of 2-3 volt peak-to-peak at 20-50 kHz produced optimal results. Finally samples were heated to 100^{o}C for 30 minutes that helped driving off absorbed water vapor. In some previous methods the measured thickness of a single GO layer on SiO_2 ranges from 0.9

to 1.5nm whereas it has been recorded as 1.5 to 2.2nm on EG layers .Fig. 3a and 3b exhibit images of flakes over pairs of electrodes. Fig. 2b shows a single layer GO flake deposited over an EG gap.

Observations:

It has been observed that single layers are usually flat and free of wrinkles. In addition to that, the thickness that has been measured for a single GO layer on SiO_2 ranges from 0.9-1.5nm.

On the other hand, some wrinkles like bright lines [fig-4b] can be seen in C-face EG. On the contrary with single layer flakes, the bilayer ones are insulating for bias voltages up to 20V.

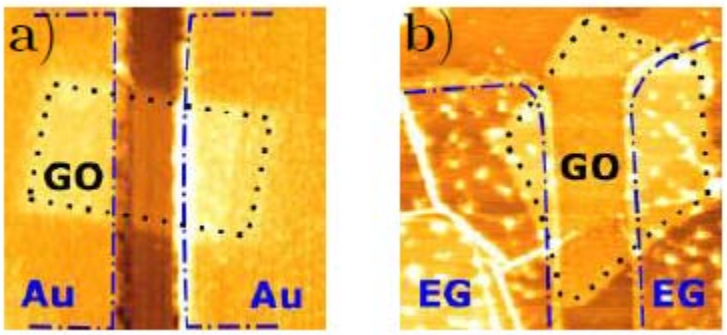


Fig4: a) a bilayer rectangular GO flake (outlined by a black dotted line) over a 400nm Au gap. Blue dash dot lines represent Au pads. b) A pentagonal GO flake bridges 2 EG electrodes[11].

This observation indicates that the electronic properties of bilayer GO differ drastically from those of single layer GO.

In a nutshell, through this method, the researchers have been able to propose an integrated model to produce all-graphene metal-semiconductor-metal devices. From the I-V characteristics of this device, a Schottky barrier height of 0.7eV has been encountered, which is a sign of a band gap of at least this value in GO. The mobility of GO that has been observed is 850cm^2/Vs which falls under the range suitable for room temperature electronics. Another advantage of this process is

that in this method, the bandgap can be tuned by changing the degree of oxidation through both thermal curing and e-beam irradiation.

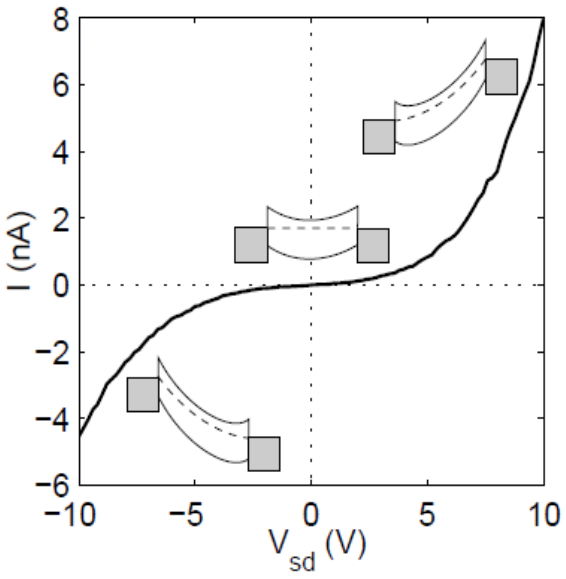


Fig5: I-V characteristics of an 800nm device. The asymmetry reflects dissimilarities of the two junctions[11]

In this process, both patterned and unpatterned EG chips were patterned. Unpatterned EG chips were oxidized by Hummers method. Likewise several ribbons were patterned on similarly grown EG chip. Rectangular windows over the central portions of the ribbons were obtained through spinning hydrogen silsequioxane on the sample and e-beam patterning. Afterward the sample was oxidized. The resultant EG/GO metal-semiconductor-metal device is completely off, even at bias voltages up to 60 , suggesting a large SB height. After e-beam contact, SBs were found to be $\leq$ 0.5eV. Thus e-beam treatment can be used to locally adjust the band gap.Thermal oxygen desorption can also be used in this process to further tune the band structure as mentioned before.

3.2 Simulation results and discussions:

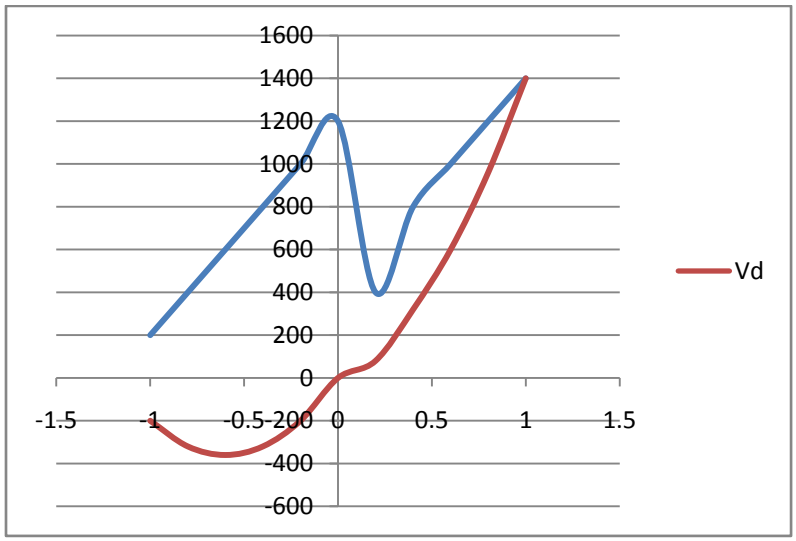


Fig-6: Plotting the equation, $V_d = \mu E$, where $V_{d=}$ drift velocity, μ= carrier mobility, E=Electric-field.

Graph Discussion:

Due to having superior thermal conductivity, the drift velocity of carriers (V_D) in a Graphene atom is faster than that of other traditional semiconducting materials such as Si. This graph shows the drift velocity (the red curve) of graphene at different mobility (values on the Y-axis) and electric field (X-axis) in Graphene. Thus high electron mobility results in higher conductivity in Graphene.

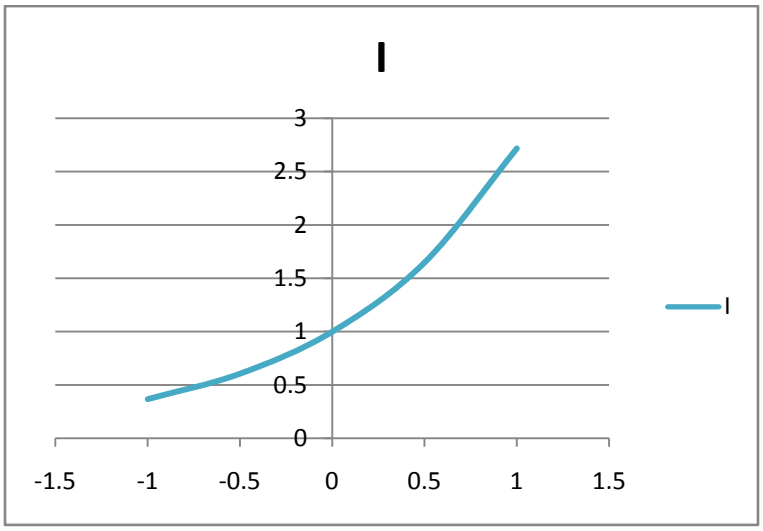


Fig-7: I-V characteristics of graphene devices

Graph discussion:

The I-V characteristics curve of graphene fits into the I-V characteristics of a semiconductor. This graph has relevance with device I-V characteristics curve. So graphene can definitely be used in device manufacturing industry as desired device-current values can be attained from expected voltage values. It is important to note that higher mobility in graphene results in comparatively higher currents.

3.3Limitations:

The main limitation of using graphene in electronics is that graphene does not have any energy band gap. Due to the absence of band gaps in graphene, the micron- scale devices have large leakage currents. Though being a zero band-gap semimetal has its own advantage of controlling the conduction of graphene with the use of a gate, but at the same time due to the same reason it becomes impossible to turn the conduction “off” below a certain limit. As seen in Fig-5, it is difficult to achieve a minimum threshold or off current which brings the issue of switching in a graphene device. Thus, the question of graphene as switching devices arises with this on/off issue.

3.3 Applications: Graphene in nano-electronics industry:

One of the prospective applications of Graphene has been that as a promising gas-sensing material. Because of its exceptional mechanical, thermal and electrical properties, graphene has attracted a lot of researchers so far. In [15], some effective and realistic ways to obtain GO have been explained. In addition to that, the use of GO in gas-sensing has been demonstrated. A potentially cost-effective method for mass-producing graphene-based devices is to produce chemically modified graphene oxide first. And after that, through chemical reduction, graphene can be obtained from GO. Though GO is electrically insulating, it can turn to be conductive if exposed to reducing agents such as hydrazine, $NaBH_4$. Among various reduction techniques, low-temperature annealing reduction of GO has been reported recently.

Hydrazine-reduced GO has performed brilliantly as gas detectors. It has been able to detect acetone, warfare agents as well as explosive agents. It has been proved to be superior compared to that based on CNTs as these graphene-based sensors can work with greatly reduced noise levels.

4.Technology Discussions:

Although being a promising candidate, graphene would take some more time to reign over the device manufacturing industry as it has to be free of its major and obstructing limitations. As discussed previously, graphene acts as a semi-metal with excellent carrier mobility. But the main limitation of using graphene in electronics is that graphene does not have any energy band gap. Due to this absence, it is quite impossible to turn the conduction below a certain level. As a result, graphene devices are not suitable as switching transistors which is a turn-off for promising graphene-based semiconductor manufacturing industry. To work with this limitation, handful of approaches have been proposed so far. Among these approaches and methods, some have drawn attention of the researchers and manufacturers as being promising and feasible ones. Let us have a look at the approaches once.

Although the fundamental challenge with graphene technology is the lack of a band-gap, and thus an inability to turn off conduction below a certain level, some solutions to these problems exist. First of all, the methods of inducing a band-gap with nanopatterning, again inducing vertical electric field, or uniaxial stress, all these have been demonstrated in some researches. A potential method of creating a band gap in graphene is to cut it into narrow ribbons of less than a few tens of nanometers (graphene nanoribbons, GNRs) (Lemme 5). And this can be achieved through an effective lithographic process.

A prospective and useful method to obtain a band-gap in graphene is *Tailoring the atomic structure of graphene nanoribbons by scanning tunneling microscope lithography* [10]. In this method, cutting of GNRs was carried out by applying a constant bias potential and simultaneously moving the Scanning Tunnelling Microscope (STM) tip with constant velocity in order to etch the desired geometry fitted to the crystallographic structure[10]. The optimal lithographic parameters for this method have been observed as below:

Bias potential= 2.4V, tip velocity= 2.0 nms^{-1}. Under this optimal condition, it has been possible to cut GNRs with regular edges suitable for the reproducibility of GNR-based devices.

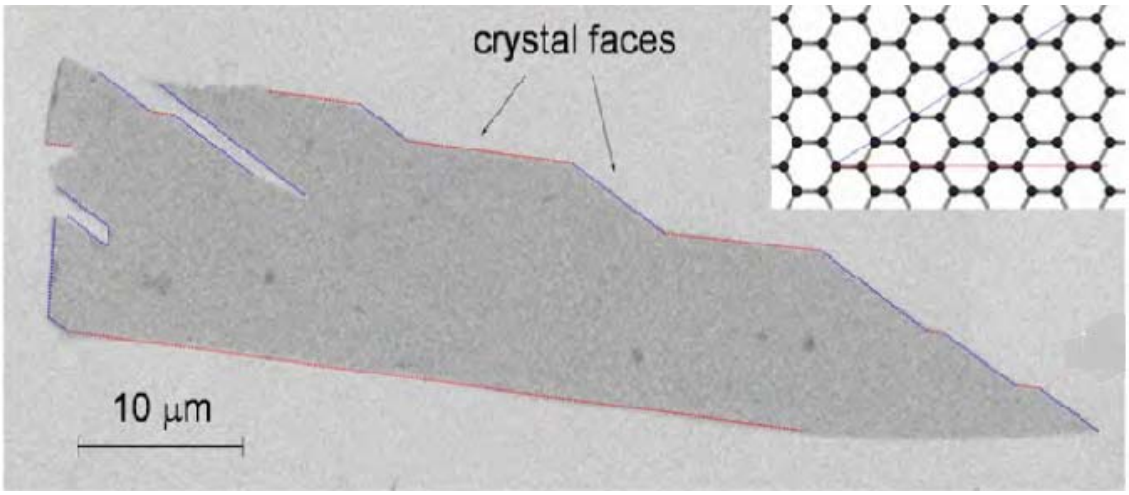


Fig8. Scanning-electron micrograph of a relatively large graphene crystal, which shows that most of the crystal's faces are zigzag and armchair edges as indicated by blue and red lines[2]

The positive aspects of the above-discussed STM lithographic method include:

1. Tailoring more complex nano-architectures
2. Giving rise to metal-semiconductor molecular junction
3. Atomically flat and defect-free structure can be obtained
4. Downscaling of the GNRs is possible during the etching process
5. Most importantly, through this method an energy gap of about **0.5 eV** can be opened in GNR. The E_g is comparable to that of Ge(E_g=0.67eV); turning the metallic GNRs into semiconducting ones.

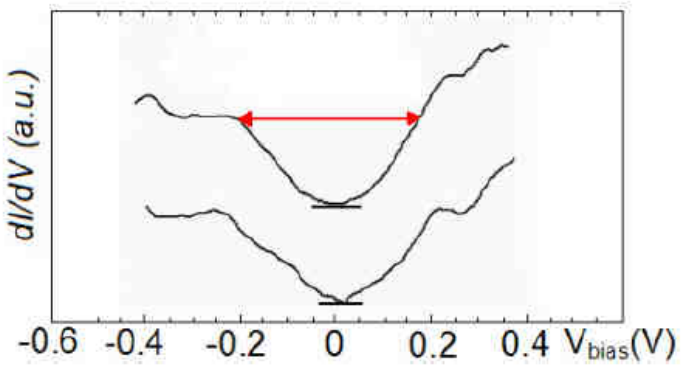
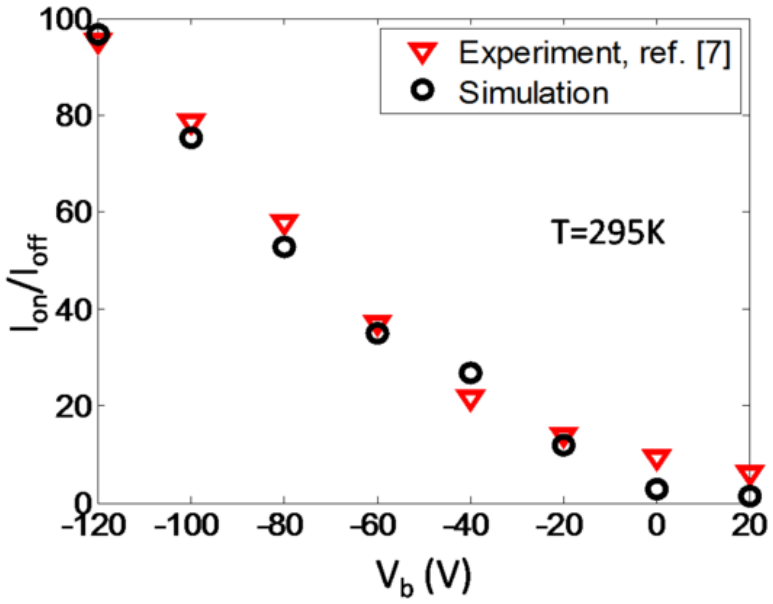


Fig9: STS spectra of a narrow ribbon revealing an energy gap of about 0.5 eV. (fig is taken from ref.10.)

In brief, using this lithographic process, it has been possible to etch semiconducting ribbons from graphene with predetermined energy gap values up to 0.5eV, allowing their applications at room temperature. This particular technique makes it possible to avoid the disadvantages of “bottom-up” methods. At the same time, it enables to build entire working circuits.

Fabricating mechanical switches:



<u>Fig-10</u>: On/off current ratio as a function of the back gate bias voltage (V_b). Experimented values almost match the simulation values. There's only a slight mismatch between the experimented and simulated values[15].

Suspended few layer graphene beam electro-mechanical switches (SGS) with 0.15um air-gap are fabricated. A random on/off current characteristics has been identified in this SGS with minimal off current. The mechanical switch operates at a very low pull-in-voltage (VPI) of 1.85V. This value is well-matched with conventional complementary metal-oxide-semiconductor (CMOS) circuit requirements.

Engineering bandgap in Bilayer graphene:

The unique property in Bilayer graphene is an increased on/off ratio which is caused by the opening of a mobility gap. For mainstream logic applications, the major problem is that graphene acts as a metal even at the charge neutrality point. Still considerable energy bandgap can be engineered in graphene especially in bilayer graphene [2].

Another approach is to induce bandgap in single-layer graphene by spatial confinement or lateral-superlattice potential but this paper will not focus deep into that approach [2]. Like monolayer graphene, two layer graphene also lies on one another-having a zero band gap. But a gap can be introduced if the "mirror-like symmetry of the two layers is distressed" [21]. The material then starts behaving like a semiconductor instead of a metal.

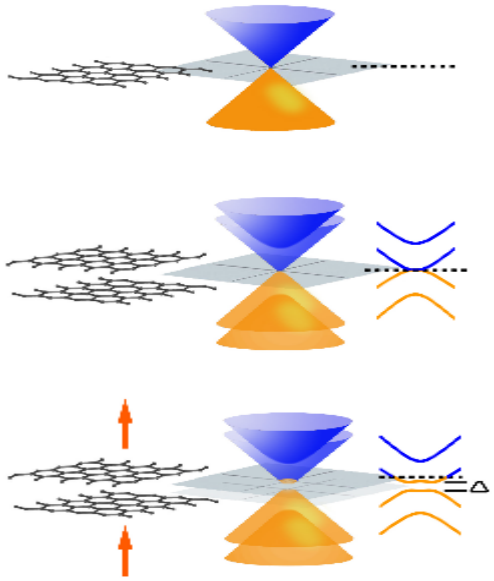


Fig11: One of the most unusual features of single-layer graphene (top) is that its conical conduction and valence bands meet at a point – it has no bandgap. Symmetrical bilayer graphene (middle) also lacks a bandgap. Electrical fields (arrows) introduce asymmetry into the bilayer structure (bottom), yielding a bandgap (Δ) that can be selectively tuned[21].

As chemical doping was uncontrollable, researchers started doping the substrate electrically. Perpendicularly applied, the electric field is continuously tunable. But when such a field is applied with a single electrode, the bilayer becomes insulating only at a certain temperature below one degree Kelvin, which is near absolute zero and that does not give the theoretical bandgap value at all. Then there was a change in their decision which directed a path towards opening a bandgap in bilayer graphene. Instead of a single-gated device, they fabricated a double-gated bilayer device which ultimately allowed the team to adjust the electronic bandgap and charge doping. This double-gated FET "controls the flow of electrons from a source to drain with electric fields shaped by the gate electrodes". A silicon substrate was used as the bottom gate accompanied by a thin layer of silicon dioxide in between it and the stacked graphene layers. Above the graphene bilayer, a transparent aluminium oxide (sapphire) layer was used. A platinum top gate was then placed on the top of it.

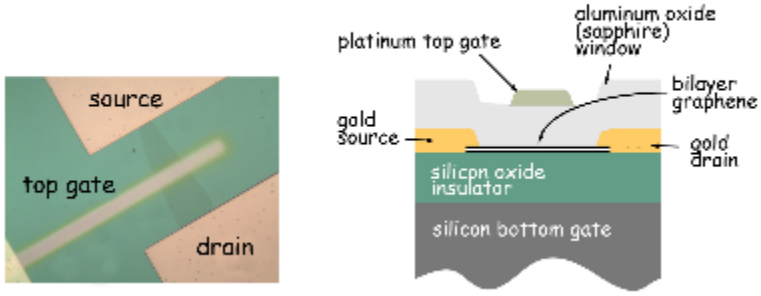


Fig12: From left, a microscope image looking down through the bilayer-graphene field-effect transistor. The second one displays the elements of the device [21].

Furthermore, the researchers then measured the device's optical transmission to measure the bandgap. Infrared beamline 1.4 at the ALS was used. Focusing on the graphene layers a tight beam of synchrotron light was sent through the device. The electrical fields were tuned by varying the voltage of the gate electrodes. And thus from these variations they were able to measure variations in the light absorbed by the gated graphene layers. In each spectrum the absorption peak offered a direct measurement of the bandgap at each gate voltage. Throughout

the method, the researchers demonstrated that the bandgap in bilayer graphene can be arbitrarily changed from 0 to 250 meV even at room temperature. Although the bandgap located in this device is remarkably narrower than semiconductors like silicon or gallium arsenide, it is capable of being used as optoelectronic devices for generating, amplifying and detecting infrared light.

5.Summary and Conclusion:

In this paper, the limitations of current semiconducting materials such as Si have been stated and thus the importance for an alternative candidate for nano-scale device manufacturing has been declared. This paper is an embodiment of graphene's prospects for future semiconductor fabrication industry, the characteristics of the material along with its limitations and some potential approaches to overcome the limitations. Furthermore it does look at the entire device fabrication process including obtaining graphene samples, etching using some useful lithographic processes to pattern the devices in a desired way. Through some simulation, the transfer characteristics, mobility and switching issues have been demonstrated. Though graphene is so far feasible, as interconnects or epitaxial layers for its excellent carrier mobility, methods have been discussed using which the switching attribute can be induced into a graphene device. Besides, as an approach to overcome the limitation of an absence of a bandgap,

Graphene is considered as a future star in the field of nano-electronics. With both its merits and demerits, it has been capable of grabbing the attention of the present day researchers and manufacturers. The methods discussed throughout the paper announce the victory of graphene in nano-electronics. In semiconductor industry, Si is still a reliable candidate for fabricating devices while in nano-scale device manufacturing, graphene is most likely to replace Si in the upcoming years with its extraordinary carrier mobility, unique structure, less dependency on temperature, excellent mechanical and electrical characteristics and so on. It is worth mentioning that the main limitation of graphene is a lack of a proper bandgap which arises the issue of switching characteristics of graphene. Graphene is still good to go as epitaxial layers or interconnects with its attractive carrier mobility. Though graphene device fabrication process has to go a long way to compete with well-established Si-based device manufacturing industry, still today graphene has already secured its place as a prospective candidate for device fabrication. The mention of bilayer graphene opening a new horizon for optoelectronics operation works as an eye-opener for interested researchers and manufacturers. However, some approaches have been proposed through which the on/off issue can be solved and thus graphene would be capable of being used as switching devices as well. With plenty of research going on vigorously throughout the world, it can be hoped that, the few limitations with graphene-devices will soon be defeated. It is no more a surprising fact that more than 200 companies and start-ups have already been involved in research that revolve around graphene.

Future work:

In future, the objective of this paper will be to look at the entire device-fabrication process using graphene. A spotlight will be placed on the prospective, effective and feasible approaches to fabricate all-graphene device as a continuation of the research. It will focus on device fabrication process as a whole including obtaining large-scale graphene samples, deposition, etching techniques using various lithographic techniques. As there is a glimpse of fabricating all-graphene devices with the methods of opening a significant band-gap in graphene, this approach will be more emphasized and its viability in future nanoelectronics industry will be examined thoroughly. Moreover there are issues still under question about how to induce a bandgap in 1D graphene which needs to be resolved through systematic research. In addition to that, the device characteristics such as carrier mobility within the device, I-V characteristics, roughness will be compared with existing traditional semiconductor devices.

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